A Reconfigurable Low Noise Amplifier for a Multi-standard Receiver

A Thesis

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By

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Declaration of Originality

I, Mohd Tafir Mustaffa, declare that the PhD thesis entitled “A Reconfigurable Low Noise Amplifier for a Multi-standard Receiver” is no more than 100,000 words in length including quotes and exclusive of tables, figures, appendices, bibliography, references and footnotes. This thesis contains no material that has been submitted previously, in whole or in part, for the award of any other academic degree or diploma. Except where otherwise indicated, this thesis is my own work.

Mohd Tafir Mustaffa

To my wonderful wife Khairunnisa Baruddin

and

my family.

ABSTRACT

Mobile devices are widely used for a vast range of applications such as mobile phones, personal digital assistant, personal computers, video games console, etc. However, the performance of these devices is restricted by the support of the network and the mobile functionality and efficiency. Current applications require high data rates and global mobility which can be satisfied with the co-existence and handover between newly developed third generation (3G) or Universal Mobile Telecommunication System (UMTS) standard and current second generation (2G) standards including: Global Standards for Mobile (GSM), Digital Cellular System (DCS), and Personal Communication Systems (PCS). Therefore, recent research in wireless communication has shifted towards achieving a multi-standard terminal, which can support efficiently multiple standards including GSM/DCS/PCS/3G.

References show that currently available multi-standard receivers employ parallel architecture to accommodate multiple standards. This option, however, is bulky, costly, complex, and consumes relatively high power. To address these limitations, current research trend is to merge the parallel paths into a single path wireless receiver. Literature review shows that currently available low noise amplifier (LNA) as part of this receiver, only support combination of a few mobile communication standards. Therefore, there is a need for a new LNA architecture that could support most of the 2G and 3G standards.

In this research, the aim is to design and implement a new LNA for a multi-standard mobile receiver based on reconfigurability concept. This research was carried out in two major parts. The first part is to design and implement wide band multi-standard multi-band LNAs for two bands of interest (lower frequency band – 800 to 1000 MHz and upper frequency band – 1800 to 2200 MHz). These two bands should cover most of the 2G and 3G standards currently in use worldwide. In this work, the design of LNA based on IDCS topology using wide band approach has been investigated, designed, implemented and approved by means of simulations, and measurement of fabricated ICs. The second part of this research, to develop a single reconfigurable multi-standard multi-band LNA is based on the design of the multi-standard multi-band LNAs. This LNA has the capability to function in two modes of operation, either at lower band or upper band of the 2G or 3G standards.

The significance of this research is to respond to the industries need of multi-standard multi-band LNA with simple architecture. This LNA is less complex, more power efficient and cost effective compared to the parallel architecture in the design of the multi-standard RF receiver architecture. Therefore, the proposed reconfigurable LNA provides access to functions such as voice calls, video calls, multimedia messaging, online TV, video on demands, etc. at a high data rate more efficiently.

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LIST OF ABBREVIATIONS

2G	Second Generation
3G	Third Generation
3GPP	3rd Generation Partnership Project
ADS	Advanced Design System
BER	Bit Error Rate
BiCMOS	Bipolar CMOS
BPF	Band Pass Filter
CEDEC	Collaborative µElectronic Design Excellence Centre
CG	Common Gate
CMOS	Complementary Metal Oxide Semiconductor
CNR	Carrier to Noise Ratio
CS	Common Source
DCR	Direct Conversion Receiver
DCS	Digital Cellular System
drc	design rule check
DUT	Device Under Test
EGSM	Enhanced-GSM
ETSI	European Telecommunication Standards Institute
GMSK	Gaussian Minimum Shift Keying
GPS	Global Positioning System
GSG	Ground-Signal-Ground

GSM	Global Standards for Mobile
IDCS	Inductively-Degenerated Common Source
IF	Intermediate Frequency
IP2	Second Order Intercept Point
IP3	Third Order Intercept Point
LNA	Low Noise Amplifier
LO	Local Oscillator
lvs	layout versus schematic
MEMS	Micro Electro Mechanical System
NCSU	North Carolina State University
NF	Noise Figure
NQS	Non-Quasi Static
PCS	Personal Communication Systems
pex	parasitic extraction
QPSK	Quadrature Phase-Shift Keying
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
SiGe	Silicon Germanium
TI	Texas Instrument
TOI	Third Order Intercept Point
UMTS	Universal Mobile Telecommunication System
USM	Universiti Sains Malaysia
UWB	Ultra Wide Band

VCO	Voltage Controlled Oscillator
WCDMA	Wide Code Division Multiple Access
WLAN	Wireless Local Area Network

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Journals

1. Mustaffa M.T, Zayegh A, Veljanovski R., Stojcevski A., and Zulkifli T.Z.A., "CMOS Low Noise Amplifier for wideband mobile receiver," Accepted for publication in Journal of the Advancement of Modelling and Simulation Techniques (AMSE), France, in 2008.

Conference papers

1. Mustaffa M.T, Zayegh A, Veljanovski R., Stojcevski A., and Zulkifli T.Z.A., "0.18 μm Fully Integrated 900 MHz CMOS LNA with Input and Output On-chip matching for Multi-standard Mobile Receiver," Proceedings of IEEE International Conference on Microelectronics**,** 14-17 December 2008, Sharjah, UAE.

2. Mustaffa M.T, Zayegh A, Veljanovski R., Stojcevski A., and Zulkifli T.Z.A., "Fully Integrated 2-GHz LNA with On-chip matching for Multi-standard Mobile Receiver using 0.18 μm CMOS Technology," Proceedings of IEEE TENCON International Conference, 18-21 November 2008, Hyderabad, India.

3. Mustaffa M.T, Zayegh A, Veljanovski R. and Stojcevski A., "A 0.8 GHz to 1 GHz 0.25 μm CMOS Low Noise Amplifier for Multi-standard Receiver," Proceedings of IEEE International Conference on Intelligent & Advanced Systems**,** 25-28 November 2007, Kuala Lumpur, Malaysia.

4. Mustaffa M.T, Zayegh A, Veljanovski R. and Stojcevski A., “A 1.8 GHz to 2.1 GHz 0.25 µm CMOS Wideband LNA for a Multi-standard Mobile Receiver,” Proceedings of IEEE International Symposium on Integrated Circuits (ISIC), 26-28 September 2007, Orchard Hotel, Singapore.

5. Mustaffa M.T, Zayegh A, Veljanovski R. and Stojcevski A., “Optimised Low Noise Amplifier for Multi-standard Receiver Architecture,” Proceedings of International Conference on Advanced Technologies in Telecommunications and Control Engineering (ATTCE), 28-29 August 2006, INTI College, Malaysia.

CHAPTER 1:

THESIS OVERVIEW

1.0 Introduction

The increasing demands of higher data transfer rates and global mobility in current wireless communication environment has led to the development of the Third Generation (3G) mobile communication standard. Nowadays, many small and large operators, serving both developed and emerging markets, are already reaping the benefits of 3G technologies. As of January 2008, there were 435 3G operators (service providers) worldwide, with more than 560 million subscribers in 143 countries [1].

The 3G wireless communication system provides voice communication together with multimedia communication such as video, internet, real TV, live cast, etc. as is represented in Figure 1.1. It supports Universal Mobile Telecommunication System (UMTS) or Wide Code Division Multiple Access (WCDMA) standard and also provides a backward compatibility with Second Generation (2G) systems [2-9]. Typical standards currently being used for 2G systems are: Global Standard for Mobile (GSM900) and Digital Cellular System (DCS1800) and Personal Communication System (PCS1900) [2-9]. In other words, the new 3G phone is a representation of new wireless trend toward the integration of multiple standards multiple functions into one wireless device that is targeted to be used virtually anywhere in the world.

Figure 1.1: 3G phone with various applications [1]

Due to increasing demand on the 3G mobile, QUALCOMM, Texas Instrument (TI), etc. (companies that provide chipset solution for 3G systems) have come up with systems using parallel architecture to cover various standards [10-12]. This concept of parallel architecture maybe originated from various radio frequency (RF) multi-standard multi-band parallel systems which were developed over the past years as shown in references [13-20]. Unfortunately, this type of implementation is very area inefficient, costly and consumes relatively high power due to the fact that different standards need

different systems or devices. In other words, consumers are paying additional cost for the added complexity of such a system. In addition, with the complex functionality (e-mail, video call, etc.), the issue of a shorter battery life of a 3G phone compared to well-known GSM mobile is quite common, as the battery might go flat within just one day, or even worse, within hours if heavy usage of the 3G mobile took place.

Having mentioned the problems with the current solutions, it is impractical in the future to adapt such implementation in designing the multi-standard multi-band mobile device, as more and more 3G wireless standards are emerging [8-9]. With these emerging standards, wireless mobile system is more complex and the system integration is virtually impossible or hard to be realised and impractical. Therefore, the search for a new system or architecture seems to be evident. Solutions to these problems are possible by introducing a new architecture with reconfigurability features that should be able to support most of the available standards [8-9].

With respect to this approach, it is possible to develop a new architecture that can cover various standards with just one single terminal, compared to the current architecture that uses a single terminal for each single standard. For instance, as GSM comprise standards that use multiple bands in the lower frequency bands: 850 and 900 MHz and the upper frequency bands: 1800 and 1900 MHz [2-9], two new circuits (in particular, low noise amplifier (LNA) as it is the main work of this research) could be designed to support these lower and upper frequency band regimes.

For the reconfigurability feature, the principle refers to the ability of the circuit to perform changes in function due to the operating environment by selecting certain section of the circuit at one time to operate, while the other sections can be switched off to reduce power consumption. Referring to this research work, reconfigurable means to modify the hardware structure to respond to the two major bands of interest (i.e. lower and upper frequency band regimes) depending on the availability of the mobile communication systems (GSM or 3G).

To design such a new architecture with reconfigurability feature, a platform (i.e. mobile receiver system) is required. Since LNA is part of the receiver system, a good receiver architecture that is suitable for multi-standard multi-band implementation is needed. From the literature, direct conversion receiver (DCR) architecture is believed to be the most suitable architecture for single-chip multi-standard multi-band mobile receiver [18-19]. This is because of its advantages such as simple circuit architecture and less off-chip components, leading to low power consumption with possible integration as a single-chip radio [18-24].

In DCR architecture, RF signal is amplified and converted to baseband signal in only one stage. Typically, DCR architecture consists of a Band Pass Filter (BPF), a LNA, a mixer, a voltage controlled oscillator (VCO), etc. In DCR architecture, LNA is considered as the most important block, as it directly affects the performance of the receiver. It amplifies the RF signal to a sufficient power level required for the subsequent stages to

process the signal and at the same time offers low noise figure (NF) and high linearity to increase the accuracy and performance of the system.

For years, LNA has been the topic of research due to its different performance requirements for different standards [25-33]. Gain, NF, linearity, and low power consumption are the major specifications in the design of LNA, and the most important parameter is NF. To achieve a low NF, common source stage with inductive degeneration showed the best noise performance with good gain and sufficient linearity with a trade-off with power consumption [25-27]. Several techniques and methods have been tried in order to produce a LNA with low NF [25-33], but, most of these methods and techniques are limited to the single standards only.

However, due to the high demand of multi-standard device, the trend of LNA design seems to move from single-standard to multi-standard LNA, with different methods and topologies as appears in literatures [34-39]. The most popular technology nowadays used to implement LNA is complementary metal oxide semiconductor (CMOS) technology which offers low power consumption and low cost solution [25-30].

In this research, an attempt to investigate and to develop effective ways of implementing architecture to support multi-standard multi-band personal wireless communications system has been performed.

1.1 Research methodologies and techniques

The aim of this research is to design and implement a low power, low noise, reconfigurable LNA using CMOS technology for a multi-standard multi-band mobile receiver based on industry-standard. The design and implementation of the LNA will provide the reconfigurable feature which allows the selection of different standards such as: GSM and 3G. In addition, the design of reconfigurable LNA was based on industry-standard process technologies and libraries such as that from MOSIS and Silterra which is similar to the technologies used by major microelectronics companies such as Intel, IBM and Freescale. Design, implementation, simulation and measurement were carried out using leading design tools and instruments: Agilent Design Suite (ADS), Cadence Design Suite (Spectre RF), Mentor Graphics (Calibre) and Agilent's instruments etc.

The details of proposed methodology and techniques to achieve the requirements of this research project are as follows:

1.2.1 Analysis of the currently available systems / Literature review

This initial stage of the research program involved searching the state of art in the field of multi-standard receiver systems especially the receiver architectures. One important aspect of this research is to understand the wireless receiver architectures and their requirements. The system level standards for GSM, DCS, PCS and UMTS have been reviewed, studied and simulated using Advanced Design System (ADS) from Agilent to

see the relation between receiver specifications and components specifications, especially LNA, as it is the main focus of this research. This step of analysis in the research provides the optimum LNA specifications, extracted from the receiver's specifications, which will be used as guideline for designing the LNA at the later stage of the research.

1.2.2 Design and implementation of wide band CMOS LNAs for multi-standard receiver

Based on the extracted specifications from receiver standards, two wide band CMOS LNAs were designed and implemented for multi-standard receiver. These LNAs were designed for two bands of interest which are lower frequency band (800 to 1000 MHz) and upper frequency band (1800 to 2200 MHz) respectively. To achieve this implementation, various CMOS LNA's topologies or methods were reviewed and studied. Wide band multi-standard multi-band LNAs were designed, simulated and implemented using the Cadence design suite based on 0.25 µm industry-standard process technology and library from MOSIS. At this stage, only ideal passive components used. Subsequently, the process of designing continued with the design and implementation of LNAs using more realistic technology and library provided by foundry (Silterra Malaysia). For this purpose, 0.18 µm process technology was used.

1.2.3 Layout implementation and fabrication of wide band CMOS LNAs for multi-standard receiver.

After the wide band LNAs was successfully designed and simulated, the research development moved forward with the layout implementation and fabrication. In this stage, post-layout simulations were carried out to verify the validity of circuit design; the layout has been implemented using 0.18 µm technology by means of Cadence tools, while Calibre tools were utilised to obtain post-layout design rule check (drc), layout versus schematic (lvs) and parasitic extraction (pex). Based on the successful results from the simulation, the layouts have been submitted for fabrication.

1.2.4 Test and measurement of the fabricated LNAs

This step has been carried out at the Collaborative µElectronic Design Excellence Centre (CEDEC) at Universiti Sains Malaysia (USM) using a leading measurement instruments available at the centre. The measurement has been carried out to measure the parameters of the fabricated LNAs: s-parameters (gain, input and output return losses and reverse isolation) and linearity parameters: third order intercept point (TOI) and compression point (P1dB).

1.2.5 Design and implementation of reconfigurable multi-standard multi-band LNA

This step involved the design and implementation of a single reconfigurable multi-standard multi-band LNA for mobile receiver. The reconfigurable LNA has been designed in such a way that, it has the capability to support two bands of interest which are lower frequency band (800 to 1000 MHz) and upper frequency band (1800 to 2200 MHz) respectively.

1.2 Organisation of the Thesis

This thesis contains seven chapters and is organised as follows:

Chapter 1 provides the introduction about this research as well as the motivation behind this research. This chapter also includes the research methodologies, techniques and the contribution of this research to the knowledge of science and engineering.

Chapter 2 presents the literature review of multi-standard multi-band RF wireless mobile communication systems, the RF receiver standards and recent developments in radio frequency integrated circuit (RFIC) mobile devices – RF receiver architectures and LNAs.

The theories and methodologies used for designing LNA, followed by the development of the proposed LNA design for upper and lower frequency band LNAs have been

presented in Chapter 3. Chapter 4 presents detailed pre-layout and post-layout experimental results and analysis of upper band and lower band LNAs.

Chapter 5 presents the test and measurement results of the fabricated LNAs. Chapter 6 elaborates on the design and implementation of reconfigurable LNA for multi-standard multi band receiver system. The conclusions and future scope for this research are discussed in Chapter 7.

1.3 Originality of the Thesis

This research contributes to the knowledge in RFIC system design and manufacturing particularly in wireless communication system. The design and development of a new reconfigurable LNA architecture is believed to be one of the pioneering attempts in providing new trend of designing LNA for multi-standard multi-band RF receiver system.

This research contributes to knowledge in the following specific areas:

(1) Identifies the minimum and optimum requirement of LNA's specifications in relation to the receiver's specification. The proposed research will be immensely beneficial to RF engineers since it further enhances the understanding of the mutual relationship between RF receiver systems and RF components specifications (specifically LNA).

(2) Demonstrates the critical issues and challenges behind the design and development of LNA for multi-standard multi-band RF receiver system.

(3) Provides a new architecture which is less complex, more power efficient and cost effective compared to the parallel architecture which is currently being employed in designing the multi-standard multi-band RF receiver architecture.

(4) Proposes a new methodology for designing LNA for relatively wider band system to support multi-standard and multi-band with just one single circuit implementation.

(5) Contributes to knowledge by proposing a new reconfigurable LNA architecture to support multi-standard multi-band RF receiver system.

CHAPTER 2:

LITERATURE REVIEW

2.0 Introduction

The purpose of this chapter is to provide the necessary background required to revise the concepts of multi-standard multi-band RF wireless mobile communication systems, the RF receiver standards and recent developments in RFIC mobile device systems.

Strong demands for multi-standard multi-band devices (to cover standards available in almost anywhere in the world) with more functionality (i.e. video call, games, email etc.) for wireless mobile devices invites the RFIC community to focus on the design of compact systems. Consequently, nowadays, mobile devices come with several standards to support multiple functions as described earlier in Chapter 1.

3G systems generally support multiple mobile communication standards such as GSM and UMTS/WCDMA [2-9]. With respect to those standards, current multi-standard multi-band mobile devices support parallel architecture of the RF receiver system on a single-chip to cover GSM and 3G standards. Specifically, industries use parallel components such as RF filters and LNAs at the front-end receiver of mobile devices to support those standards [10-12]. Unfortunately, this implementation is very area inefficient, costly and consumes relatively high power. Thus, a better solution is needed

to produce a compact mobile device to meet the need for a multi-standard multi-band system with more functions that could result in the reduction of the cost and complexity of the system as well as power consumption.

Referring to work presented in [40], it proposed a single multi-standard LNA in combination with several RF filters at the front-end circuit to meet the need for multiple standards devices. In another proposal [41-45], reconfigurable architecture is used, using the concept of hardware sharing with also multiple RF filters at the very front-end of the RF receiver. The proposed architectures reduce the complexity, power consumption and components used in current solutions.

In conclusion, multi-standard radio architecture involves a lot of design issues such as the following [40] [47]:

• A multi-standard receiver must have minimum component count and area and to continue miniaturisation.

• All the considered standards do not need to be covered at the same time, i.e., when specific band or standard is active, the others can be switched off or in idle mode, in order to save power and reuse hardware resources.

To highlight more details on the concepts of mobile communication system and issues regarding it as mentioned above, this chapter is arranged as follows. Section 2.1

elaborates on multi-standard RF systems with details about the RF standards and RF receiver architectures used for mobile communication systems, and followed by the developed mobile devices in current and past years. Section 2.2 covers the reconfigurable LNA for multi-standard systems and provides details of the developments of mobile devices that have reconfigurability features. Conclusion remarks are made in Section 2.3.

2.1 Multi-standard RF Systems

As stated in the previous section, multi-standard RF systems consist of several standards such as GSM and 3G standards. In this section, some details on the RF standards in terms of frequency allocation, modulation techniques used, etc are provided. Then, followed by the presentation of RF receiver architectures used to support those standards. Finally, this section will end up with the discussion of the recent and past developments of the multi-standard RF mobile systems.

2.1.1 RF standards

In this section, the requirements of the GSM and 3G standards are systematically mapped onto set of measurable specifications for receiver architecture.

2.1.1.1. RF Standards to receiver specifications

RF standards can be categorised in two groups: GSM and 3G/WCDMA/UMTS. GSM consists of several standards such as GSM850 and GSM900 with carrier frequencies of 850 MHz and 900 MHz. Other standards which fall in this group are the DCS1800 and PCS1900 with carrier frequencies of 1800 MHz and 1900 MHz [3-4]. While WCDMA/UMTS standards consist of bands with carrier frequencies of 850 MHz to 2100 MHz, also known as UMTS band I to VI [5] [7].

The original version of the GSM standards was developed by European Telecommunication Standards Institute (ETSI) and evolved through out the time. Table 2.1 shows the frequency allocation for the GSM systems. Specifically, GSM850, GSM900 and DCS1800 are used in Europe, while PCS1900 is deployed in the United State (U.S.) [1-7]. While, Table 2.2 gives the summary of the band allocation for 3G.

In terms of the characteristics of the GSM and 3G systems such as modulation scheme, channel bandwidth, etc., the most relevant parameters that refers to both standards are summarised in Table 2.3.

Reference [4] clearly shows that the receiver requirements for all the GSM standards are very similar. Though they are very similar, GSM900 is considered to be the strictest version in terms of receiver specifications. Hence, for the sake of clarity, our analysis will be based on this standard. Similarly, for 3G, all the standards are very similar but

3G standard (Band I) is the common standard and is believed to be the first draft [6]. For that, 3G standard (Band I) will be referred for the discussion in this thesis.

Table 2.1: Frequency allocation for GSM systems [2-4]

Operating Band	Uplink Frequencies; Mobile transmits, base receives.	Downlink Frequencies; Base transmits, mobile receives.
GSM850	824 MHz to 849 MHz	869 MHz to 894 MHz
GSM900	890 MHz to 915 MHz	935 MHz to 960 MHz
DCS1800	1710 MHz to 1785 MHz	1805 MHz to 1880 MHz
PCS1900	1850 MHz to 1910 MHz	1930 MHz to 1990 MHz

Table 2.2: Frequency allocation for UMTS systems [7]

Operating Band	Uplink Frequencies; Mobile transmits, base receives.	Downlink Frequencies; Base transmits, mobile receives.
I	1920 - 1980 MHz	2110 -2170 MHz
II	1850 -1910 MHz	1930 -1990 MHz
III	1710-1785 MHz	1805-1880 MHz
IV	1710-1755 MHz	2110-2155 MHz
V	824 - 849 MHz	869-894 MHz
VI	830-840 MHz	875-885 MHz

Table 2.3: Signal characteristics for GSM/3G systems

Parameters	GSM	3G
Modulation Technique	GMSK	QPSK
Channel Bandwidth	200-kHz	3.84-MHz
Channel Separation	200-kHz	5-MHz
Data Rate	270.8-kbs	3.84-Mbs

To understand the behavior of GSM and 3G systems, the key characteristics of these systems such as sensitivity, selectivity and linearity are needed to be understood. Sensitivity, selectivity and linearity are modelled in terms of the system performance parameters, including NF, carrier to noise ratio (CNR) and TOI or also known as third-order intercept point (IP3). The required system characteristics are directly governed by the standards to be supported by the system. Every wireless communication standard has clearly defined characteristics for radio transmission and reception [2-9]. Critical transmission and reception limits are defined by the standard along with the modulation, demodulation schemes and other parameters. In this chapter, only NF, gain and TOI are discussed as these are the most important parameters that will be required for LNA characterisation or derivation from the receiver specifications which will be covered later in the following section.

Sensitivity, as one of the key specification of receiver design, is defined as the ability of the receiver to detect minimum signal in the presence of the noise and interferers at an

acceptable bit error rate (BER). The system NF of the receiver for the GSM standard is normally used as the measure of the sensitivity.

For GSM900, a sensitivity level of -102 dBm is required with system NF of 10 dB. Meanwhile, the system NF for WCDMA is 9 dB and a sensitivity level of -117 dBm is required.

On the other hand, the system transfer function must be linear over the wide dynamic range of the input signal in the presence of the blocking interferers. Linearity of the system is modelled by IP3. Input IP3 (IIP3) for GSM systems is about -19.0 dBm. For 3G, IIP3 required is a bit lower with the value of -19.1 dBm.

Another major specification to be considered in the receiver system is gain. The required system gain for GSM and 3G standards is generally more than 60 dB. This required gain is distributed amongst all the RF front-end components. The maximum gain achievable by any component is limited by the circuitry.

Table 2.4 gives the summary of the specifications for GSM and 3G systems. The complete set of RF specifications set by the 3rd Generation Partnership Project (3GPP) can be found in [3-9]. In addition, more explanations about the RF specifications are described in [46-48].

Table 2.4: Receiver specifications for GSM/3G systems and the proposed specifications for multi-standard system [46-48]

Specification	GSM	3G	Multi-standard
Sensitivity (dBm)	-102	-117	-117
CNR (dB)	10	9	9
System IIP3 (dBm)	-19	-19.1	-19
System NF (dB)	10	9	9
Gain (dB)	> 60	> 60	> 60

2.1.1.2 From receiver specifications to LNA specifications

Having reviewed the requirements for RF receiver specifications, the specifications have to be translated into specifications for receiver's components, in particular LNA. According to the previous work in [47], Table 2.5 gives the summary of the requirements for the LNA derived from the system simulation which has been carried in ADS from Agilent. Also, in Table 2.6 the collection of extracted specifications of LNA from literature as comparison to the ideal LNA specifications are presented.

Tables 2.5 and 2.6 show that the specifications for LNA are not fixed but flexible, depends on the requirements of the receiver's specifications. For example, if the specifications for the LNA are set to be stringent, this means that the specifications for the following blocks of the receiver's component can be relax or vice versa. In addition, for IIP3, the achieved

specification values were ranging from -2.5 to -4.0 dBm as in [65] [69] down to -7.2 to -14.0 dBm [34] [35]. This is probably due to the different optimisation were took place and it is always hard to trade-off between various specifications (i.e. NF, gain etc.) Same goes for the NF, where in [65], it achieved the best NF performance compared to others.

Table 2.5: Ideal LNA specifications proposed for multi-standard multi-band system

Specification	Optimum range	Optimum point
Gain (dB)	10 to 20	20
NF (dB)	1 to 6	1
IIP3 (dBm)	-5 to 5	5

Table 2.6: Typical LNA specifications proposed for multi-standard multi-band system

	Gain max. (dB)	NF (dB)	IIP3 (dBm)
[34]	≤ 14	≤ 2.9	-14
[35]	14.2	5.2	-7.2
[65]	12	0.76	-2.5
[69]	≤14.2	≤ 2	≤ -4

2.1.2 RF receiver architectures

Recall from the previous section, a system to support mobile communication standards is needed. Part of that system is called RF receiver section. There are several RF architectures which are being used for decades and becoming popular overtime. These are superheterodyne architecture, homodyne architecture, image-reject architecture and low-IF architecture. However, in this chapter, only superheterodyne architecture and homodyne architecture will be discussed as other architecture i.e. low-IF is rather suitable for narrowband technique but this research is focus on wide band approach. In the following sub-sections, these two architectures are examined and described in terms of their merit and demerit.

2.1.2.1 Superheterodyne receiver architecture

As early as 1916 [49], superheterodyne or heterodyne receiver architecture was introduced and becoming widely used architecture for wireless mobile architecture for decades because of its superior selectivity and sensitivity. As shown in Figure 2.1, this architecture consists of a collection of components such as filters, oscillators etc. using combination of several technologies such as silicon bipolar and Complementary Metal Oxide Semiconductor (CMOS) are used for its component fabrication.

In heterodyne receiver architecture, first, the signal band is translated down to some intermediate frequency (IF) which is usually much lower than the initially received frequency band. This relaxes the requirements for the channel selection filter. The

process of translation also performs image rejection. Next, as the first mixer down-converts frequency bands symmetrically located above and below the local oscillator (LO) frequency to the same center frequency, an image reject filter in front of the mixer is needed. This filter (passive off-chip component) is further attenuating the interfering signals and the noise of the LNA at the image frequency. The rest of the processes are shown in Figure 2.1.

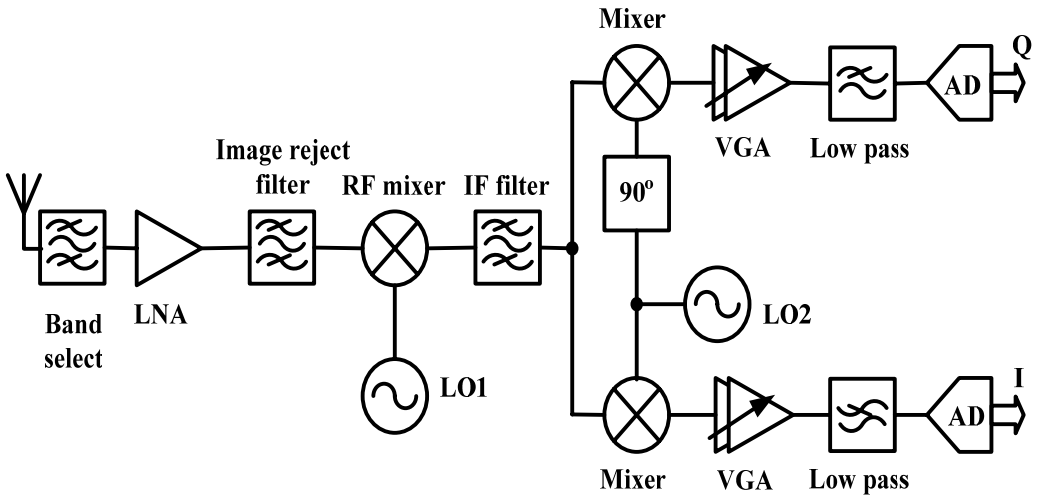

Figure 2.1: Superheterodyne architecture [48]

The adaptability to different receiver requirements is a major advantage of the heterodyne receiver. It provides superior performance in terms of selectivity and sensitivity; however, the need for a large number of external components and the complexity of the structure, make it virtually an impossible choice for high level of integration if needed. The major drawback of this architecture is the external components used which are expensive and bulky. Also, important disadvantage of the heterodyne receiver architecture is its missing adaptability to different wireless

standards and modes. Moreover, since external IF filters are optimised for a certain mode of operation (i.e. GSM900 or DCS1800), which results in a fixed bandwidth and center frequency, it cannot be re-used for a different mobile communication standard [50] [55-64].

2.1.2.2 Homodyne receiver architecture

Compared to heterodyne, homodyne architecture (also known as DCR or zero-IF architecture) is considered as the most suitable architecture for single-chip multi-standard multi-band mobile, because no intermediate stage required, less off-chip components used, leading to low power consumption with possible integration as a single-chip radio [18-24].

In the DCR architecture, RF signal is amplified by the LNA and converted to baseband signal in only one stage. This is done by mixing the RF signal with an LO frequency that is equal to the carrier frequency. In other words, LNA amplifies the RF signal power to a sufficient level required for the subsequent stages to process the signal and at the same time offers low NF and high linearity to increase the accuracy and performance of the system.

Typically, DCR architecture consists of a BPF, a LNA, mixer, a VCO, etc. As shown in Figure 2.2, DCR architecture is characterised by a smaller number of functional components in the receiver. Moreover, it is free from image problem if quadrature down-converter is used [50]. The IF SAW filter and the subsequent down-conversion stages

are replaced by low pass filters and baseband amplifiers that can be easily integrated in the receiver architecture.

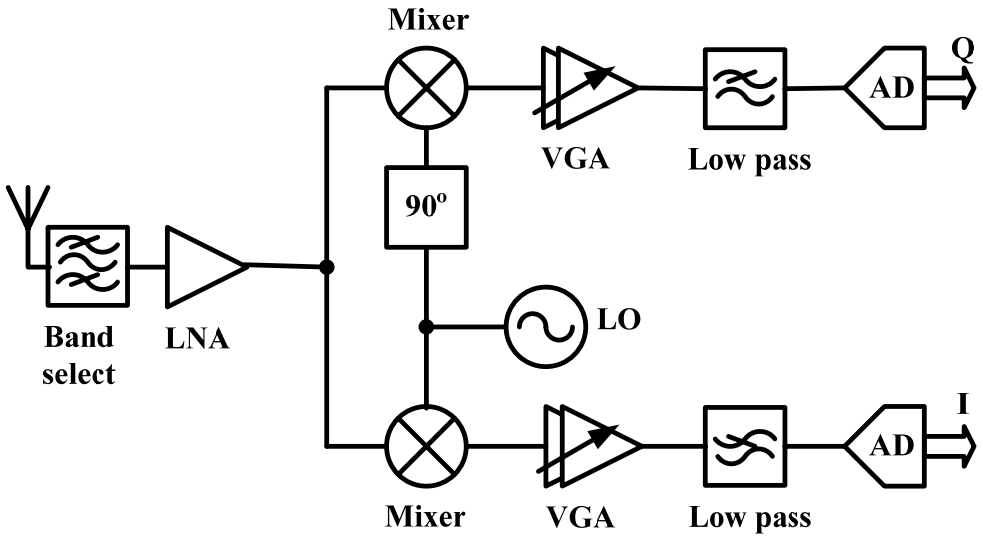

Figure 2.2: Homodyne architecture [46]

On the other hand, even though DCR architecture has several advantages over heterodyne architecture, it also has its own problems, but not as serious as in the heterodyne architecture. This is due to the fact that the down-converted frequency band to zero frequency led to the corrupted RF signal because of the offset voltages. This problem called as DC offsets. This problem occurs due to the 'self-mixing' phenomenon [51-53].

Another issue associated with DCR is I/Q mismatch [51-54]. The mismatch distorts the constellation diagram of the baseband signal, and consequently causes an increased BER. But, this problem can be resolved by the use of the pilot symbol assisted channel

estimation in WCDMA system. In addition to that, with higher levels of integration, I/Q mismatch will eventually be less significant.

Another problem exist in DCR is even-order distortion [51-54]. Typically RF receivers are susceptible to only odd-order intermodulation effects, but in DCR, even-order distortion also becomes problematic. As illustrated in Figure 2.3 (a), two strong interferers close to the channel of interest, experience nonlinearity in the LNA that generates a low-frequency beat in the presence of even-order distortion. But, because of the mismatch of the mixer and LO's deviation, a finite direct feed through will happens at the output showing that low-frequency beat standing beside the RF signal.

Another problem of even-order distortion is associated with the second order harmonic of the desired RF signal which is down converted to the baseband, then mixed with the second harmonic of the LO output which produces the second-order nonlinearity, as shown in Figure 2.3 (b). The bottom line is that, even-order distortion put a stringent requirement for second order intercept point (IP2). A feasible solution for this problem is by using differential components or balanced circuits i.e. differential LNA and mixers. Another solution is by designing circuits with high common-mode rejection, near perfect balance between differential arms of I/Q signal paths, as well circuit topologies to improve phase quadrature between the I/Q signals [54].

Last but not least, flicker noise also is one of the major issues related to DCR architecture. Since the down converted RF signal in DCR is located around zero

frequency, the 1/f noise of the device has a profound effect on the signal especially in MOS implementations. Fortunately, this problem can be reduced by a combination of techniques such as a relatively larger device and periodic offset cancellation. Moreover, for a broadband or wide band system such as WCDMA system, the effect of the flicker noise is much lower [54].

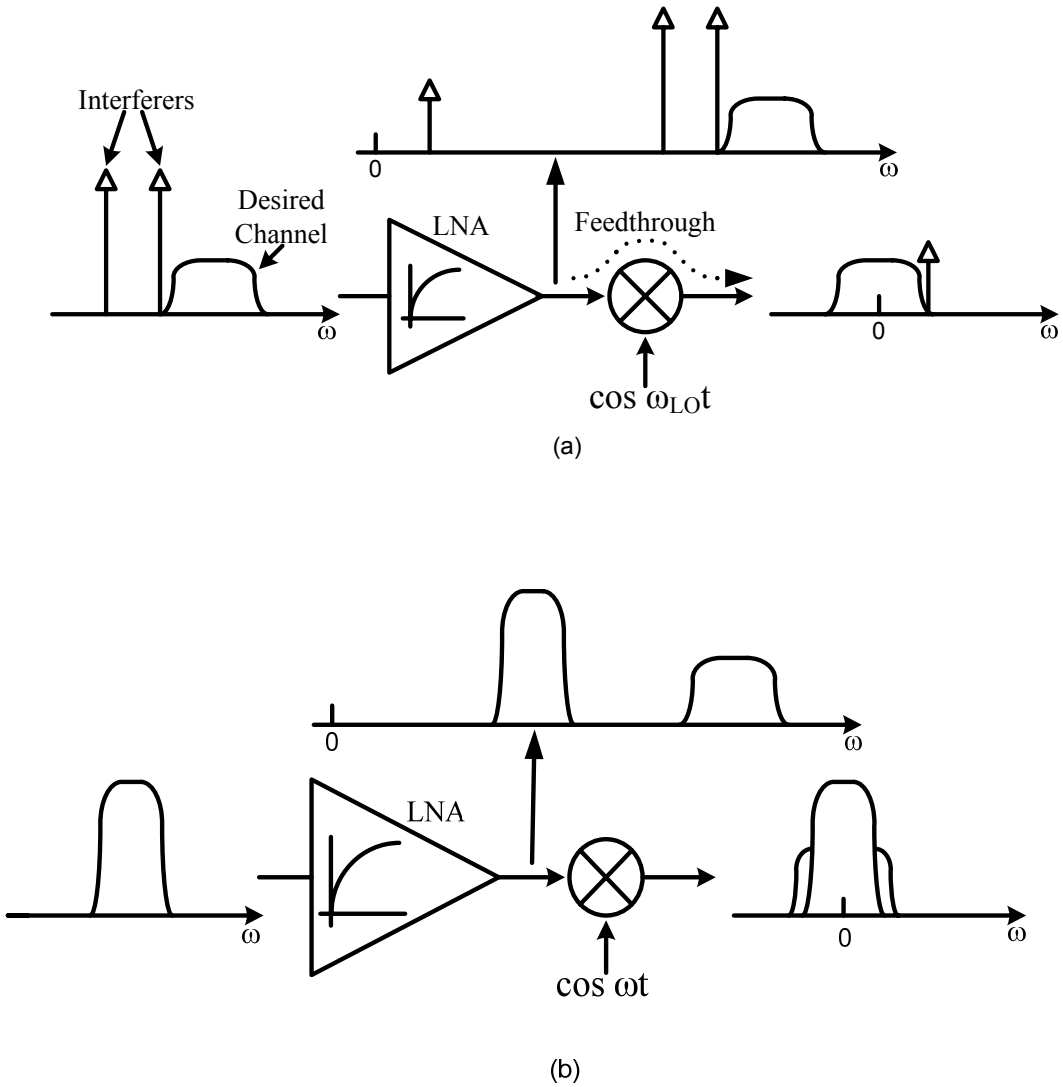

Figure 2.3: Effect of even-order distortion [51]

Despite of all the above mentioned problems, DCR is eventually becoming the designer's choice over heterodyne and is now adapted by most of the companies for designing RF receiver system [10-13] [18-24]. It is also worth to mention that, another receiver type, the low-IF architecture, is also gaining the designer's attention [40] [46]. However, it will not be discussed in this thesis as it works well for rather narrowband system which is not the focus of this work.

At this point, it is clear that DCR is more suitable for monolithic integration over other architectures, especially when dealing with wide band system, but none of the architecture discussed offers reconfigurability features with respect to integration level, power consumption, components design, etc. Therefore, a new architecture is needed to meet the requirements of multi-standard multi-band mobile receiver. The straight way to do that is to modify the available architecture, in particular DCR or even heterodyne, by making it reconfigurable that has the ability to adapt itself with the change in the mobile operating system. For this reason, Section 2.2 will highlight in more detail the reconfigurable feature whether at systems or components level.

2.1.3 The development of RF receiver architectures

Since the demand for multi-standard mobile device increases, RF engineers have started to design systems based on parallel architecture as it is easier to implement. The external review has been received on recent systems including many LNAs, that increase the cost, complexity, and power consumption of the system. This is

substantiated in the following reference papers: [10-20]. These papers show the examples of the current research and development, even the marketed products of RF receiver system based on parallel architecture. For instance, Figure 2.4 shows how several standards such as GSM, Enhanced-GSM (EGSM), DCS and PCS of GSM group can be integrated into one system using parallel structure. This system is based on DCR architecture.

In another example, similar approach has been developed as shown in Figure 2.5. It is even more interesting because it give more functionality to the mobile device, where the system currently employs WCDMA or 3G standard with multiple bands and other wireless standard i.e. Global Positioning System (GPS) [10]. This system is currently available in the market, supplied by the well-known company (QUALCOMM) which provides chipset solutions to all mobile manufacturers. In addition, similar approaches in the development of the mobile device systems are presented in [10-20].

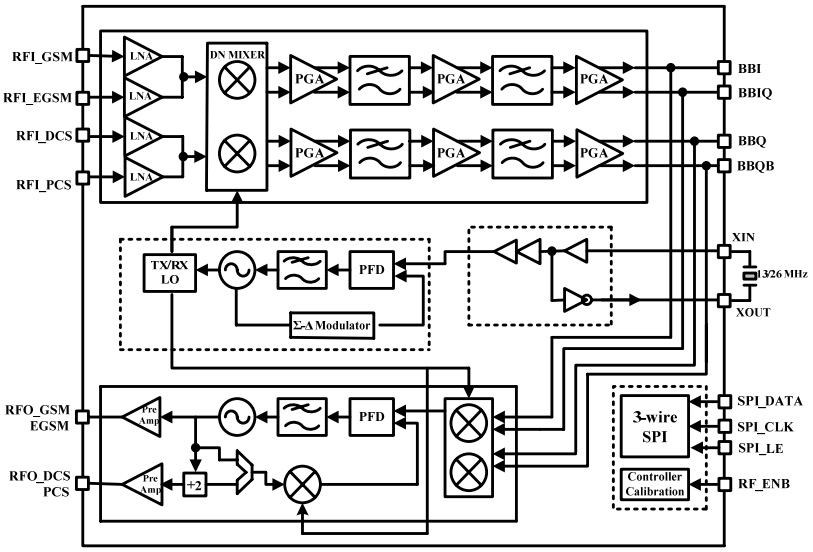

Figure 2.4: Parallel DCR architecture for multi-standard mobile as in [20]

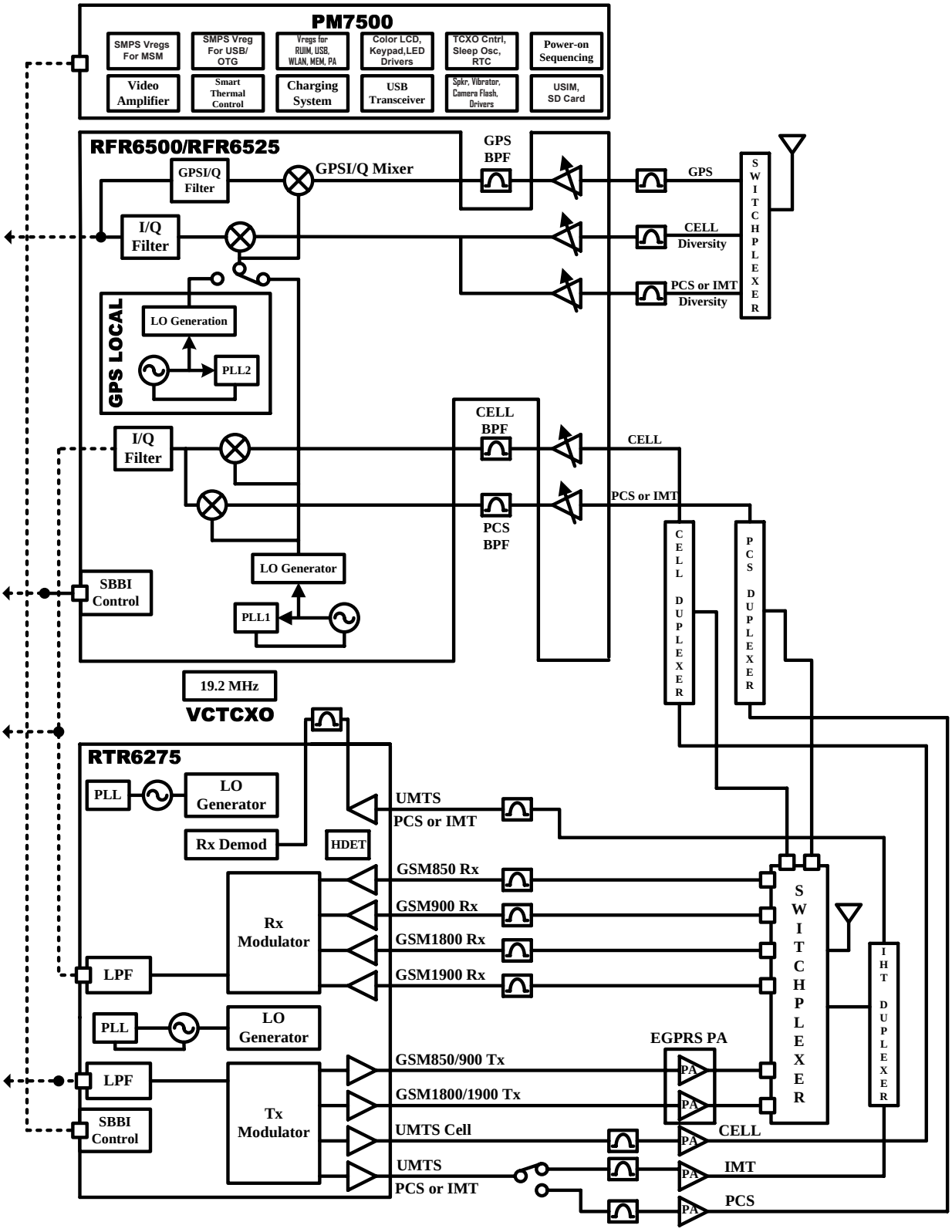

Figure 2.5: QUALCOMM chip solution (redrawn partly) [10]

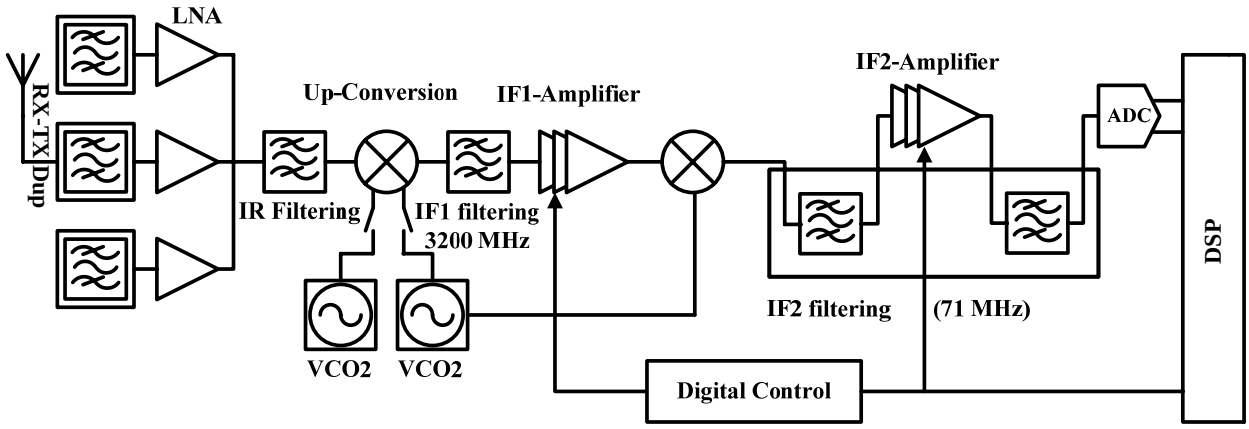

Figure 2.6: Superheterodyne receiver as in [55]

It is worth mentioning here, that heterodyne architecture is less preferred nowadays for multi-standard mobile device; but, still there are a few developments that use this architecture, i.e. as depicted in Figure 2.6 and Figure 2.7. Other sets of literature of receiver systems based on heterodyne can be found in [57-64].

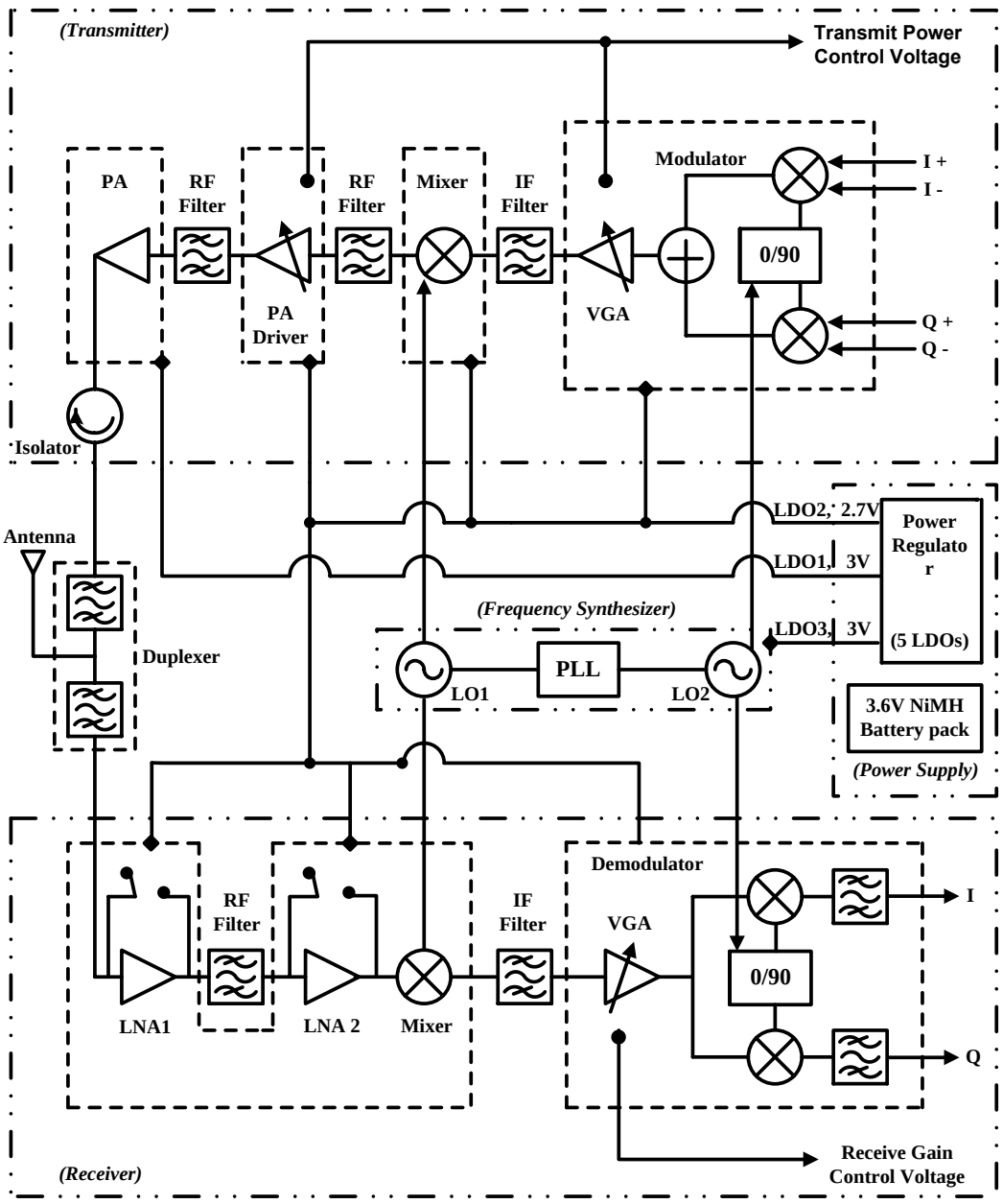

Figure 2.7: Superheterodyne receiver as in [56]

After reviewing the RF receiver architectures that were developed and currently being implemented, it can be concluded that, most of these architectures are limited in terms of standards of mobile communications covered in the design. Also, the implemented RF receiver's architectures are used to cover either single standard or few standards in

parallel form. For that reason, these architectures can be modified by making it reconfigurable to provide multi-standard multi-band capability. For instance, if only GSM system is available at certain place, the architecture should adjust itself to respond to the system. Thus, it is essential to find a better solution, how to produce a mobile device with a compact architecture based on reconfigurable concept to meet the need for multi-standard multi-band system. This, in return could reduce the cost of the system and also provide a system with longer battery life at a very affordable price. The following section will highlight in more details the reconfigurable features which currently being researched and developed around the world.

2.2 Reconfigurable Multi-standard Mobile Terminals

In this research, the term reconfigurable architecture means that the system hardware can adjust itself to serve multi-standard multi-band mobile terminals. Therefore, reconfigurable terminals represents the system that uses multiple ways to reconfigure the available architectures either at system level or at component level, with the objective to provide better performance that is more efficient in cost, area and power consumption. The following sub-section will highlight the development of reconfigurable receiver's architectures and followed by reconfigurable LNAs for multi-standard mobile terminals.

2.2.1 Recent developments of reconfigurable multi-standard system

In the previous section on RF receiver architectures, the concept of multi-standard multi-band systems which cover most of the cellular standards and other wireless standards has been discussed. But the concept of parallel system is no longer suitable to support the current trend for high data rates and global mobility. Thus, RF engineers and researchers around the world have come up with an idea of designing a mobile device that could support as many as possible the cellular and wireless standards in one terminal using the concept of reconfigurability.

Based on the reconfigurability concepts, several systems appears in the literature to support multi-standard terminals that consists of several combinations of cellular and wireless standards such as GSM, UMTS, Bluetooth, GPS, wireless local area network (WLAN), etc. For instance, in Figure 2.9, the reconfigurable architecture combines the advantages of both heterodyne and homodyne architecture that support two standards: UMTS and WLAN. In this architecture, the use of heterodyne provides good rejection between RF and LO port and good selectivity. On the other hand, the use of homodyne or DCR for UMTS system reduces the problem with I/Q imbalance [65-66].

In addition, to demonstrate the concept of reconfigurability being adopted successfully, Figure 2.10 shows another proposal and implementation of reconfigurable receiver architecture and a reconfigurable RF design technique using a switchable passive network. The architecture is targeted to cover WCDMA, 802.11a/b/g WLAN, and WiBro (Wireless Broadband) with a single receiver chain [67].

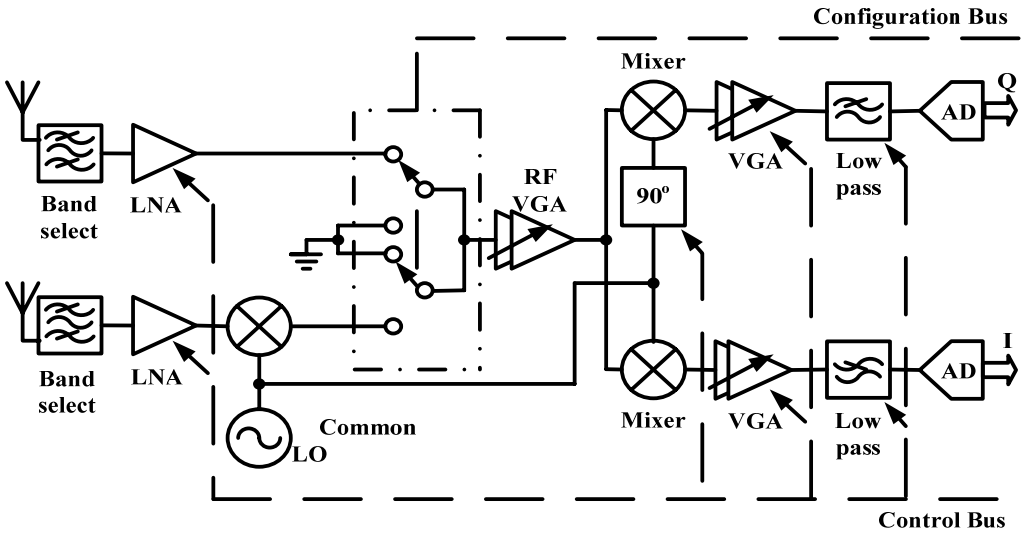

Figure 2.9: Reconfigurable receiver architecture as in [65]

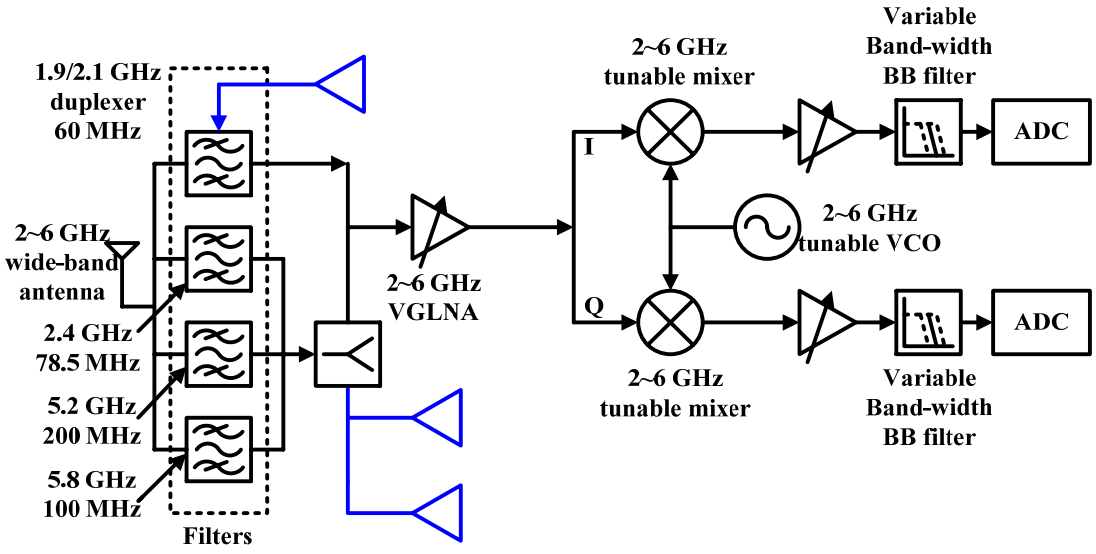

Figure 2.10: 2-6 GHz multi-standard receiver architecture [67]

At this point, it has been shown that the available reconfigurable architectures just cover some standards in one implementation, i.e. as in [65-66]. These designs just cover the

GSM1800 and WCDMA standards for personal mobile communications and WLAN for wireless communication only. Then in [67], it only adds WiBro on top of what have been implemented in [65-66].

The dream then is to design a single system (as introduced by QUALCOMM) which covers almost all of the personal wireless communication standards (GSM and UMTS) and other wireless standards such as GPS and Bluetooth. Also, this new system based on reconfigurable architecture should needs less components (e.g. less inductor), cheaper and less power consumption. The simplest idea is to use one reconfigurable LNA that could be reconfigured to serve multiple standards for GSM and UMTS (i.e. GSM850, GSM900, DCS1800, PCS1900, and UMTS – Band I-VI). This approach will reduce number of required components, leading to a system with less complexity, less area and more importantly less power consumption.

In addition, with all the presented examples and proposed concepts of reconfigurability, so far, there's no one method to be followed by the RF designers to design such reconfigurable terminal for multi-standard system. There are two possible initiatives in the process of developing the reconfigurable terminals for multi-standard systems which are [66]:

(1) Necessity: Dictated by the differences in standards and frequency bands in different geographical regions.

(2) Economically: e.g. development of GSM/UMTS multi-standard terminals that take advantage of superior data rates of UMTS and full coverage of GSM.

In this thesis, these two directions are followed in designing a personal wireless communication unit. Hence, Figure 2.11 shows a proposed multi-standard terminal that uses DCR as the architecture of choice. It employs only one terminal of a reconfigurable LNA (in conjunction with other components that are also made multi-band components i.e. multi-band RF filters, multi-band mixers, etc.), to accommodate multiple bands and standards. This results in a great reduction in the system complexity, and significantly reduces the system power consumption and cost.

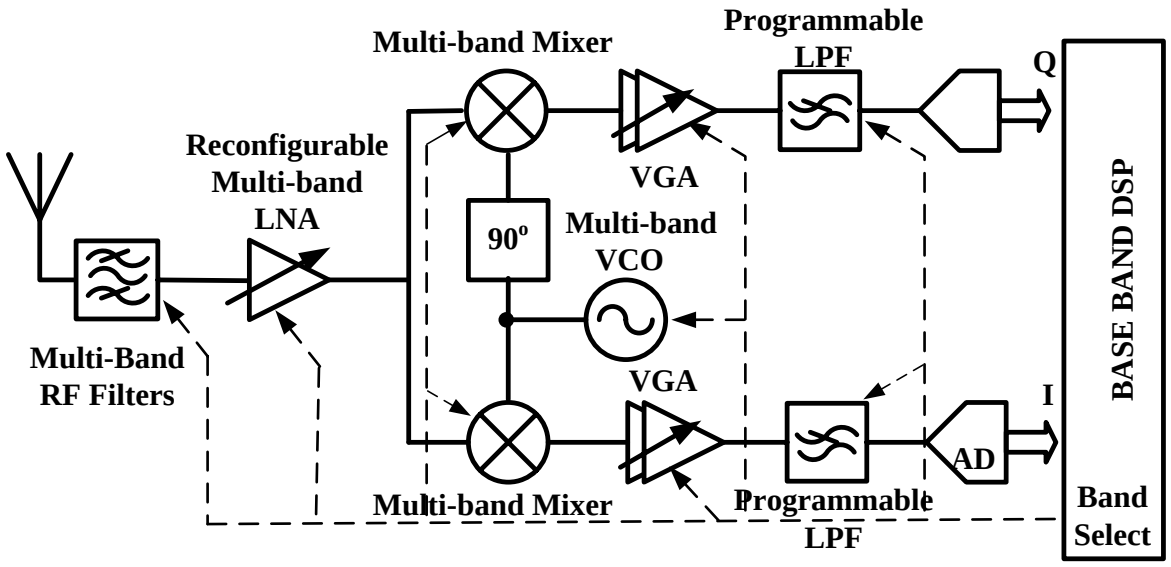

Figure 2.11: Proposed receiver architecture

2.2.2 Recent developments of reconfigurable multi-standard LNA

Recall from the previous section on RF receiver architectures, it tells that the concept of parallel system is no longer suitable to support the current trend for high data rates and global mobility. For that reason, researchers have come up with an idea of designing a mobile device system using the concept of reconfigurability. Despite all the limitations of such technology (i.e. CMOS), different standard requirement, etc., based on this concept, a few systems appear in the literature with different levels, including as many available standards as possible to support the demand for functionality and global mobility.

At components level, for instance, the design of LNA had several approaches and implementations to meet the requirement of multi-standard multi-band system. Therefore, reviewing some of reconfigurable LNA at this time is important. Figure 2.12 shows a new topology of multiband reconfigurable LNA based on positive feedback for a system that cover DCS/UMTS/802.11b-g standards [68]. The feedback loop (reflection from the load to the input) allows three different bands selection of 1.8, 2.1 and 2.4 GHz. Moreover, the use of shunt positive feedback configuration provides enhanced current gain compared with other feedback topologies, thereby improving the overall receiver noise figure. On top of that it uses variable gain and tunable load to meet the different requirement for DCS/UMTS/802.11b-g standards.

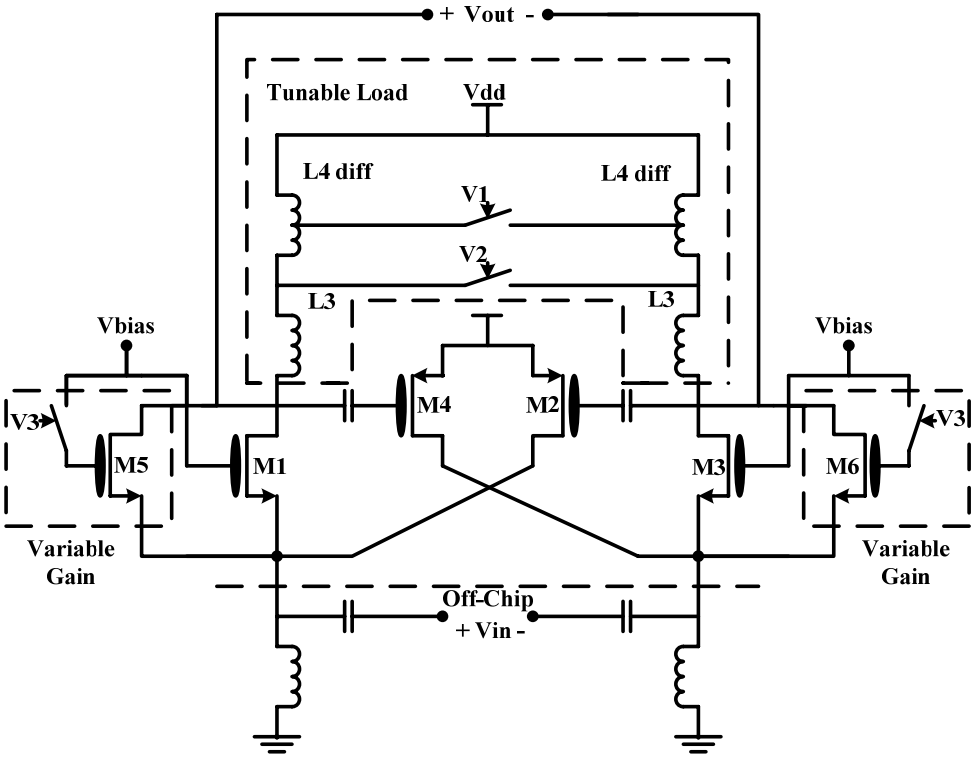

Figure 2.12: Multiband LNA architecture [68]

Another example, Figure 2.13 shows an implementation of LNA based on Bipolar CMOS (BiCMOS) Silicon Germanium (SiGe) technology [69]. The LNA uses cascode topology with inductive emitter-degeneration which offers better trade-off between gain, noise figure, power consumption and linearity. The most area consuming elements, the on-chip inductances are shared between the two involved standards, DCS1800 and WCDMA. The selection of the operating standard is performed through a bias scheme that selects the appropriate current reference, bias circuitry and load resonant frequency. It also uses variable gain (low-gain and high-gain) that can also be selected through the switch implementation which adds a low resistance in parallel with LNA load.

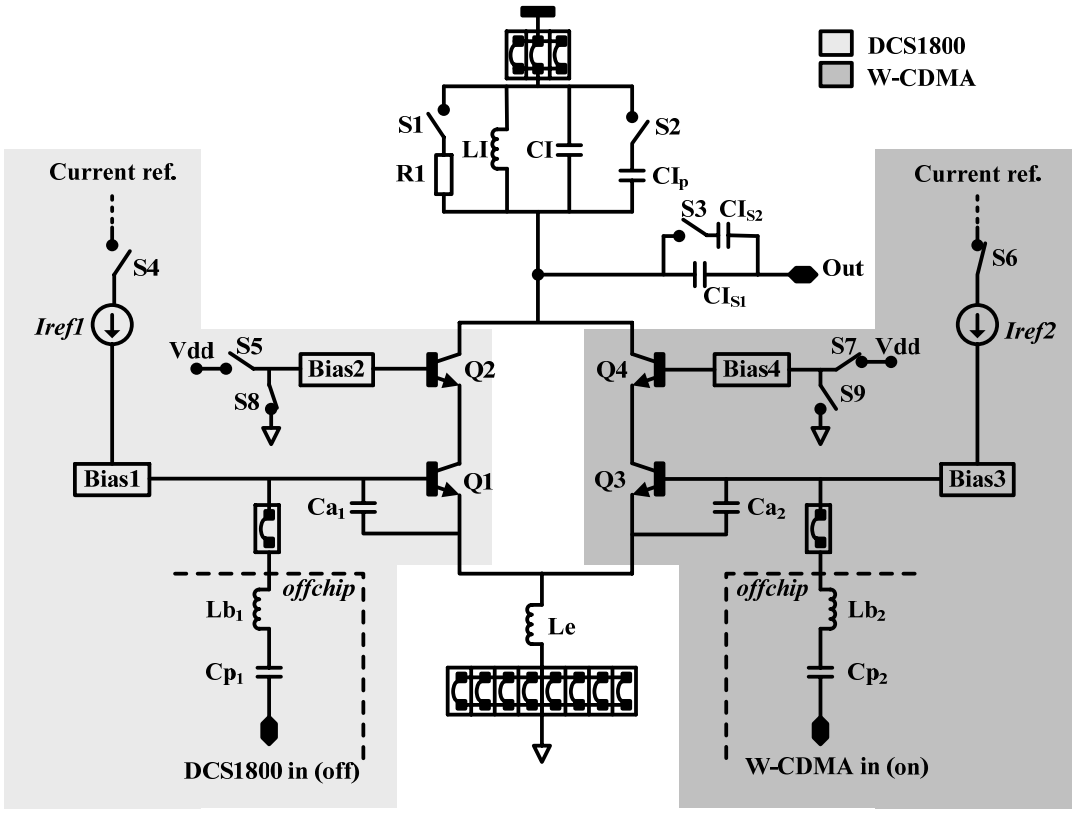

Figure 2.13: Dual-standard LNA as in [69]

Therefore, it is clear that, there are multiple ways to implement a reconfigurable LNA for multi-standard receiver architecture. However, all the above mentioned examples are limited to a few combinations of the personal mobile communication standards (i.e. DCS1800 and WCDMA standards) and other wireless communications standards (i.e. WLAN) as in [65-66]. Meanwhile, in the rest of the literature [70-71], the LNAs are either developed for standards other than mobile communication standards (e.g. [70]) or only a combination of two personal mobile communication standards and wireless standards [71]. For this reason, a new multi-standard multi-band reconfigurable LNA is needed that could cover more standards but in compact mode.

2.3 Conclusion

In this chapter, a review of RF multi-standard receiver systems that include the RF standards, RF receiver architectures, reconfigurable architectures for multi-standard system at the system level and component level (LNA), have been presented. The discussions were based on the relationship between the receiver's specifications and receiver's components specifications (i.e. LNA). Also, the receiver architectures that have been used and currently being used to support those specifications in particular heterodyne and DCR architectures were presented. The discussion was based on the suitability of these architectures for monolithic integration especially when referring to multi-standard systems. Based on these architectures, the development of the receiver systems have been reviewed in detail, in particular the disadvantage and limitations of the current solution for multi-standard system, in specific that utilising parallel system architecture. Also, the concept of reconfigurability as the solution to the above mentioned problem associated with parallel implementation has been discussed.

At this point, it is clear that the design of LNA is facing challenges, despite advancement in sub-micron technologies, and several particular solutions that are available to the designer of the receiver architectures and its components. The designers still have to struggle through trade-offs, technology constrains and increasing requirements (i.e. more standards with more functionality). Consequently, the receiver components, even the best available, still show non-ideal behavior. But this doesn't stop the manufacturers coming up with a system that marginally satisfies the current need for multi-standard

multi-band system with more functionality, which responds to the need for global mobility and high data rates requirements.

Therefore, in order to design a reconfigurable LNA, it is necessary to investigate the available architectures or techniques which could meet the need for multi-standard multi-band mobile communication system. For that reason, the following chapter is presented in such a way that explores the chosen technique in details in form of theories and designs of the multi-standard multi-band LNAs design. From there, the idea to design a reconfigurable LNA was developed. However, only in Chapter 6, the reconfigurable multi-standard multi-band LNA will be discussed in details where Chapters 4 and 5 are allocated for the results of the designed LNAs in Chapter 3.

CHAPTER 3:

LNA THEORIES AND DESIGNS

3.0 Introduction

LNA is considered as one of the most important component or key block in the design of RF receivers as discussed in Chapter 2. It plays a critical role in determining the overall system NF of the receiver. The main function of an LNA is to provide sufficient gain to reduce the noise of subsequent stages (e.g. mixers) while adding as little noise as possible. At the same time, it has to provide good linearity which is typically measured in terms of the IP3. Moreover the need to provide stable 50 Ω input impedance for the termination of an unknown length of transmission line (which delivers RF signals from the antenna to the LNA) put more stringent requirements on the LNA design. Also, it should consume low power, which is considered as another design requirement.

For these reasons, the focus is to provide the best architectures that could adhere to simultaneous requirements which are in general contradictory. For instance, the need for low power is always opposite to the requirement for sufficient gain and good linearity. However, despite of that problem, good designers should always find a way to design such amplifiers that meet all the requirements, off course with some trade-off. Having mentioned that, researchers around the world have investigated LNA techniques

in the frequency band of 850 MHz to 2.1 GHz, which includes most of the world's use of frequencies of the mobile communication standards (GSM and 3G). Techniques such as inductively-degenerated common source (IDCS), common source (CS) with shunt-input resistor, common gate (CG), and shunt-series amplifiers are the most discussed around the world [72]. Among these four techniques, it is known that IDCS is believed to be the preferred architecture for most applications, especially in mobile communication systems [73-74]. Based on IDCS, more techniques have been introduced in the LNA design arena to meet most of the requirements for today's wireless applications.

Therefore, this chapter will discuss the LNA theories and designs. Section 3.1 will highlight the LNA theories based on IDCS topology as it is the core design technique of LNA in this chapter specifically and in this thesis generally. While LNA designs based on IDCS topology is followed in Section 3.2. The conclusion remark is in Section 3.3.

3.1 LNA theories

As stated earlier, LNA is an important block of RF receivers as it represents the first gain stage in the receiver's path. Its main function is to provide enough gain to overcome the noise of the subsequent stages while introducing as little noise as possible to the receiver system. These two tasks are not always easily achieved simultaneously, the main reason being the noise impedance matching and the input impedance matching are not always obtained for the same source impedance. Therefore, the choice of the LNA topology is very important to achieve the expected performance. As introduced in Section 3.1, IDCS cascode is preferred over other

architectures such as CS with shunt-input resistor, common-gate (CG), and shunt-series amplifiers [72]. This is due to the fact that IDCS offers the possibility of achieving the best noise performance of any architecture, as mentioned earlier. Therefore, in the following sub-section, the discussion on the theories of the IDCS technique is presented.

3.1.1 Impedance matching

Impedance matching is important in LNA design because usually the system performance can be strongly affected by the quality of the termination [75]. For example, the frequency response of the antenna's filter that precedes the LNA will be deviated from its normal operation if there are reflections from the LNA back to the filter. The quality of the termination is defined by the reflection coefficient Γ introduced in Appendix–A. An impedance match occurs when the reflection coefficient is equal to zero, and when $Z_S = Z_L$ as in Figure 3.1.

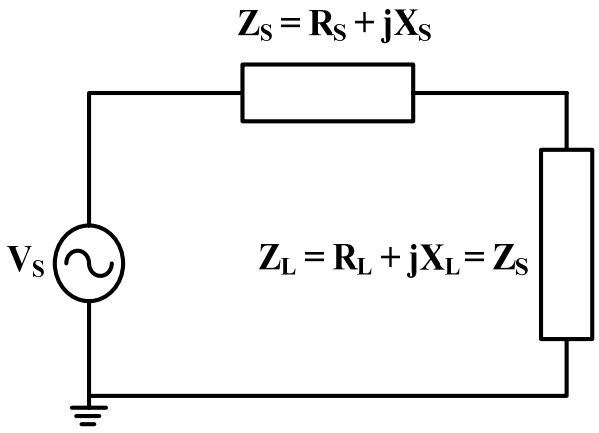

Figure 3.1: Condition for impedance match

Notice that there is a fine distinction between impedance matching and power matching. As stated previously, the condition for impedance matching occurs when the load impedance is equal to the characteristic impedance. In other words, impedance matching is clearly not concerned with the amount of power transferred into the load impedance. On the other hand, for power matching, the condition takes place when the load impedance is the complex conjugate of the characteristic impedance. When the impedances are real, the conditions for power matching and impedance matching are equal.

3.1.1.1 Input impedance match for IDCS technique

It has been explained that, providing an impedance match is important in LNA design. Input impedance matching based on inductive degeneration is shown in Figure 3.2. This type of matching is preferred due to the fact that the matching to the source does not introduce any noise theoretically [72] [75].

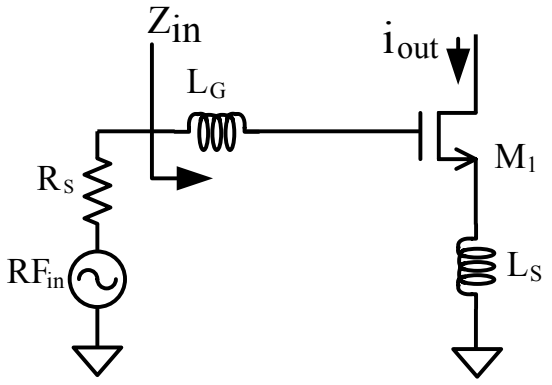

Figure 3.2: Inductive source degeneration

The circuit shown in Figure 3.2 has input impedance as given in (3.1) [72].

$$Z_{in} \approx s\left(L_G+L_S\right)+\frac{g_{m1}L_S}{C_{gs}}+\frac{1}{sC_{gs}} \tag{3.1}$$

where L_G is the gate inductor and L_S is the transistor source inductor and are assumed as ideal inductors. C_{gs} is the gate-source capacitance and g_{m1} is the transconductance of input device M_1

Therefore, to achieve the input match, at resonance, the following condition has to be satisfied:

$$R_S=\frac{g_{m1}L_S}{C_{gs}}=50\ \Omega \tag{3.2}$$

In other words, at resonance frequency ω_o, once L_S is chosen to provide the input match, L_G also can be chosen to make Z_{in} in real term and is equal to (3.2). For L_G, the following equation must hold:

$$\omega_o=\frac{1}{\sqrt{\left(L_G+L_S\right)C_{gs}}} \tag{3.3}$$

3.1.2 Noise sources in CMOS

It is better to highlight some of the important theories behind the design of the LNA. The following sub-section gives the analysis of the noise sources of the CMOS device. The two most important noise sources of the CMOS transistor are presented [25] [72].

3.1.2.1 Thermal noise model for IDCS technique

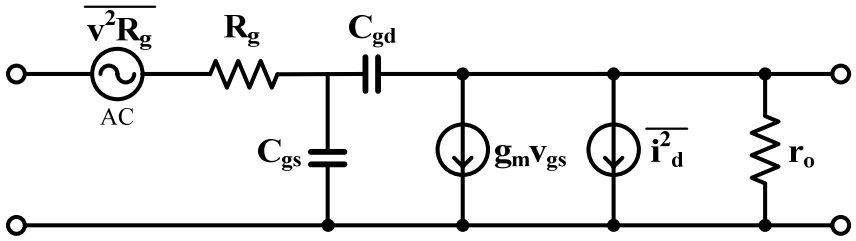

Figure 3.3: Standard CMOS noise model representing thermal noise [25]

Thermal noise is commonly modelled as a current source across the drain and the source in shunt with the transconductor of the transistor (Figure 3.3). It has a power spectral density given by [25]:

$$\frac{\overline{i_d^2}}{\Delta f} = 4kT\gamma g_{d0} \tag{3.4}$$

where g_{d0} is the device zero-bias drain conductance, γ is a bias-dependent factor and Δf is the noise bandwidth. The basic noise figure of the LNA can be determined by analysing the circuit in Figure 3.4.

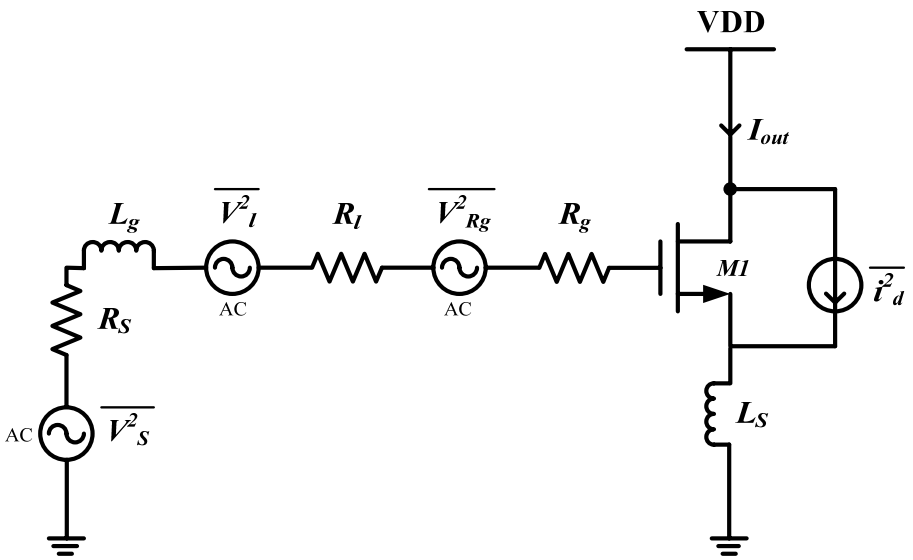

Figure 3.4: IDCS circuit for input stage noise calculations [25]

In Figure 3.4, R_l is the series resistance of L_g, and R_g is the gate resistance of the NMOS. The subsequent stages contribution to the noise figure is neglected and this is acceptable if the first stage provides sufficient gain. C_{gd} is also neglected, as the topology is of a cascaded nature and therefore this approximation is accepted. To evaluate the output noise when the amplifier is driven by a 50 Ω source, the transconductance of the input stage needs to be evaluated first. Therefore at resonance [25],

$$G_m = g_{m1} Q_{in} = \frac{g_{m1}}{\omega_o C_{gs}\left(R_S + \omega_T L_S\right)} = \frac{\omega_T}{\omega_o R_S\left(1 + \frac{\omega_T L_S}{R_S}\right)} \tag{3.5}$$

where Q_{in} is the effective Q of the amplifier input circuit, g_{m1} is transistor transconductance, ω_o is the operating angular frequency and ω_T is the transition angular frequency.

It is well-known that the noise factor definition is given by [25] [72],

$$F = \frac{Total\ output\ noise\ power}{Total\ output\ noise\ due\ to\ the\ input\ source} \tag{3.6}$$

Therefore, using (3.5), the output noise power density due to 50 Ω source is given as follow:

$$S_{out,source}(\omega_o) = S_{source}(\omega_o) G_{m,eff}^2 = \frac{4kT\omega_T^2}{\omega_o^2 R_S \left(1 + \frac{\omega_T L_S}{R_S}\right)^2} \tag{3.7}$$

Similarly, to obtain the output noise power density due to gate resistance and series resistance, R_l and R_g, the following expression is given:

$$S_{out,R_l R_g}(\omega_o) = \frac{4kT\left(R_l + R_g\right)\omega_T^2}{\omega_o^2 R_S^2 \left(1 + \frac{\omega_T L_S}{R_S}\right)^2} \tag{3.8}$$

Recall equation (3.4), the derivation of the output noise due to this channel current noise is given as:

$$S_{out,i_d}(\omega_o) = \frac{\frac{\overline{i_d^2}}{\Delta f}}{\omega_o^2 R_S \left(1 + \frac{\omega_T L_S}{R_S}\right)^2} = \frac{4kT\gamma g_{d0}}{\omega_o^2 R_S \left(1 + \frac{\omega_T L_S}{R_S}\right)^2} \tag{3.9}$$

Therefore, to obtain the noise factor (F) for IDCS topology of the circuit as in Figure 3.4, equation (3.6) is used with all the expression in of (3.7) – (3.9),

$$F = \frac{S_{out,source}(\omega_o) + S_{out,R_l \text{ and } R_g}(\omega_o) + S_{out,i_d}(\omega_o)}{S_{out,source}(\omega_o)} \quad (3.10)$$

which then yield the following equation [25],

$$F = 1 + \frac{R_l}{R_S} + \frac{R_g}{R_S} + \gamma g_{d0} R_S \left(\frac{\omega_o}{\omega_T} \right)^2 \quad (3.11)$$

3.1.2.2 Induced Gate Noise Model for IDCS Technique

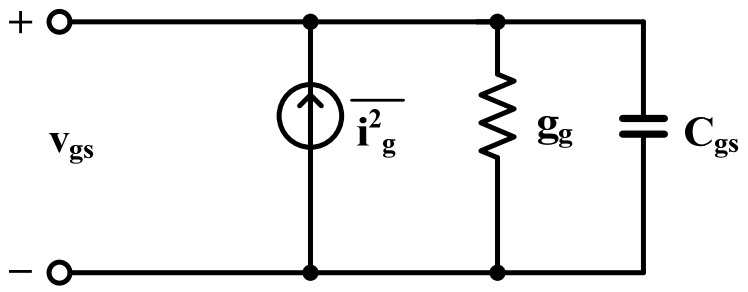

Figure 3.5: Standard CMOS noise model representing induced gate noise [25]

Induced gate noise is a high frequency noise source that is caused by the non-quasi static effects influencing the power spectral density of the drain current (more details about the non-quasi static effect is shown in Appendix–B) [75]. Gate noise is explained by van der Ziel in [76]. This noise source is coming from the thermal noise in the

channel that coupled through the oxide capacitance (due to the capacitive coupling) to the gate terminal, causing a gate noise current to flow. This noise source is normally not included in standard noise analysis because at low frequencies it is negligible. However, this noise source can be dominant at RF frequencies. Its circuit model is shown in Figure 3.5, and its power spectral density is given in the equation 3.12 as follow [25]:

$$\frac{\overline{i_g^2}}{\Delta f} = 4kT\delta g_g \tag{3.12}$$

where,

$$g_g = \frac{\omega^2 C_{gs}^2}{5 g_{d0}} \tag{3.13}$$

and, δ is the coefficient for gate noise. The gate noise is partially correlated with the drain noise. The correlation coefficient is given by,

$$c = \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g^2}\,\overline{i_d^2}}} \approx 0.395j \tag{3.14}$$

This value c is valid for long-channel as well as for short-channel regime as stated in [77]. Based on this coefficient, gate noise can be re-written as

$$\frac{\overline{i_g^2}}{\Delta f} = 4kT\delta g_g \left(1 - |c|^2\right) + 4kT\delta g_g |c|^2 \tag{3.15}$$

The first term of the expression represents the uncorrelated noise and the second term is representing correlated noise.

To continue with the process of getting the more precise analysis of the noise of the circuit, let take a look at Figure 3.6.

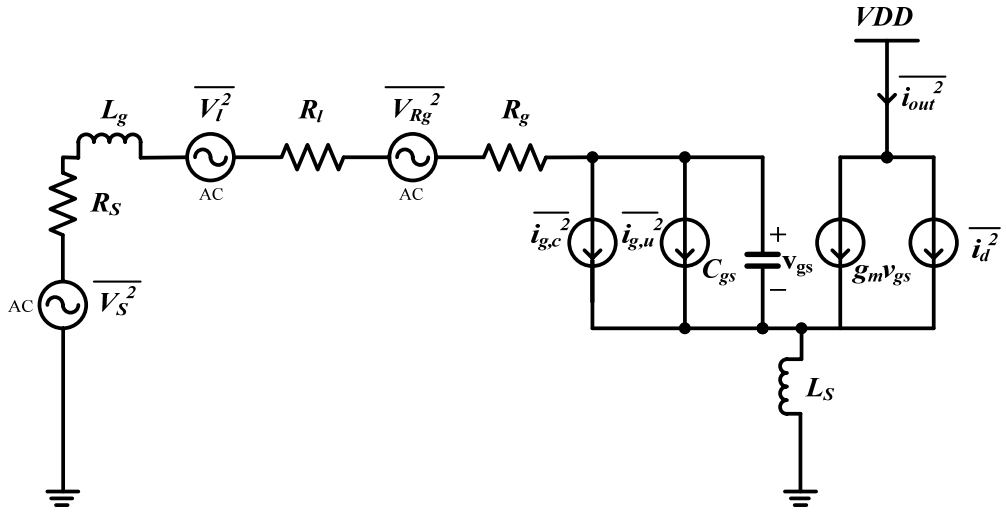

Figure 3.6: Revised IDCS small-signal model for input stage noise calculations [25]

Looking at the circuit model, the gate noise has been categorised into two parts. First, $\overline{i_{g,c}^2}$ is representing the correlated gate noise and $\overline{i_{g,u}^2}$ represents the uncorrelated gate noise. For that reason, the correlated gate noise is given by [25],

$$S_{out,id,\,ig,\,c}(\omega_o) = \kappa S_{out,id}(\omega_o) = \frac{4kT\gamma\kappa g_{d0}}{\left(1+\frac{\omega_T L_S}{R_S}\right)^2} \tag{3.16}$$

where

$$\kappa = \frac{\delta\alpha^2}{5\gamma}|c|^2 + \left[1 + |c|\sqrt{\frac{\delta\alpha^2}{5\gamma}}\right]^2 \tag{3.17}$$

and

$$\alpha = \frac{g_m}{g_{d0}} \tag{3.18}$$

On the other hand, the uncorrelated gate noise is given as,

$$S_{out,id,\,ig,\,u}(\omega_o) = \xi S_{out,id}(\omega_o) = \frac{4kT\gamma\xi g_{d0}}{\left(1 + \frac{\omega_T L_S}{R_S}\right)^2} \tag{3.19}$$

where

$$\xi = \frac{\delta\alpha^2}{5\gamma}\left(1 + |c|^2\right)\left(1 + Q_L^2\right) \tag{3.20}$$

and

$$Q_L = \frac{\omega_o\left(L_G + L_S\right)}{R_S} = \frac{1}{\omega_o R_S C_{gs}} \tag{3.21}$$

Since all the noise terms of the transistor M_1 are proportional to $S_{out,id,}(\omega_o)$, it is very important to re-define the noise of M_1 to be [25],

$$S_{out,M1}(\omega_o) = \chi S_{out,id}(\omega_o) = \frac{4kT\gamma\chi g_{d0}}{\left(1+\frac{\omega_T L_S}{R_S}\right)^2} \tag{3.22}$$

where

$$\chi = \kappa + \xi = 1 + 2|c|\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}\left(1+Q_L^2\right) \tag{3.23}$$

With the observation of (3.22) and (3.23), it shows that induced gate noise alters the noise contribution of the device which is proportional to χ. Therefore, for IDCS topology, the following equation describe mathematically the noise factor [25] [72]

$$F = 1 + \frac{R_l}{R_S} + \frac{R_g}{R_S} + \gamma\chi g_{d0} R_S \left(\frac{\omega_o}{\omega_T}\right)^2 \tag{3.24}$$

which also after factoring out Q_L from the equation, F can be re-written as below

$$F = 1 + \frac{R_l}{R_S} + \frac{R_g}{R_S} + \frac{\gamma}{\alpha}\frac{\chi}{Q_L}\left(\frac{\omega_o}{\omega_T}\right) \tag{3.25}$$

This equation of the noise factor shows that there exist a minimum noise factor for a given ω_T as it can be observed from the expression, that F is proportional and

inversely proportional to Q_L. Also, it is worth to notice here that, this noise factor is a noise factor derived for power-constrained noise optimisation [72].

3.1.3 S-parameters

Typically, at low frequencies, two common representations, the impedance matrix (Z parameters) and the admittance matrix (Y parameters), are particularly useful to measure the impedances and the admittances of the two-port network. This is because they can be measured by applying either a test current or test voltage to the input port and connecting either the output port as a short or open circuit, depending on the definition. However, at RF and microwave frequencies, Z and Y parameters become very difficult to measure due to the need for broadband short and open circuits [78]. Furthermore, an active two-port network might oscillate if one of its ports was short or open circuited. Hence, a different representation of the two-port network is needed at RF and microwave frequencies. The representation used is the scattering, or s-parameters. In short, s-parameters, as important specifications of the LNA, are expressed in equations (3.26) to (3.29). More details on how these equations were obtained are presented in Appendix–D.

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_{2=0}} \tag{3.26}$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_{1=0}} \tag{3.27}$$

$$S_{21} = \left.\frac{b_1}{a_1}\right|_{a_{2=0}} \tag{3.28}$$

$$S_{22} = \left.\frac{b_1}{a_2}\right|_{a_{1=0}} \tag{3.29}$$

where S_{11} is known as input return loss, S_{12} known as reverse isolation, S_{21} as power gain, and S_{22} as output return loss.

3.1.4 Linearity

In this section, another parameter for LNA, linearity, is presented. Linearity is a key parameter of the LNA because it specifies how much LNA can maintain linear operation even in the presence of large input signals. The measurement of linearity are usually done by using two parameters, IIP_3 and $P1dB$. The following sub-section briefly introduces these parameters. A more details explanation can be found in Appendix–E.

3.1.4.1 IIP3

In a two-port network, the measurement of the amount of third order non-linearity is called input third order intercept point. Mathematically, IIP_3 is obtained as in (3.30).

$$IIP_3 = \sqrt{\frac{4}{3}\left|\frac{A_1}{A_3}\right|} \tag{3.30}$$

where A_1 and A_3 are constants and defined in Appendix–E.

3.1.4.2 P1dB

$P1dB$ is a measure of the power of the input signal such that it causes the third order non-linearity to decrease the linear gain (defined in AE.3) by 1 dB. Mathematically, $P1dB$ is obtained as in (3.31) and eventually yield (3.32) as follows

$$20\ log\left(1+\frac{3A_3}{4A_1}S_1^2\right)=-1\ dB \tag{3.31}$$

where S_1 , A_1 and A_3 are defined in Appendix–E.

Then, after solving for S_1 (refer to Appendix–E), $P1dB$ is obtained as follows

$$P1dB=0.33\sqrt{\frac{4}{3}\left|\frac{A_1}{A_3}\right|} \tag{3.32}$$

3.2 Multi-standard multi-band LNA

3.2.1 Multi-standard LNA

The main design goals of an LNA is to achieve low noise figure (NF), sufficient gain (depending on the receiver's application), low power consumption, good linearity

(especially in a receiver for 3G application which impose stringent linearity requirement), and finally good s-parameters performance to implement the required matching and reverse isolation. Hence, the choice of the LNA topology is very important to achieve the expected performance. Here, the design of the LNA based on the IDCS is presented. As discussed earlier, this topology is believed to be the best in providing low noise and low power consumption with sufficient gain and input matching over the required bandwidth whether it is narrowband or wide band. Typically, IDCS is used to design the narrowband LNA for particular standard i.e. GSM900 or DCS1800 which has a bandwidth of less than 100 MHz. However, this topology has been improved to work in a broader bandwidth range from several hundreds MHz up to few GHz as shown in [79-81].

Referring back to Chapter 2, it is worth to re-mention here that over the past few years, RF engineers have tried to produce mobile devices that meet the current demands for multi-standard multi-band system with more functionality in the wireless mobile communication field. The focus on the design of a compact CMOS RF multi-band system that could satisfy the need for multi-standard wireless mobile communication systems was then established. However, current multi-band systems support parallel architecture on a single-chip to suffice the multi-standard systems such as GSM and 3G. Specifically, industries use parallel components such as Radio Frequency (RF) filters and LNA at the front-end receiver of the mobile devices to support these standards [10-12]. This implementation as mentioned before is very area inefficient, costly and consumes relatively high power. Referring to work presented in [40], it

proposed a single multi-standard LNA in combination with several RF filters at the front-end circuit to meet the need for multiple standards devices. The proposed LNA architecture reduces the complexity, power consumption and components used in the current solution.

Even so, the design of such LNA for a multi-standard system is not easy due to stringent requirements for different standards i.e. gain requirement for GSM (23 dB) is tougher than 3G (18 dB). The requirement for linearity is much more difficult to achieve for the 3G standard (0 dBm) compared to GSM (-5 dBm) [40]. In addition, the requirement for simultaneous low noise and low power design is also hard to achieve. Hence, a better design technique, such as inductively-degenerated with improvement for multi-standard multi-band LNA circuit is essential. Here, modification of the available architectures, in particular IDCS by making it suitable for multi-standard multi-band system will performed.

3.2.2 Multi-standard LNA for wide band receiver system

To accommodate such requirement for a multi-standard multi-band system, LNA with a wide band capability is considered. For instance, multi-standard system comprises GSM and 3G bands in two regimes format i.e. 800-1000 MHz (200 MHz bandwidth) and 1800-2200 MHz (400 MHz bandwidth) compared to a single standard implementation (i.e. 900 MHz or 1800 MHz band) should be implemented. For that reason, one might consider designing an amplifier with the ability to capture most of the standards

simultaneously, or one standard in one particular time depending on the availability of the standards using a wide band approach. With a wide band LNA implementation, a single device (i.e. LNA or mixer) to cover each single standard is no longer needed. This approach achieves a reduction in component count, cost and die area.

But, in the design and implementation of wide band LNA, some important issues have to be discussed. First, compared to narrow band approach, wide band initiative is however, could suffers from the effect of out-of-band signal interferers or blockers that can mix with the phase noise (in receiver system) and increase the amount of noise in the desired channel. Fortunately, (as the proposed receiver architecture uses multi-band RF filters), the benefit is that the out-of-band blockers is attenuated by the RF filters prior to the LNA input. This means that, although the LNA is acting as a wide band device, the signal it captures is narrow band. In other words, any signals that passes through the RF filters, at any frequency i.e. DCS1800 at 1.8-GHz or UMTS850 at 850-MHz are detectable by the proposed wide band LNAs. Thus, the issue of the effect of out-of-band interferers is insignificant. Hence, with the proposed receiver architecture as depicted in Figure 2.11 (Chapter 2), the requirement for the linearity should remain the same for the LNA (as the RF filters at the front-end are already attenuating the out-of-band interferers). It is worth mentioning here that even though the proposed LNA designed needed 10 RF filters to support 10 standards, but in reality it doesn't have to be that many. This is due to the fact that there are an overlap frequency bands (i.e. UMTS Band I and IV and UMTS Band V and VI). For that reason, the same RF filter could be reused by means of reconfiguration (if necessary – has to be

investigated, as it is beyond the scope of this thesis) which lead to less filters count. Moreover, looking back at Tables 2.1 and 2.2, with a simple observation, the needed RF filters to support the proposed receiver architecture (Figure 2.13) is only 6 instead of 10. In addition, if the RF filters used are to be made tunable, it could simply reduce the filters count even more as suggested in [68] as it proposed the use of tunable SAW filter prior to the multi-band LNA.

Second, the issues related to the wide band are the harmonic distortion and sub-harmonic-mixing. For instance, let say the receiver receives the signals from 0.7 GHz to 2.5 GHz; a strong signal at 0.7 GHz will create a third-order harmonic distortion at 2.1 GHz, and then corrupts any signals at that frequency. Likewise, if the wanted signal and LO are at 0.7 GHz, a strong signal at 2.1 GHz will sub-harmonically mix with $3F_{LO}$ which will potentially corrupts the wanted signal.

Having discussed those issues, it is clear that the design of the wide band device has to be done carefully. Therefore, for these specific reasons (as for this thesis's concern), instead of designing one single wide band LNA to cover most of the GSM and 3G standards for GSM850 to UMTS2100, two LNAs with wider bandwidths to cover two different bands in two regimes format i.e. 800-1000 MHz (200 MHz bandwidth) and 1800-2200 MHz (400 MHz bandwidth) as mentioned earlier are proposed. This could resolve the problems associated with the wide band design.

3.2.3 Multi-standard multi-band LNA designs using wide band approach

Referring to the latest literature, it is found that based on IDCS, the design for wide band LNAs have been introduced [80-84]. These designs used several approaches to design such LNA that produce a wide bandwidth circuit based on IDCS technique. These designs also prove that the claim of IDCS technique is only suitable for narrow band LNA is rather not true. Unfortunately, as far as the author's concern, all the designed LNAs described in the literature were not specifically designed for personal mobile communication but for ultra wide band (UWB) communications or not for specific applications range from few MHz to several GHz.

Therefore, the designs of several LNAs based on the IDCS topology with wide band approach using different optimisation techniques are to be presented. The designs have been developed using two CMOS technologies, 0.25 μm and 0.18 μm. The design kits were supplied by the university research group of North Carolina State University (NCSU) and from Silterra Malaysia Sdn Bhd (a semiconductor wafer foundry). The LNAs were designed for carrier frequency standards from 1800 to 2200 MHz (frequency center at 2 GHz) and divided into two categories. One is designed and implemented with output buffer, and the other one with no output buffer for comparison purpose. On the other hand, for carrier frequencies from 800 to 1000 MHz (frequency center at 900 MHz), one LNA has been designed with no output buffer. These LNAs were first designed separately to demonstrate the feasibility of the technique used which is IDCS before been combined as a single reconfigurable LNA (discussion is in Chapter 6.0).

They were designed to cover the most of the standards currently used for mobile communication ranging from 800 to 2200 MHz. This range is covering 10 standards for GSM and 3G (refer to Tables 2.1 and 2.2).

It is worth to mention here that the design kit obtained from NCSU consist of the real CMOS technology files for the transistors and not for the passive components (such as capacitors and inductors). Therefore, the design based on NCSU design kit is only optimised using ideal passive components. On the contrary, the Silterra design kit is supplied with realistic technology files and libraries for both transistors and passive components. Thus, in this thesis, especially in this chapter and in the following chapters, the real design implementation starts from schematic design to fabrication and ends with test and measurement are presented.

The following section will highlight the designs of the LNAs mentioned above in details. (Since all the designs involved or presented in this thesis were designed for wider bandwidth as compared to narrow bandwidth application [32], it is worth mentioning here that all the designs will be named as wide band LNA i.e. wide band LNA1 etc. for the purpose of this discussion). The wide band LNAs were designed as a single-ended LNA based on an IDCS technique. In addition, the power-constrained noise figure optimisation was used in order to achieve low power and low noise with sufficient wide input-matching bandwidth [25] [72].

3.3 Multi-standard multi-band LNA designs

3.3.1 Multi-standard multi-band LNA design flow

Initially, the design starts by investigating and finding the transistor width, finger number and operating point, which have to be defined based on simulations for a given power consumption. Noise parameters such as described in Section 3.1.2, which depends on transistor width and supply current result from these investigations. Next, linearity considerations which also depend on the transistor size etc. should finish the design. Therefore, an optimum transistor size could be obtained based on these parameters.

Basically, the following design flow was used in all the LNA designs:

- Design LC tank for wanted frequency.
- Calculate the pad capacitance and take into account the wiring parasitic.
- Make transistors of the first stage and second stage (i.e. M_1 and M_2) equal to each other, as a first approximation. Additionally choose the proper number of fingers for the transistors.
- Knowing pad capacitance, find such a transistor width W that together with L_S give the wanted real input impedance part.
- Choose the L_G inductor to make full input matching.
- Choose the proper biasing value and check current consumption.
- Make the output matching, a properly chosen series blocking capacitor together with a pad are enough.

- Check the gain of the amplifier and bandwidth; change the LC tank values if needed.
- Change L_S if needed.
- Simulate nonlinearities. P1dB is improved by larger transistor, while larger V_{od} improves small signal nonlinearity (IIP3).
- Change the size of the second transistor if needed, taking into account gain, noise and linearity.
- If needed, extra passive components at the input and output might be considered for optimisation.
- The design is finished.

Definitely, as in most engineering problems, an experience based on skill and intuitions are useful for a successful design. The design flow presented here has been used for the design of multi-standard multi-band LNA for GSM and 3G mobile systems as will be presented in the following sub-sections.

3.3.2 Multi-standard multi-band LNA designs – 2 GHz with buffer

3.3.2.1 LNA1

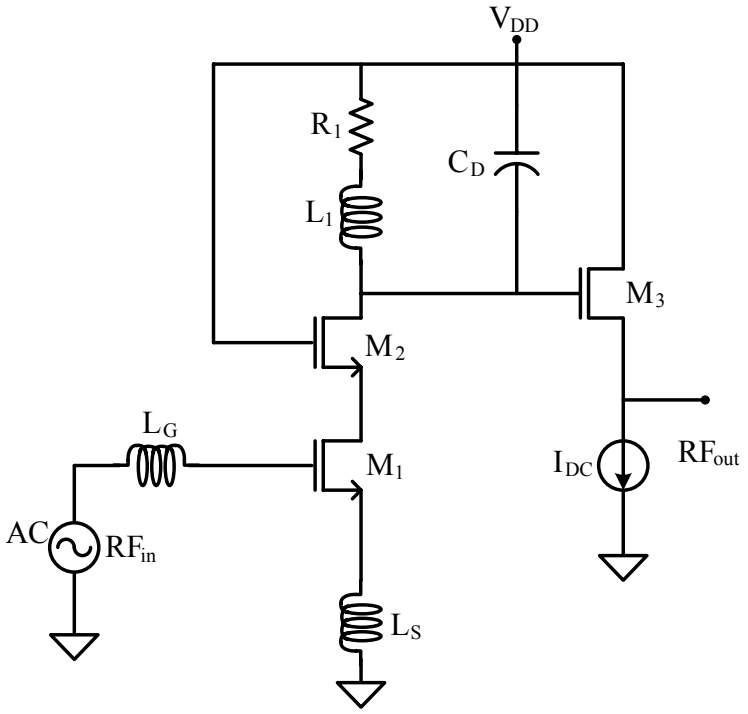

Figure 3.7: Wide band IDCS LNA1 [85]

Figure 3.7 presents the schematic diagram of wide band IDCS LNA1 targeted to cover carrier frequency from 1800 to 2200 MHz. This range of frequencies includes the GSM standards (DCS1800 and PCS1900) and 3G standards (Band I-IV) [2] [7]. Thus, to accommodate such a frequency range from 1800 to 2200 MHz, a new frequency centre of 2 GHz was chosen. This is because it is defined as the geometric mean of the band-edge frequencies of, i.e., 1800 and 2200 MHz. The input-matching bandwidth Δf i.e., the frequency range that satisfies $20 \log |S_{11}| \leq -10\ dB$ was selected to be 400 MHz. According to (3.1), S_{11} can be expressed as [79] [85]

$$S_{11}=\frac{Z_{in}-R_S}{Z_{in}+R_S}=\frac{s^2+\omega_o^2}{s^2+Bs+\omega_o^2}=\frac{s^2+\omega_o^2}{s^2+\frac{\omega_o s}{Q}+\omega_o^2} \tag{3.33}$$

in which

$$\omega_o^2=\frac{1}{C_{gs}(L_G+L_S)} \tag{3.34}$$

$$B\equiv 2\times\frac{g_{m1}L_S}{C_{gs1}\times(L_G+L_S)}\approx\frac{100}{(L_G+L_S)} \tag{3.35}$$

$$Q=\frac{\omega_o}{2R_S}\left(L_G+L_S\right) \tag{3.36}$$

where B is the bandwidth, and Q is the quality factor of the input circuit and is proportional to Q_L in (3.21).

Then, by substituting (3.33) into $20\ log\ |S_{11}|\le -10\ dB$, the following expressions are obtained for ω [79].

$$\frac{-B+\sqrt{B^2+36\omega_o^2}}{6}\le\omega\le\frac{B+\sqrt{B^2+36\omega_o^2}}{6} \tag{3.37}$$

$$\Delta f = \frac{\Delta\omega}{2\pi} = \frac{B}{2\pi} \approx \frac{50}{3\pi\left(L_G + L_S\right)} \tag{3.38}$$

where Δf is the corresponding matching bandwidth.

Based on (3.36) and (3.38), the design equation with normalized matching bandwidth $\Delta f / f_o$ of CMOS cascode LNAs, for the upper limit of the total inductance of the inductors used at the input transistor, can be obtained as follows:

$$\frac{\Delta f}{f_o} = \frac{1}{3Q} \tag{3.39}$$

For the gain, the following equations were modified to suit the design based on [79],

$$\begin{aligned} S_{21} &= 2 \times \frac{v_{out}}{v_{in}} \\ &= \frac{-2g_{m1}\omega_o^2}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2} \times \frac{1}{1 + \frac{s}{\omega_{M2}}} \times \frac{R_1\omega_{o1}^2 + sL_1\omega_{o1}^2}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2} \\ &\approx \frac{-2g_{m1}\omega_o^2}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2} \times \frac{R_1\omega_{o1}^2 + sL_1\omega_{o1}^2}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2} \\ &\equiv \frac{-2g_{m1}\omega_o^2}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2} \times Z_L(s) \end{aligned}$$

$$S_{21} \equiv G_{m21}(s) \times Z_L(s) \tag{3.40}$$

where, $\omega_{M2} \equiv g_{m2}/C_{gs2}$, $\omega_{o1}^2 \equiv 1/L(C_1 + C_{gs3})$ and $Q \equiv (\omega_o L)/r$, while $G_{m21}(s)$ is the transconductance gain if the input voltage adopts the input terminal voltage (i.e. $V_{in}/2$).

Notice that, in this implementation, optimisation has been made to satisfy the requirement for the multi-standard multi-band LNA by introducing the shunt-peaking inductor at the load tank. Shunt peaking is the bandwidth extension technique in which an inductor L_1 is connected in series with the load resistor R_1, that shunts the output capacitor C_D . Treating the transistor as a small-signal dependent current source, $I_{in} = g_m V_{in}$, the gain is simply the product of g_m and $Z(s)$ [85-87]. For the shunt-peaked network:

$$Z(s) = \frac{v_{out}}{i_{in}} = \frac{1}{sC_D} \left\| (R_1 + sL_1) = \frac{R_1 + sL_1}{1 + sR_1 C_D + s^2 L_1 C_D} \right. \tag{3.41}$$

The inductor introduces a zero in $Z(s)$ which increases the impedance with frequency, and compensates for the decreasing impedance of C_D , therefore extends the -3 dB bandwidth.

With respect to input matching and gain of the LNA, it basically follows the theory highlighted by [79] and follows (3.33) to (3.40) which set the lower and upper limit of the total inductance of the inductors connected to the input transistor.

To determine the NF, based on (3.25) the following equation is used [88]

$$NF = 10\log[F] = 10\log\left[1 + \frac{R_l}{R_S} + \frac{R_g}{R_S} + \frac{\gamma}{\alpha}\frac{\chi}{Q_L}\left(\frac{\omega_o}{\omega_T}\right)\right] \tag{3.42}$$

For the width of the transistor M_1, the following equation is given [72] [79]

$$\begin{aligned} W_{opt} &= 1.5(\omega_o L C_{ox} R_s Q_{in,opt,P_D})^{-1} \\ &\approx \frac{1}{3\omega L C_{ox} R_S} \end{aligned} \tag{3.43}$$

where W_{opt} is the optimum width of M_1, L is the effective length of M_1 transistor, C_{ox} is the oxide capacitance and Q_{in} is the input circuit quality factor.

Accordingly, to attain a low NF over the chosen bandwidth based on the theory introduced, the size of transistor M_1 and the inductances of L_G and L_S are set. Therefore, the cascode transistors M_1 with M_2, L_G and L_S connected as in Figure 3.7 set the input impedance and noise-matching simultaneously. L_1, R_1, and C_D function

as tuned load and M_3 act as a buffer. Table 3.1 shows the corresponding component values used for LNA1. The simulation was carried out using Cadence design suite.

Table 3.1: Component values for LNA1

Case	Condition
Freq.	2 GHz
M_1	334 μm
M_2	315 μm
L	0.24 μm
C_{ox}	K ε_{ox}/t_{ox} = 5.95 $fF/\mu m^2$
L_1	2.45 nH
R_1	3.5 Ω
L_G	8 nH
L_S	0.8 nH
C_D	2.1 pF

3.3.2.2 LNA2

For LNA2, Figure 3.8 presents the schematic diagram of wide band IDCS LNA2 targeted to cover carrier frequency from 1800 to 2200 MHz. The difference between LNA1 and LNA2 can be seen at the input tank. In this design, C_{ex} was used to give extra freedom at the input tank for the input matching. Therefore, for this circuit, (3.1) and (3.2) can be re-written as follows [88]:

$$Z_{in} \approx s\left(L_G + L_S\right) + \frac{g_{m1}L_S}{C_{gg1} + C_{ex}} + \frac{1}{s\left(C_{gg1} + C_{ex}\right)} \tag{3.44}$$

$$R_S = \frac{g_{m1}L_S}{C_{gg1} + C_{ex}} = 50\ \Omega \tag{3.45}$$

where g_{m1}, $C_{gg1} = C_{gs1} + C_{gd1} + C_{gb1}$, C_{ex}, L_G and L_S are the transconductance, total gate capacitance, external gate source capacitance, and gate and source-degenerative inductors, respectively. The total gate capacitance is the summation of gate-source, gate-drain and gate-bulk capacitances, respectively.

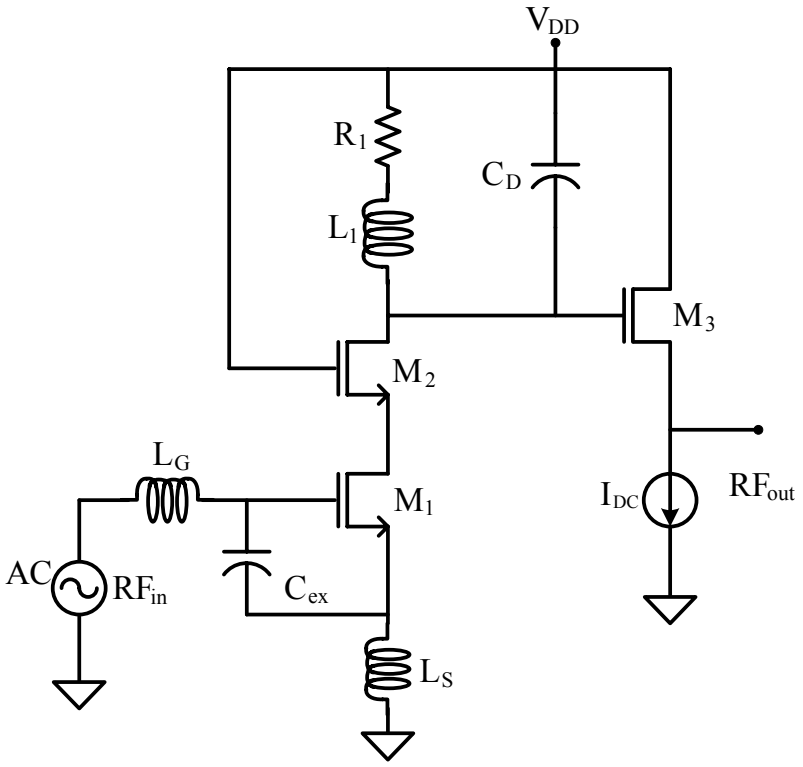

Figure 3.8: Wide band IDCS LNA2 [88]

Apart from (3.44) and (3.45), the previous expressions used to determine the specifications for LNA1 is still applicable for LNA2. Table 3.2 shows the corresponding components values used for the design of LNA2. Notice also, in this design, two

simulations have been done named as pre-layout or schematic simulation and post-layout simulation compared to LNA1 which is only pre-layout simulation was implemented. To verify the validity of circuit design, the layout has been implemented using 0.18 μm technology by using Cadence Design Suite while Calibre tools from Mentor Graphics were utilised to obtain post-layout design rule check (drc), layout versus schematic (lvs) and parasitic extraction (pex). Figure 3.9 shows the layout of the wideband LNA2. This layout has been submitted for fabrication. Notice that for the L_S, three inductors have been used in parallel to realise the 0.55 nH. This is due to the smallest available inductor value from the foundry is 1.65 nH (see Appendix–C for the value of the inductors used for this design) and they were used just for the purpose of proof-of-concept. Also, filtering capacitors were placed at the VDD and the biasing points. These capacitors will eliminate any RF positive feedback to the input of the common-gate transistor.

Table 3.2: Component values for LNA2

Case	Condition
Freq.	2 GHz
$M_1 = M_2$	290 μm
L	0.18 μm
C_{ox}	K ε_{ox}/t_{ox} = 9.45 $fF/\mu m^2$
L_1	7.66 nH
R_1	20 / 10* Ω
L_G	10.7 nH
L_S	0.55 nH
C_D	100 / 120* fF
C_{ex}	120 fF

***: refined for post-layout**

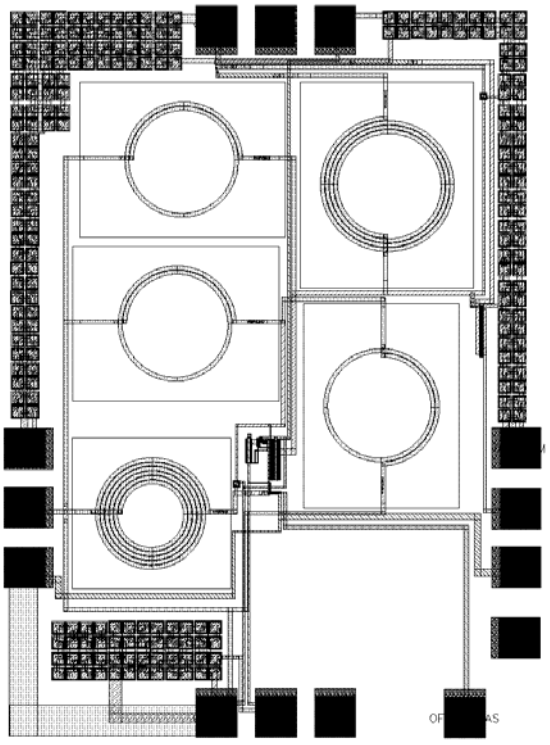

Figure 3.9: Layout of CMOS LNA2 with GSG pad and DCQ pad for dc supply and biasing voltage [88]

3.3.3 Multi-standard multi-band LNA designs – 0.9 GHz with no buffer

3.3.3.1 LNA3

In this circuit, the buffer section was not included as it is used for testing purposes as well as to achieve output matching [72] [79]. On the other hand, to achieve output return loss below -10 dB, a new technique has been used by introducing one inductor and

resistor $(R_1 L_1)$ connected in series and placed in parallel with the load inductor. By doing that, some compromise in gain should be observed.

Figure 3.10 presents the schematic diagram of a wide band IDCS LNA3, designed using 0.25 µm technology (same as LNA1) and targeted to cover carrier frequency from 800 to 1000 MHz. This range of frequencies include the GSM standards (GSM850 and GSM900) and 3G standards (Band V-VI) [2] [7]. Thus, to accommodate such frequency range from 800 to 1000 MHz, frequency centre of 0.9 GHz was chosen. The input-matching bandwidth (Δf) was selected to be 200 MHz to satisfy $20 \log |S_{11}| \leq -10\ dB$.

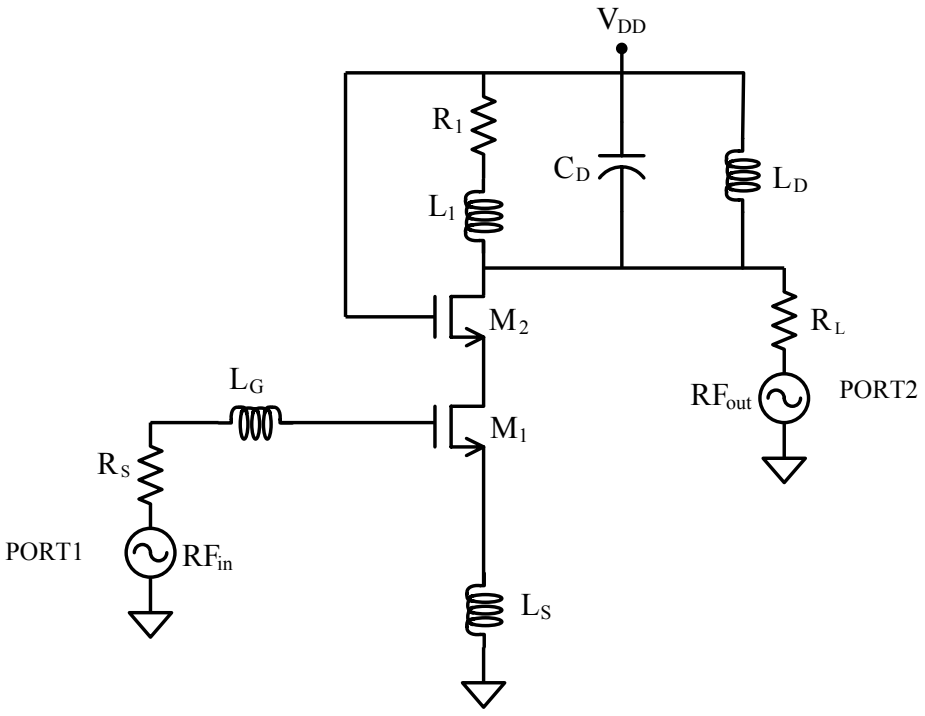

Figure 3.10: Wide band LNA3 [89]

To determine the input matching, (3.1) and (3.33) were used. But for output impedance matching the following equations were used:

$$Y_L = sC_D + \frac{1}{r+sL_D} + \frac{1}{R_l+sL_l}$$

$$\therefore Z_L = \frac{1}{Y_L} = \left(\frac{1}{sC_D}\right) \square \left(r+sL_D\right) \square \left(R_l+sL_l\right) \tag{3.46}$$

$$= \frac{R_1 r + s\left(R_1 L_D + L_l r\right) + s^2 L_l L_D}{1 + sC_D\left(r + R_1\right) + s^2 C_D\left(L_l + L_D\right)}$$

where r is the series resistance of L_D, and C_D, L_D, L_l and R_l are the load capacitor, load inductors and load resistor respectively.

At resonance, C_D, L_D, L_l will be eliminated and leaving the real impedance into play.

The gain of the LNA is obtained by:

$$S_{21} = 2\frac{v_{out}}{v_{in}} \equiv G_{m21}(s).Z_L(s) \tag{3.47}$$

where $G_{m21}(s)$ represents the transconductance gain when the input voltage adopts the input-terminal voltage (i.e., $v_{in}/2$). $Z_L(s)=1/Y_L(s)$ represents the equivalent load impedance seen at the drain terminal of transistor M_2.

In the design of LNA3, the previous expressions used to determine the specifications for the LNA1 are still applicable except for (3.46) and (3.47). Table 3.3 shows the components values for LNA3 [89].

Table 3.3: Component values for LNA3

Case	Condition
Freq.	2 GHz
M_1	475 μm
M_2	235 μm
L	0.36 μm
C_{ox}	K ε_{ox}/t_{ox} = 5.95 $fF/\mu m^2$
L_D	6 nH
L_1	0.5 nH
R_1	50 Ω
L_G	19.5 nH
L_S	0.9 nH
C_D	3 pF

3.3.3.2 LNA4

Figure 3.11 presents the schematic diagram of wide band IDCS LNA4 targeted to cover carrier frequency from 800 to 1000 MHz. The difference between LNA3 and LNA4 can be seen at the input tank. In this design, C_{ex} was used to give extra freedom at the input tank for the input matching. Therefore, (3.44) and (3.45) were used in determining the input impedance for LNA4. As for other specifications, the previous equations used as in LNA1 to LNA3 are also applicable in this design. Table 3.4 shows the corresponding components values used for LNA4 [90].

To prove the validity of this circuit design, the layout has been implemented using 0.18 µm technology by means of Cadence tools while Calibre tools were utilised to obtain post-layout design rule check (drc), layout versus schematic (lvs) and parasitic extraction (pex). Figure 3.12 shows the layout of the wideband LNA4. This layout has been submitted for fabrication. Notice that for L_S, three inductors (2.26 nH) have been used in parallel to realise the 0.75 nH. Similar to LNA2, they were used for proof-of-concept only.

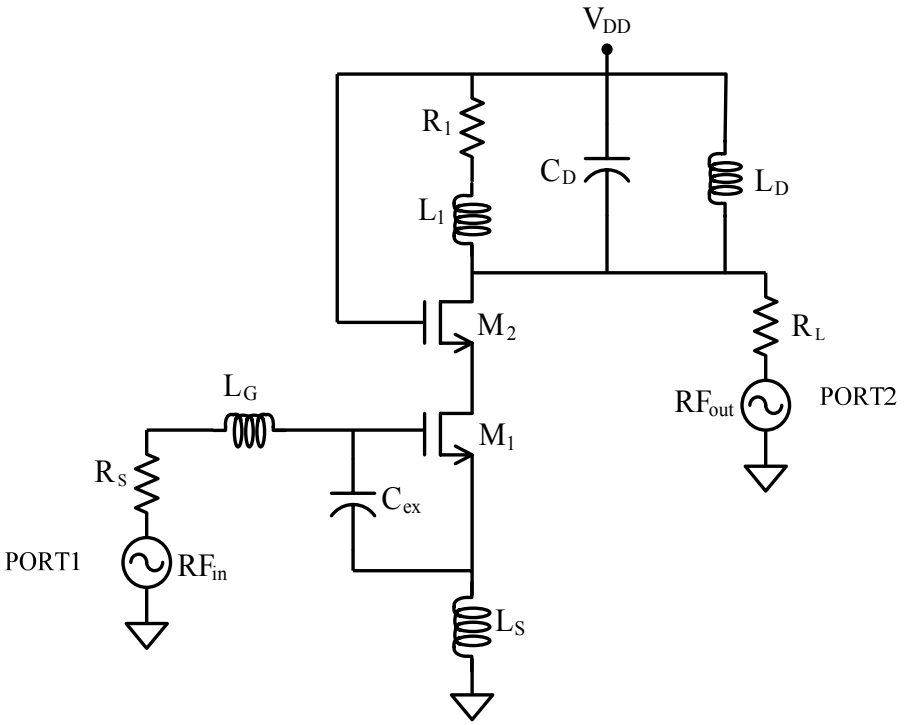

Figure 3.11: Wide band LNA4 [90]

Table 3.4: Component values for LNA4

Case	Condition
Freq.	0.9 GHz
L	0.18 μm
C_{ox}	K $\varepsilon_{ox}/t_{ox} = 9.45\ fF/\mu m^2$
L_1	4.21 nH
R_1	55 Ω / 40 Ω*
L_D	15.8 nH
L_G	22.9 nH
L_S	0.75 nH
C_D	2.63 pF / 2.25 pF^*
C_{ex}	1.35 pF

***: refined for post-layout**

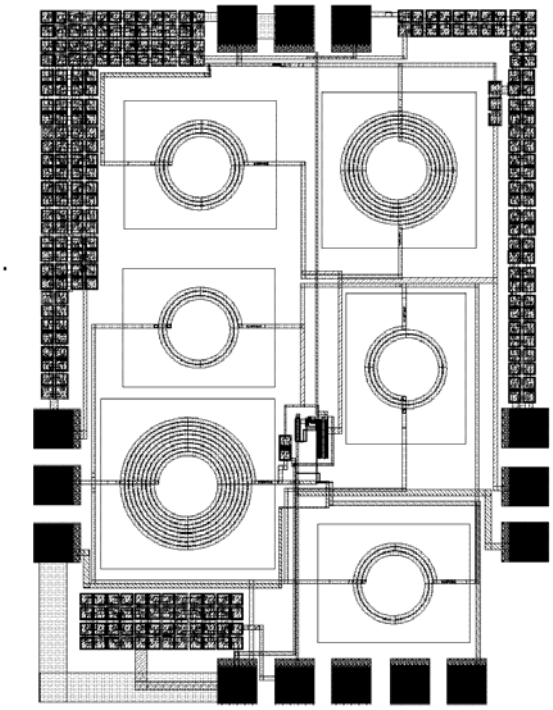

Figure 3.12: Layout of CMOS LNA4 with GSG pad and DCQ pad for dc supply and biasing voltage [90]

3.3.4 Multi-standard multi-band LNA design – 2 GHz with no buffer

3.3.4.1 LNA5

Figure 3.13 presents the schematic diagram of wide band IDCS LNA1 targeted to cover carrier frequency from 1800 to 2200 MHz. A frequency centre of 2 GHz was chosen. The input-matching bandwidth of Δf i.e., the frequency range that satisfies $20\ log\ |S_{11}| \leq -10\ dB$ was selected to be 400 MHz, same as LNA1 and LNA2. But, in this implementation, technique used for LNA3 and LNA4 was implemented where $R_1 L_1$ were connected in series and placed in parallel with the load inductor. Therefore, the expressions used for LNA3 and LNA4 are also used to determine the specifications for this LNA. As a result, Table 3.5 shows the corresponding components values used for LNA5 [91].

Similar to LNA4, the layout has been implemented using 0.18 µm technology and also was sent for fabrication. Figure 3.14 shows the layout for LNA5. Notice that for L_S, three inductors (1.65 nH) have been used in parallel to realise the 0.55 nH, and they were used for proof-of-concept.

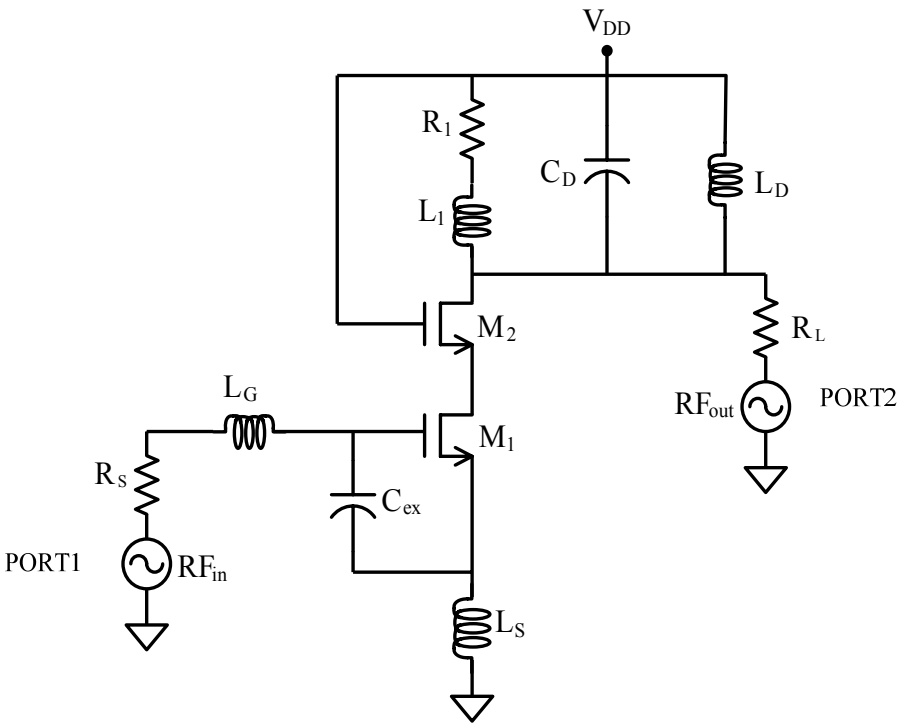

Figure 3.13: Wide band LNA5 [91]

Table 3.5: Component values for LNA5

Case	Condition
Freq.	2 GHz
L	0.18 µm
C_{ox}	K $\varepsilon_{ox} / t_{ox}$ = 9.45 fF /µm^2
L_1	4.21 nH
R_1	55 Ω / 40 Ω*
L_D	15.8 nH
L_G	10.7 nH
L_S	0.55 nH
C_D	400 fF / 150 fF *
C_{ex}	160 fF / 250 fF *

***: refined for post-layout**

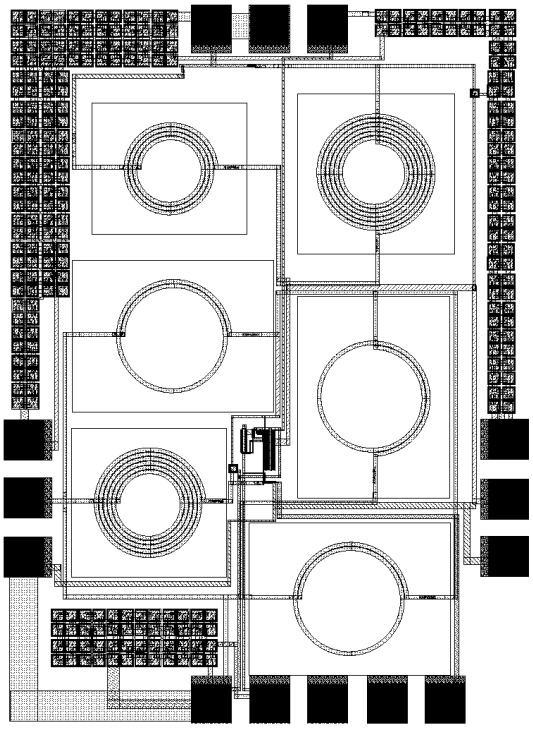

Figure 3.14: Layout of CMOS LNA5 with GSG pad and DCQ pad for dc supply and biasing voltage [91]

3.4 Conclusion

This chapter has presented the theories and designs of the LNAs for multi-standard multi-band mobile receiver. Five LNAs (LNA1 to LNA5) were presented in two bands (800 to 1000 MHz; 1800 to 2200 MHz) with different frequency centres' of 900 MHz and 2 GHz along with the other two different techniques – buffered and unbuffered. The designs were using two different technologies – from NCSU and wafer foundry. With these designs, it was proven that the use of IDCS technique is not just suitable for narrowband but also for a rather wider band design. With the wide band LNA approach,

the need for multiple LNAs in parallel (in the multi-standard receiver the front-end design) was reduced significantly.

In the next chapter, the results of the implemented LNA designs will be presented. The reason why such a designs introduced in this chapter will be discussed in further details in form of results and justifications.

CHAPTER 4:

RESULTS & DISCUSSION

4.0 Introduction

The theories, designs and implementations of multi-standard multi-band LNAs for two bands of interest (i.e. lower band; 800 to 1000 MHz and upper band; 1800 to 2200 MHz) have been presented in Chapter 3. This research was carried to design and implement the wide band multi-standard multi-band LNAs. Also, the feasibility of using IDCS (topology which was typically used for designing a narrowband LNA) for wide band approach has been approved.

In this chapter, detailed simulation results and discussion on the design of the two stages – pre-layout and post-layout will be presented. Section 4.1 provides the pre-layout results while post-layout results are presented in section 4.2. Following that is the discussion of the results which are provided in Section 4.3. Conclusion remarks are ended in Section 4.4.

4.1 Pre-layout simulation results

In the design of multi-standard multi-band LNAs, the simulation for pre-layout was carried out using Cadence design suite. The following sub-sections will highlight the results and the discussion of the wide band LNAs (LNA1 to LNA5).

4.1.1 Multi-standard multi-band LNA designs – 2 GHz with buffer

4.1.1.1 LNA1

The wideband IDCS LNA1 was designed using a 0.25 μm standard CMOS technology. Figures 4.1 to 4.5 illustrate the simulation results of the s-parameters, NF and linearity ($P1dB$ and $IIP3$) respectively.

Figure 4.1 presents S_{21} or power gain achieved in the simulation. The illustration indicates value of about 23 dB at peak and remains approximately between 11 to 23 dB along the design bandwidth of 400 MHz. This peak value is good as it is exceeds the targeted specification as set in Table 2.5. Figure 4.1 also shows the reverse isolation or S_{12}. The attained value is -47 dB at peak frequency and is believed to be a good reverse isolation as it exceeds the requirement which is typically -30 dB.

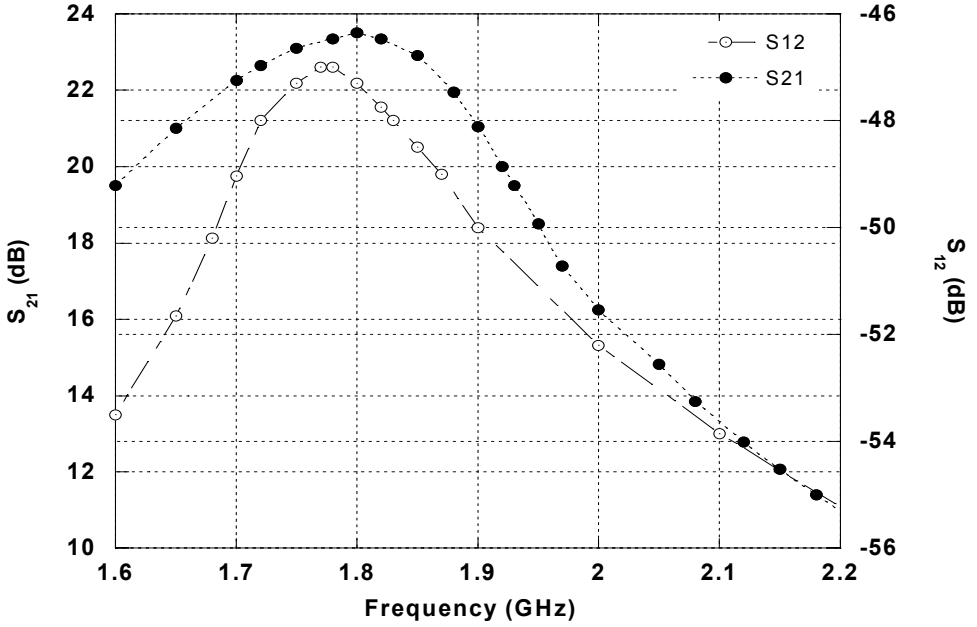

Figure 4.1: Forward gain and reverse isolation of LNA1.

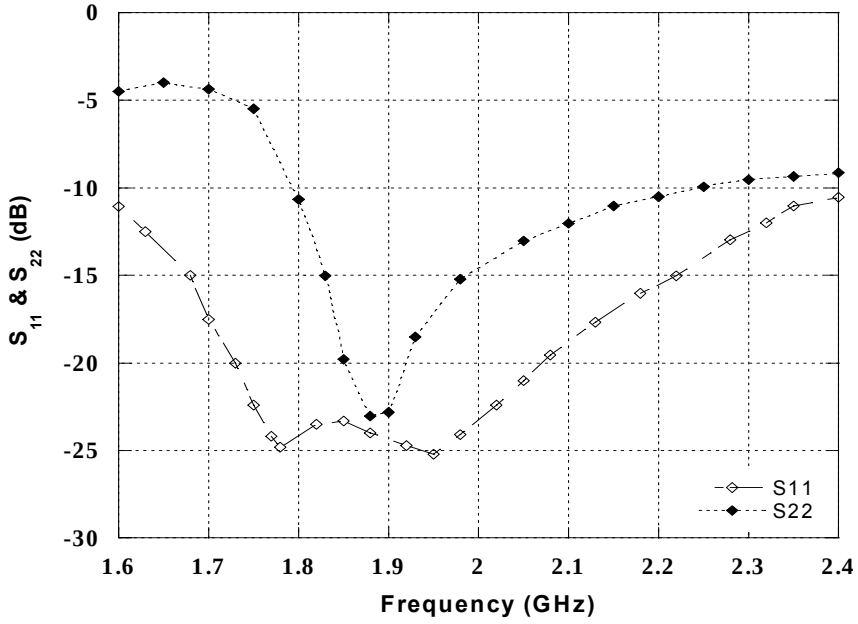

Figure 4.2: Input and output return losses of LNA1.

In Figure 4.2, the input reflection coefficient (S_{11}) of the LNA1 achieved is -25.2 dB while output reflection coefficient (S_{22}) is -23 dB at peak frequency. As shown in Figure 4.2, the input reflection coefficient remains under -10 dB which begins from 1.6 GHz and ends at 2.4 GHz. This yields twice the bandwidth required. It also indicates that this design for the input impedance matching is acceptable and within expectation. However, for the output reflection coefficient, the bandwidth achieved follows the bandwidth set by the calculation which is from 1.8 GHz to 2.2 GHz. Therefore, S_{22} is not as superior as S_{11}, but it is still within expectation.

Figure 4.3 shows the noise figure of the LNA1 achieved in the simulation. It is below 1.5 dB along the band of interest and is about 0.6 dB at peak.

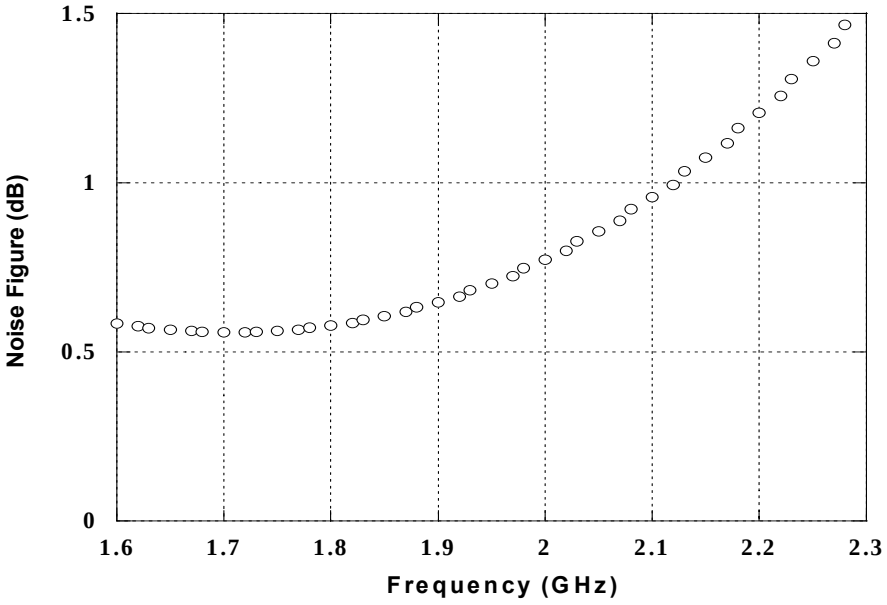

Figure 4.3: Noise figure of LNA1.

To check for the linearity requirement, a two-tone test for third-order intercept point was performed on the LNA. The two tones were applied at frequencies of 2 GHz and 2.05 GHz respectively with equal power. The achieved $IIP3$ is -5.1 dBm and is shown in Figure 4.4. This achieved value is typically an acceptable specification and represents the trade-off between power consumption and linearity requirements. In other words, the design has been optimised to obtain the best IIP3 value with intention to consume the least amount of current in the circuit. In addition, transistor M_3 limits the linearity of the circuit due to the gain which precedes it [25].

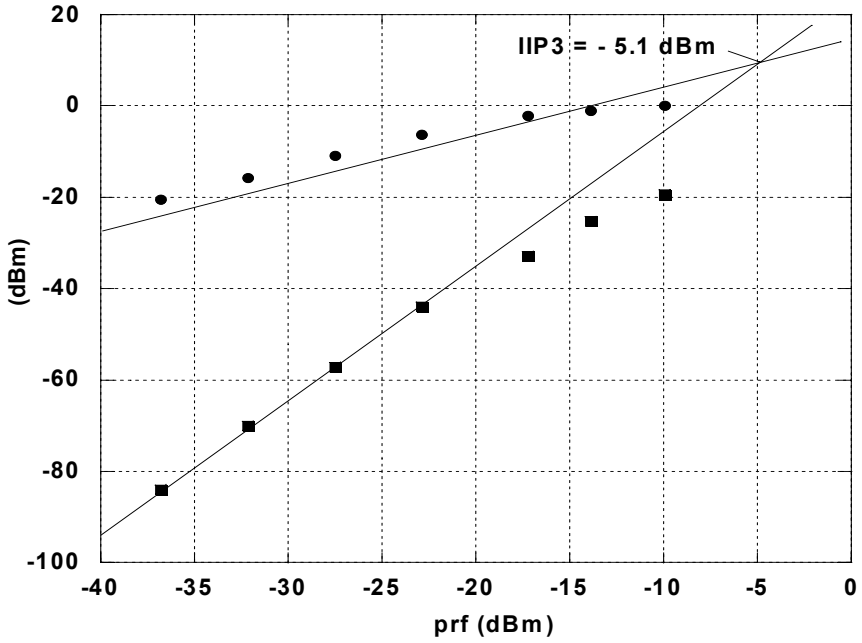

Figure 4.4: $IIP3$ of LNA1.

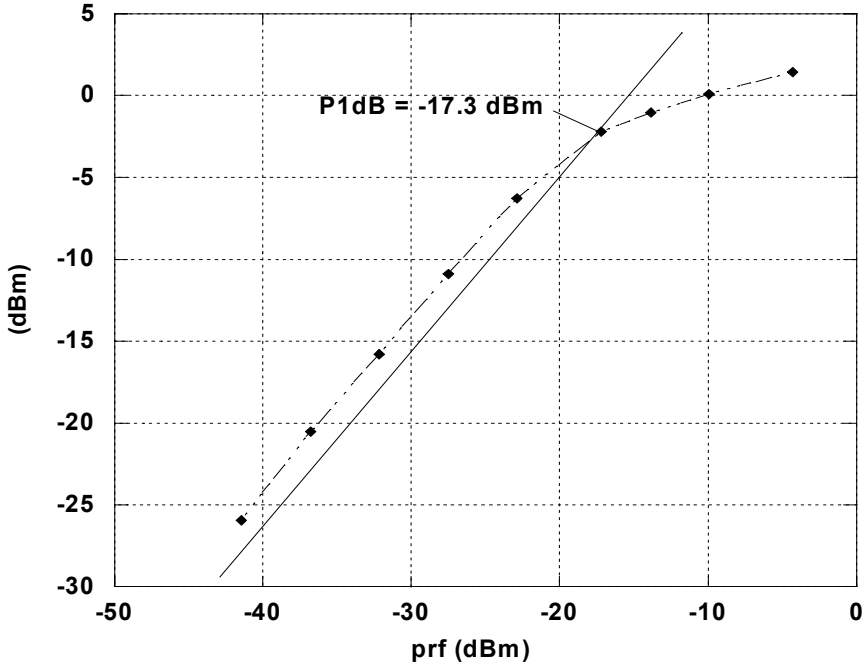

Figure 4.5: $P1dB$ of LNA1.

Another measurement for linearity is the $P1dB$. As shown in Figure 4.5, the simulated $P1dB$ achieved is -17.3 dBm. Also, notice that the achieved value is typically an acceptable specification and is a trade-off between power consumption and linearity requirements.

4.1.1.2 LNA2

As mentioned in Chapter 3, the wide band IDCS LNA2 was designed using a 0.18 µm CMOS technology. The simulation results of LNA2 are shown in Figure 4.6 to 4.10. The power gain (S_{21}) obtained is about 23.16 dB at the center frequency and is shown in Figure 4.6. Notice that the center frequency is slightly shifted to the right from the targeted frequency (2 GHz) to about 2.05 GHz. The reason behind this is because of

the quality factor of the inductors used, which are derived at 2.4 GHz by the foundry while this design is resonated at 2 GHz. The gain obtained is well above 10 dB and range from 21.9 to 22.6 dB along the 400 MHz bandwidth.

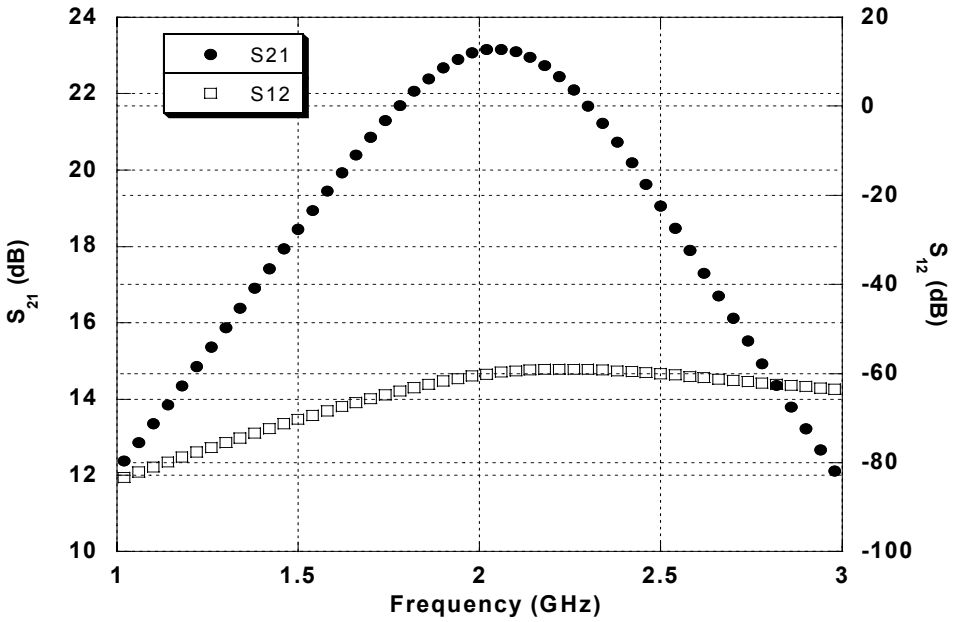

Figure 4.6: Forward gain and reverse isolation of LNA2.

The reverse isolation (S_{12}) obtained from the simulation is better than the typical value which is normally -30 dB. As shown in Figure 4.6, the S_{12} of the circuit gives the values ranging from about -63.5 to -59 dB along the 400 MHz bandwidth.

The input and output return losses, S_{11} and S_{22} of the LNA are shown in Figure 4.7. For S_{11}, the simulation produced an input return loss of -35.6 dB at the center frequency and ranging from -11.6 dB to -14.8 dB along the bandwidth set. For output return loss,

(shown as S_{22} (a) in Figure 4.7), simulation result produced value of -26.9 dB at the center frequency and as expected, is well below -10 dB along the bandwidth targeted. However this value is achieved before optimisation for linearity been put into place.

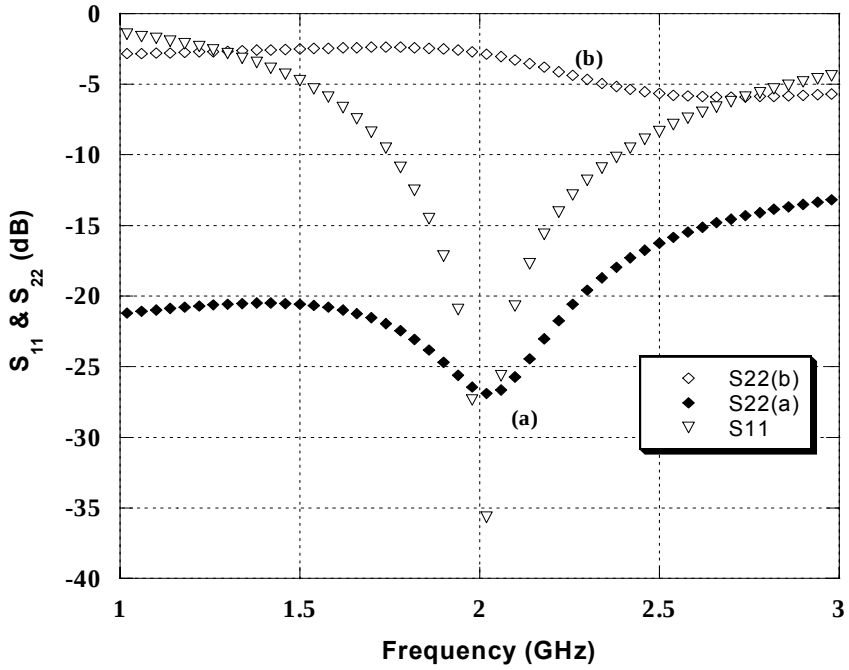

Figure 4.7: Input and output return losses of LNA2: S_{22} (a) not optimised for linearity, S_{22} (b) optimised for linearity

The noise figures of the circuit obtained is below 2 dB and quite flat along the 400 MHz bandwidth ranging from 1.64 to 1.98 dB as shown in Figure 4.8.

To check for the linearity requirement, a two-tone test for third-order intercept point was performed on the LNA. The two tones were applied at frequencies of 2 GHz and 2.01 GHz respectively with equal power. The achieved $IIP3$ is -7.08 dBm and is shown in

Figure 4.9. This achieved value is typically an acceptable specification and represents the trade-off between the S_{22}, power consumption and linearity requirements. In other words, to achieve the specification for $IIP3$, the design has been optimised to obtain the best $IIP3$ value but has to trade-off with the output return loss. Thus, in Figure 4.7, S_{22} (b) shows the corresponding S_{22} for the circuit which clearly below the target (-10 dB). This could be explained further by looking into the equation (3.40). The change of the current in M_3 changes the C_{gs3}, thus alters the output impedance $Z_{\mathrm{L}}(s)$. In addition, buffer implementation used in this design was not a good choice as it limits the linearity and destroys the output return loss (S_{22}) of the circuit. Hence, this problem has been addressed in LNA5 design.

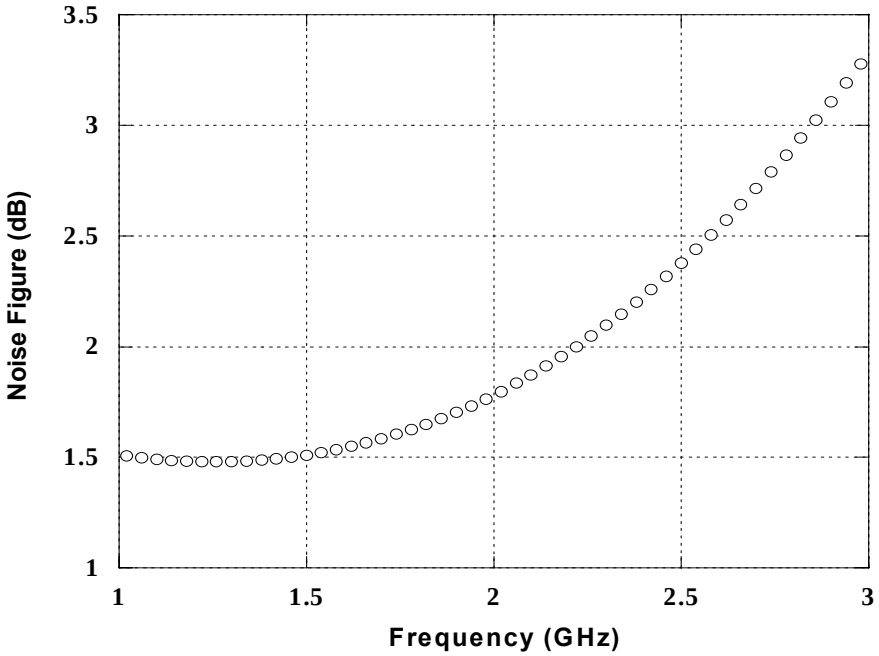

Figure 4.8: Noise figure of LNA2.

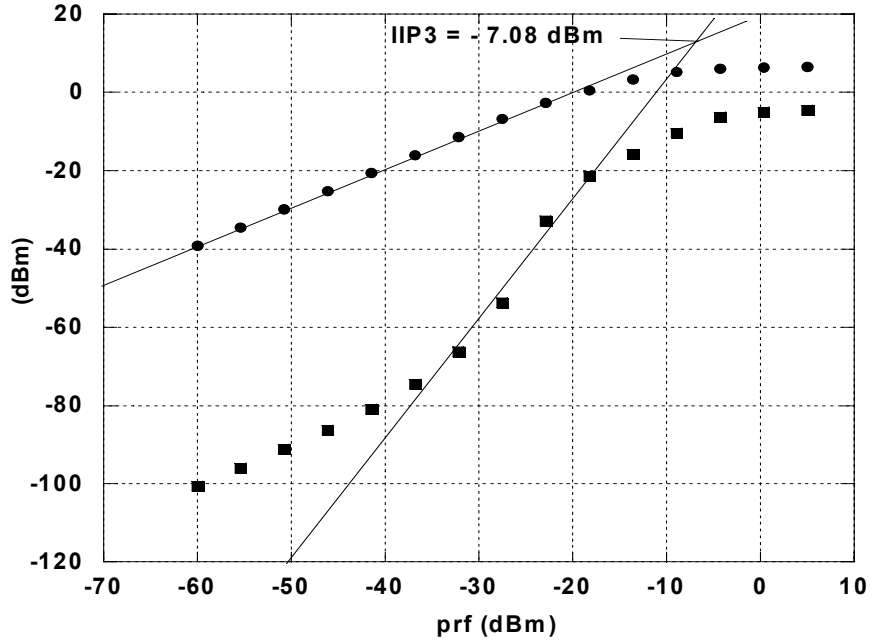

Figure 4.9: *IIP3* of LNA2.

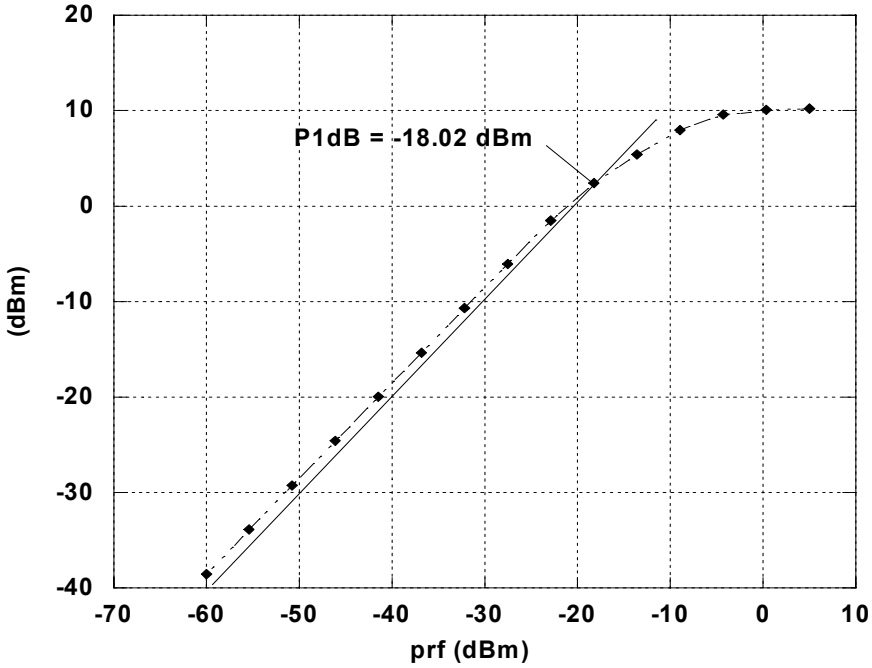

Figure 4.10: *P1dB* of LNA2.

For compression point ($P1dB$), shown in Figure 4.10, the achieved result is -18.02 dBm. Notice that the achieved value is typical and is a trade-off between S_{22}, linearity requirement and power consumption.

4.1.2 Multi-standard multi-band LNA designs – 0.9 GHz with no buffer

4.1.2.1 LNA3

The wideband IDCS LNA3 was designed using a 0.25 µm standard CMOS technology. Figures 4.11 to 4.15 show the simulation results of the LNA3. Figure 4.11 presents the S_{21} achieved in the simulation. The illustration indicates value of around 12 dB at peak and remains approximately more than 10 dB along the design bandwidth. Figure 4.11 shows also, the reverse isolation S_{12}. The attained value is about -52 dB and is good reverse isolation as it exceeds the requirement which is typically -20 to -30 dB.

Figure 4.12 shows the input and output return losses; S_{11} and S_{22} of LNA3. For S_{11}, the obtained value is -14 dB while for S_{22} is about -34 dB at peak frequency. The input return loss (S_{11}) remains under -10 dB which begins from 800 MHz and ends at 1.03 GHz. It indicates that the design for input impedance matching is acceptable and within expectation. On the other hand, the output return loss (S_{22}) achieved remains well under -10 dB and more than the targeted values which range from 700 MHz to 1.1 GHz.

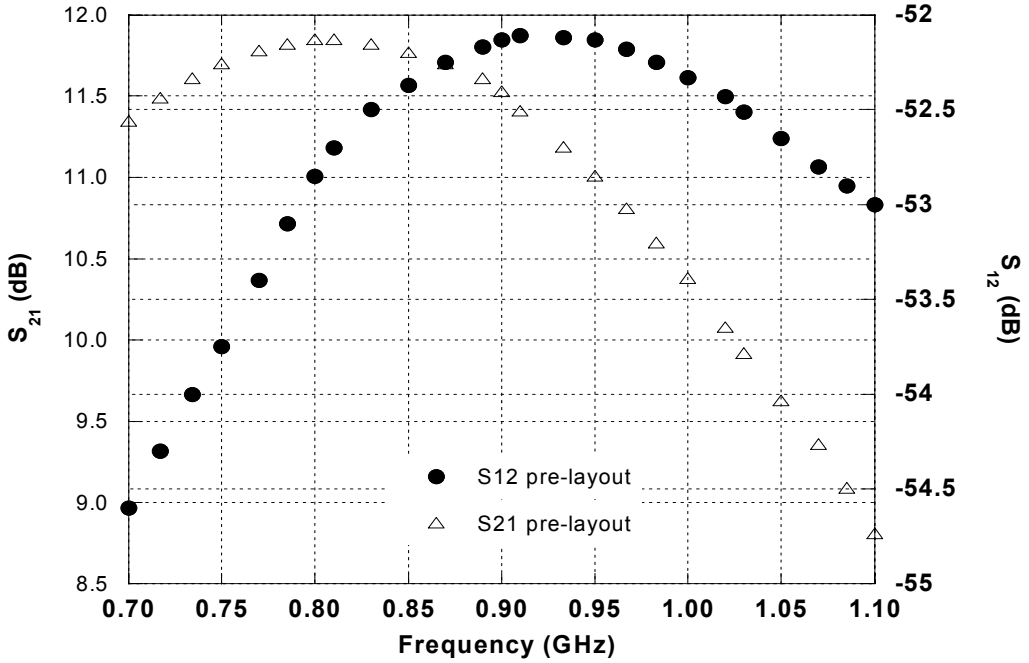

Figure 4.11: Forward gain and reverse isolation of LNA3.

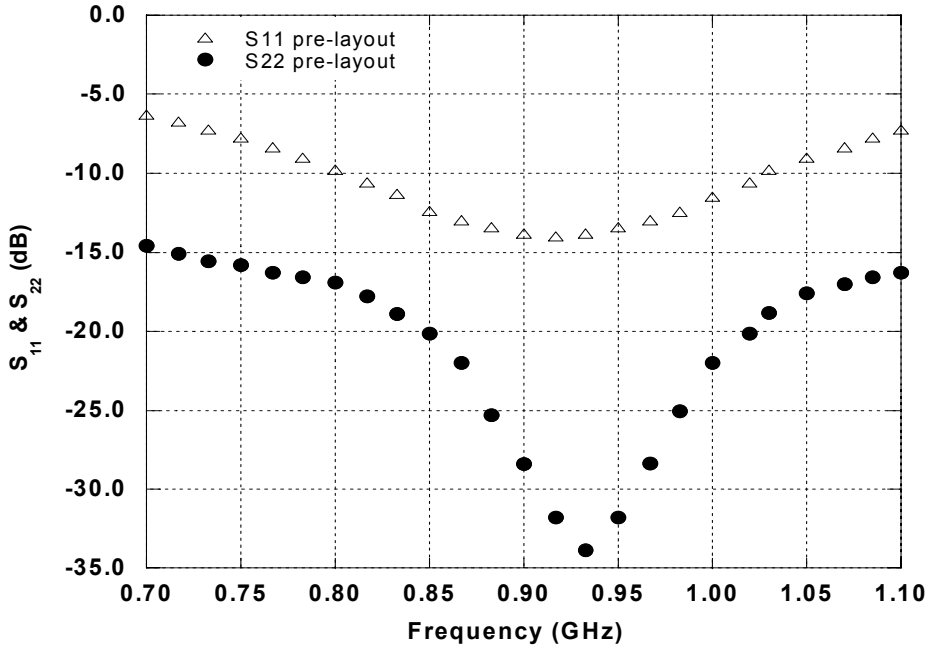

Figure 4.12: Input and output return losses of LNA3.

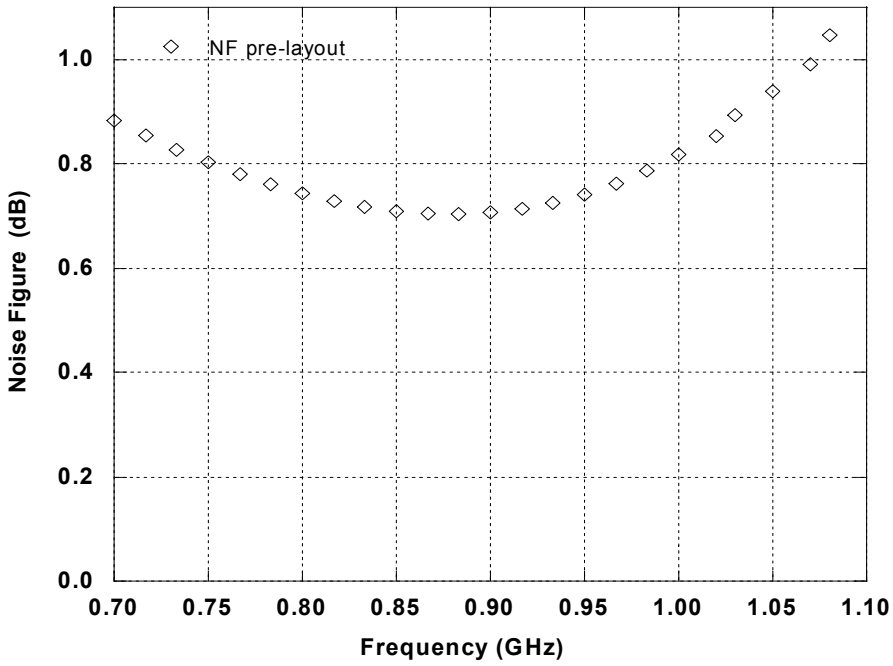

Figure 4.13: Noise figure of LNA3.

Figure 4.13 shows the noise figure of the LNA3 achieved in the simulation. It is reasonably flat over the band of interest and is about 0.7 dB at peak. Also shown is the noise figure ranging from 0.75 to 0.8 dB along the bandwidth of 200 MHz.

For the linearity requirement, a two-tone test for third-order intercept point was performed on the LNA3. The two tones were applied at frequencies of 900 MHz and 920 MHz respectively with equal power. The achieved $IIP3$ is +7.63 dBm as shown in Figure 4.14. This achieved value exceeded the specification needed. In other words, the design has been optimised to obtain the best $IIP3$ value with intention to consume the least amount of current in the circuit.

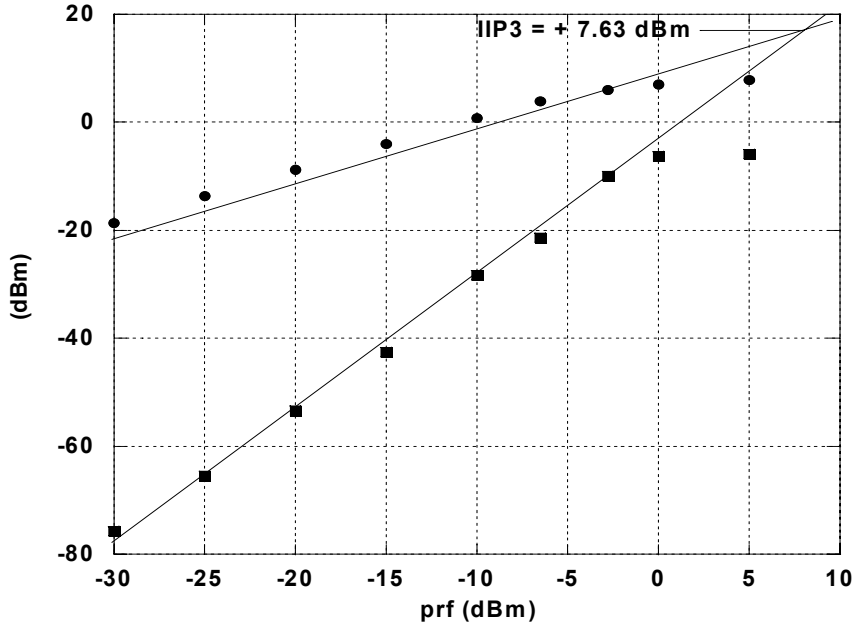

Figure 4.14: *IIP3* of LNA3.

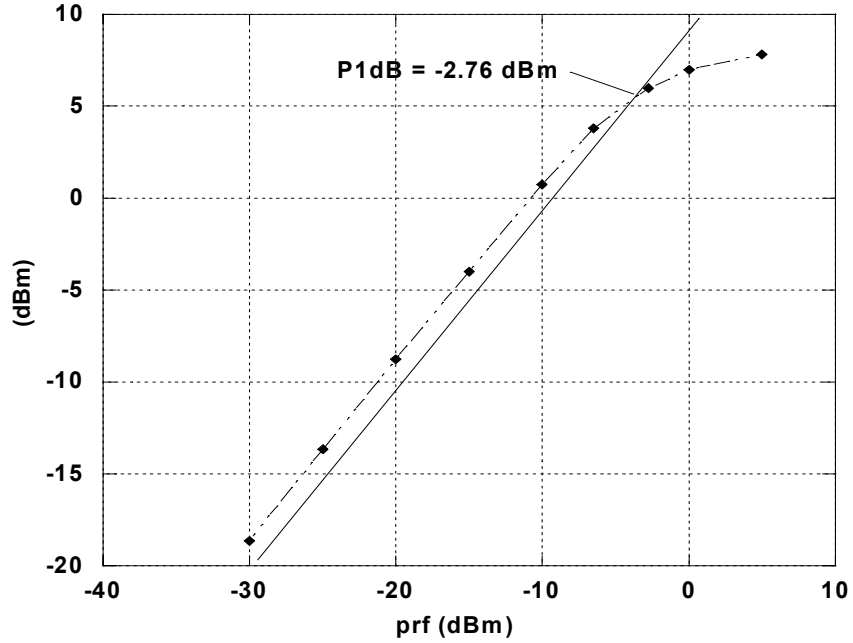

Figure 4.15: *P1dB* of LNA3.

Figure 4.15 shows the result for $P1dB$. The simulated result achieved is -2.76 dBm and is believed to be a good value as it is far from the optimum specification.

4.1.2.2 LNA4

The wideband IDCS LNA4 was designed using a 0.18 μm standard CMOS technology. The simulation results are shown in Figure 4.16 to 4.20. The achieved power gain (S_{21}) is about 11.32 dB at the center frequency as shown in Figure 4.16. Observe that the center frequency is shifted to the left from the targeted frequency (900 MHz) to about 790 MHz. This is due to the quality factor of the inductors used, which are derived at 2.4 GHz by the foundry, while this design is resonated at 900 MHz. The reverse isolation (S_{12}) obtained is better than the typical value, which is normally -30 dB. As shown in Figure 4.16, S_{12} of the circuit gives values ranging from about -62.22 to -61.51 along the 200 MHz bandwidth and believed to be a good specification as it exceeded the targeted values.

Figure 4.17 shows the input and output return losses; S_{11} and S_{22}. For S_{11}, the value is -47.7 dB at the center frequency and ranging from -12.34 to -11.34 dB over frequency band of 800 to 1000 MHz.. For S_{22}, at the center frequency, -23.88 dB (slightly shifted to 915 MHz) is obtained and ranging from -20.89 to -19.06 dB along the 200 MHz bandwidth. Notice that the shift of the center frequency at 915 MHz cannot be avoided as the optimisation is limited by the inductors used, where their values ranging from 1.65 to 22.9 nH at 10 different values supplied by the foundry. Thus, the optimisation can only done by adjusting C_{D} and R_1. The output return loss achieved, however, is well below -10 dB along 200 MHz bandwidth and is within expectation.

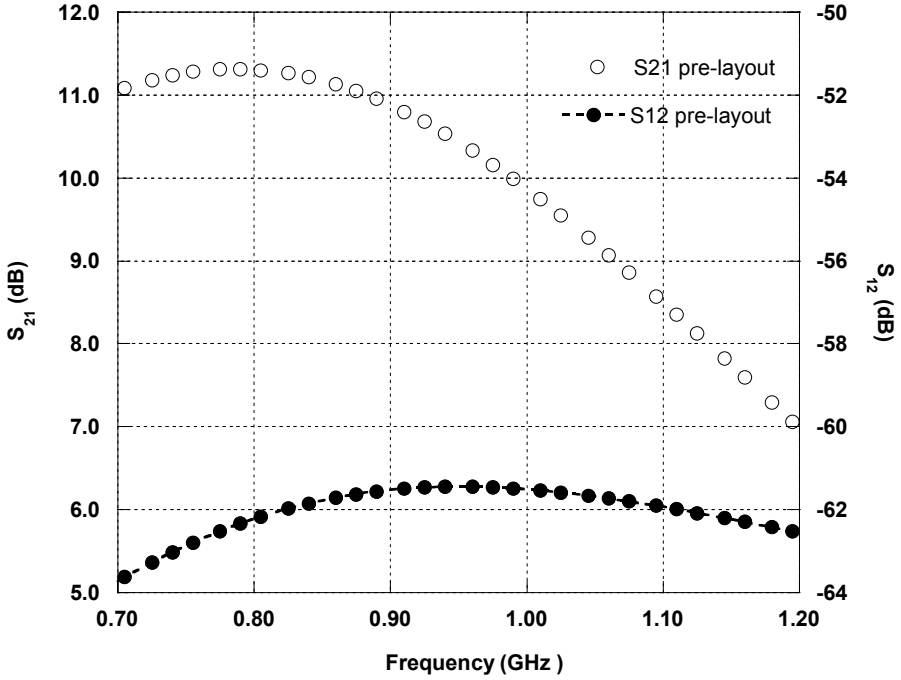

Figure 4.16: Forward gain and reverse isolation of LNA4.

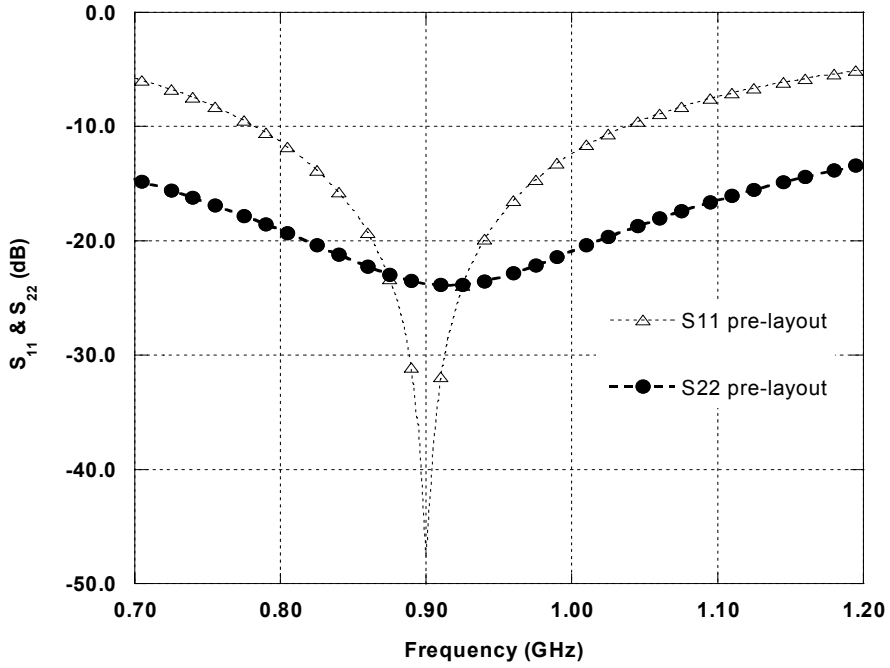

Figure 4.17: Input and output return losses of LNA4.

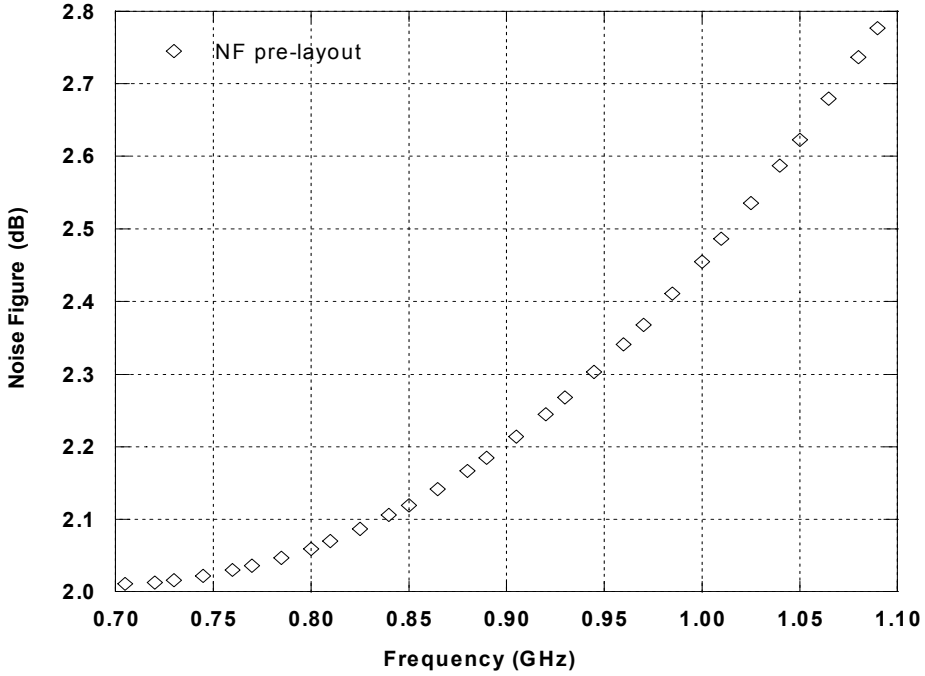

Figure 4.18: Noise figure of LNA4.

The noise figure of the circuit is around 2.2 dB at the center frequency as shown in Figure 4.18. This value is good giving the fact that the inductor L_G is big which corresponds to the high series resistance at the input. Also shown are noise figures ranging from 2.06 to 2.46 dB along the bandwidth of 200 MHz.

For the linearity requirement, a two-tone test for third-order intercept point was performed on the LNA4. The two tones were applied at frequencies of 900 MHz and 920 MHz respectively with equal power. The achieved $IIP3$ is +8.28 dBm and is shown in Figure 4.19. This achieved value exceeds the specification needed. In other words, the design has been optimised to obtain the best $IIP3$ value with intention to consume the least amount of current in the circuit.

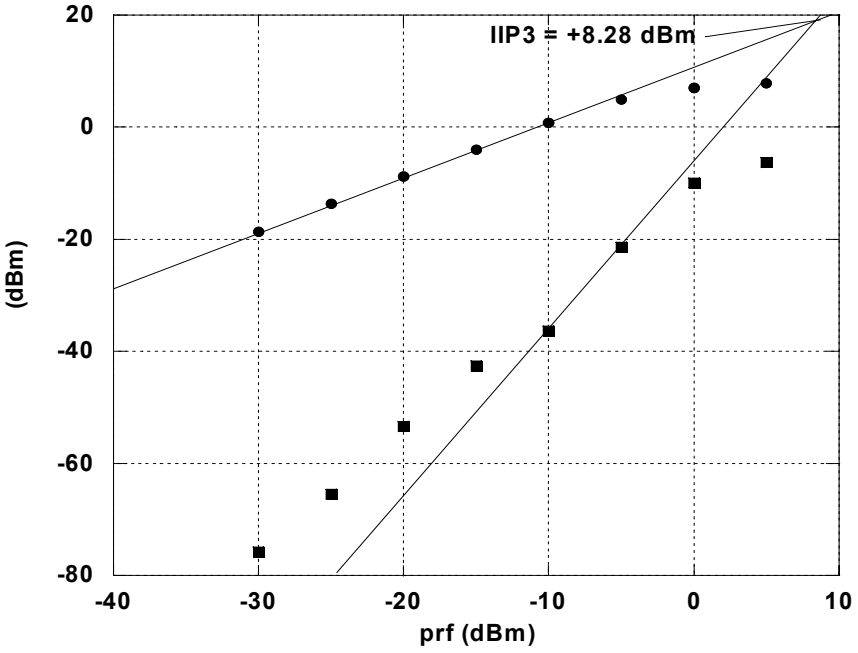

Figure 4.19: *IIP3* of LNA4.

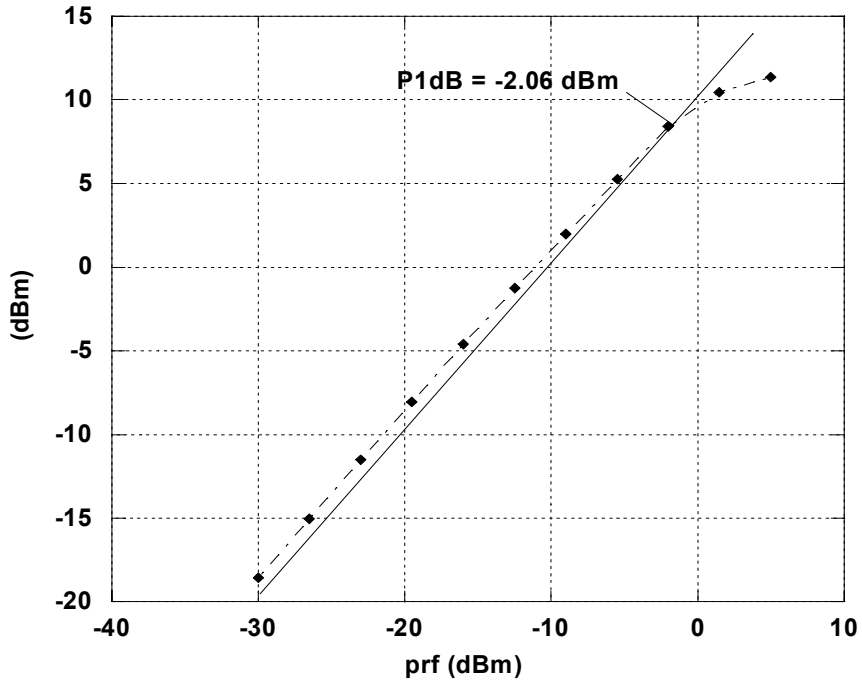

Figure 4.20: *P1dB* of LNA4.

The simulated result for $P1dB$ as shown in Figure 4.20 is -2.06 dBm and is good as it is far from the targeted specification.

4.1.3 Multi-standard multi-band LNA design – 2 GHz with no buffer

4.1.3.1 LNA5

Similar to LNA2 and LNA4, the wideband IDCS LNA5 was designed using a 0.18 µm standard CMOS technology. The simulation results are shown in Figures 4.21 to 4.25. The forward gain (S_{21}) achieved is about 12.6 dB at the center frequency as shown in Figure 4.21. Notice that the center frequency is slightly shifted to the left from the targeted frequency (2 GHz) to about 1.7 GHz. This happens because of the quality factor of the inductors used (derived at 2.4 GHz by the foundry while this design is resonated at 2 GHz). The gain obtained is well above 10 dB along the bandwidth needed. However, compared to LNA2, this LNA5 experiencing low gain because of the optimisation method used causing the gain reduction. This is the trade-off made in order to achieve on-chip matching for the LNA5 design.

The reverse isolation (S_{12}) obtained from the simulation is well above the typical value which is normally -30 dB. In Figure 4.21, the S_{12} of the circuit gives values ranging from about -51 to -48 dB along the 400 MHz bandwidth.

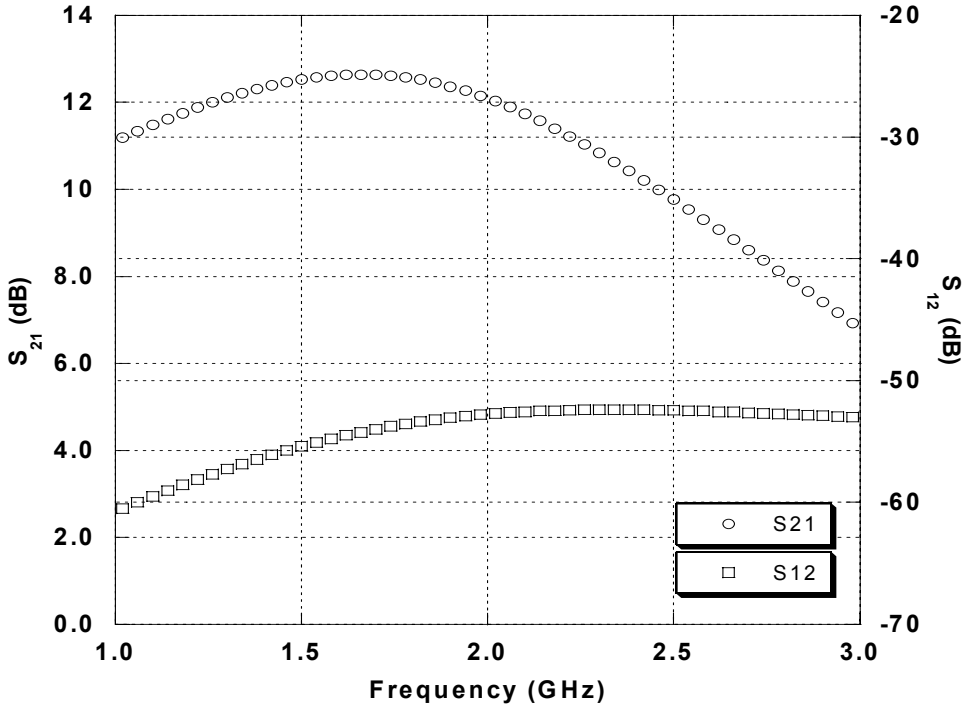

Figure 4.21: Forward gain and reverse isolation of LNA5.

The input and output losses, S_{11} and S_{22} of LNA5 are shown in Figure 4.22. For S_{11}, the simulation produced an input return loss of -24.4 dB at the center frequency and ranging from -12.9 dB to -14.83 dB along the bandwidth set. For S_{22}, simulation result produced a value of -11.21 dB at the center frequency. Notice that the shifting of the center frequency is at 1.7 GHz. This cannot be avoided as the optimisation is limited by the inductors used, where their values ranging from 1.65 nH to 22.9 nH at 10 different values. Therefore, the optimisation can only be done by adjusting R_{I} and C_{D}. The output return loss achieved, however, is well below -10 dB along the bandwidth targeted.

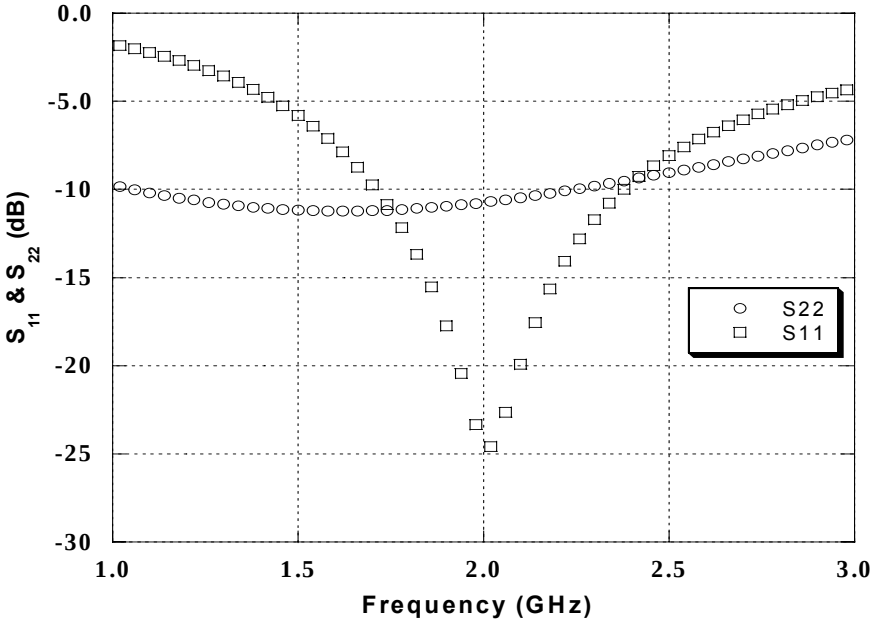

Figure 4.22: Input and output return losses of LNA5.

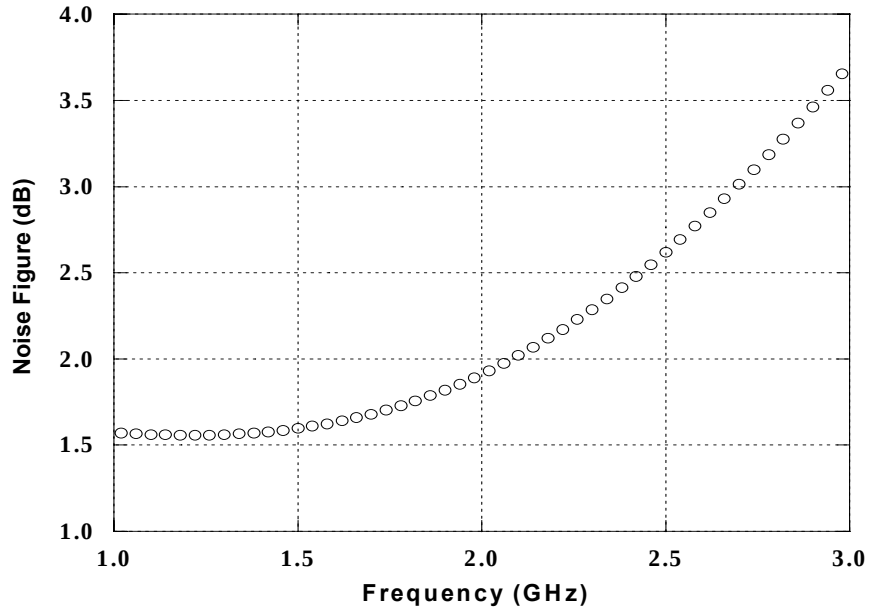

Figure 4.23: Noise figure of LNA5.

The noise figures of the circuit obtained is 1.91 dB at the center frequency and is ranging from 1.74 to 2.15 dB along the 400 MHz bandwidth as shown in Figure 4.23.

For the linearity requirement, a two-tone test for third-order intercept point was performed on the LNA5. The two tones were applied at frequencies of 2 GHz and 2.01 GHz respectively with equal power. The achieved $IIP3$ is +8.4 dBm and is shown in Figure 4.24. This value achieved is better than LNA2 (for similar technology) and exceeds the specification. In other words, the design has been optimised to obtain the $IIP3$ as best as possible for the circuit. On the other hand, Figure 4.25 shows the result for $P1dB$. The simulated result achieved is -2.02 dBm and is better than the specification.

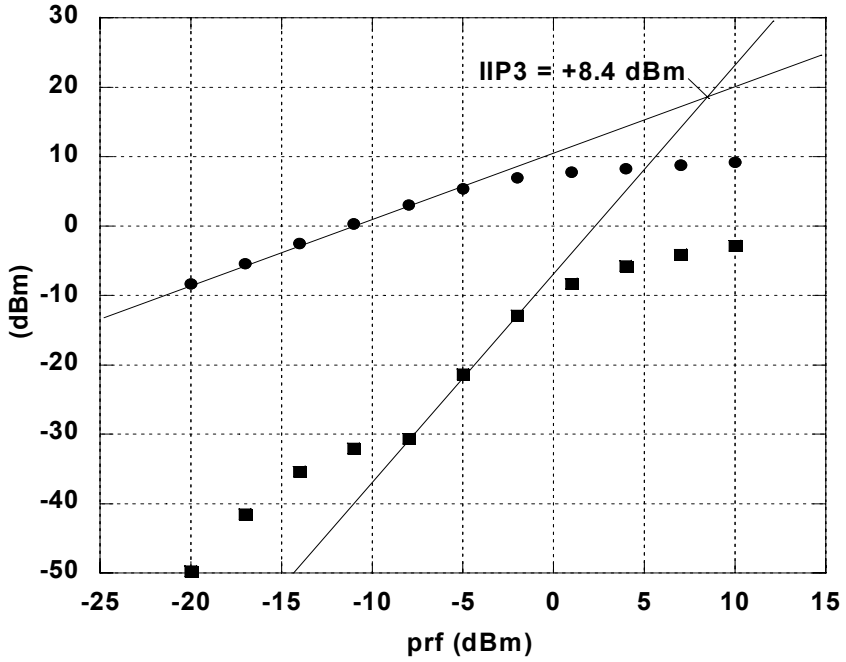

Figure 4.24: $IIP3$ of LNA5.

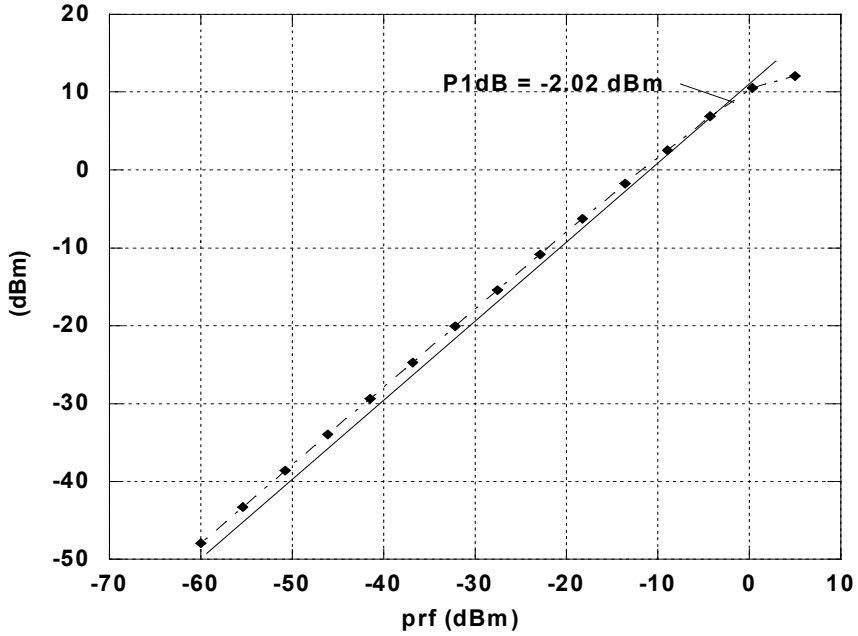

Figure 4.25: $P1dB$ of LNA5.

4.2 Post-layout simulation results

In this section, for post-layout simulation, Cadence and Calibre tools were utilised to obtain post-layout design rule check (drc), layout versus schematic (lvs) and parasitic extraction (pex).

4.2.1 Multi-standard multi-band LNA2 design – 2 GHz with buffer

The post-layout simulation results are shown in Figures 4.26 to 4.28. For power gain (S_{21}) as in Figure 4.26, the achieved value is about 25.6 dB at the center frequency. Notice that the center frequency is slightly shifted to the left from the targeted frequency (2 GHz) to about 1.87 GHz. This is due to the quality factor of the inductors used, which

were derived at 2.4 GHz by the foundry while this design is resonated at 2 GHz. The gain obtained is well above 10 dB, as expected along the 400 MHz bandwidth needed, starting from 1800 to 2200 MHz. The reverse isolation (S_{12}) obtained is well above the typical value which is normally -30 dB. As shown in Figure 4.26, S_{12} of the circuit gives the values ranging from about -58 to -59 dB along the 400 MHz bandwidth.

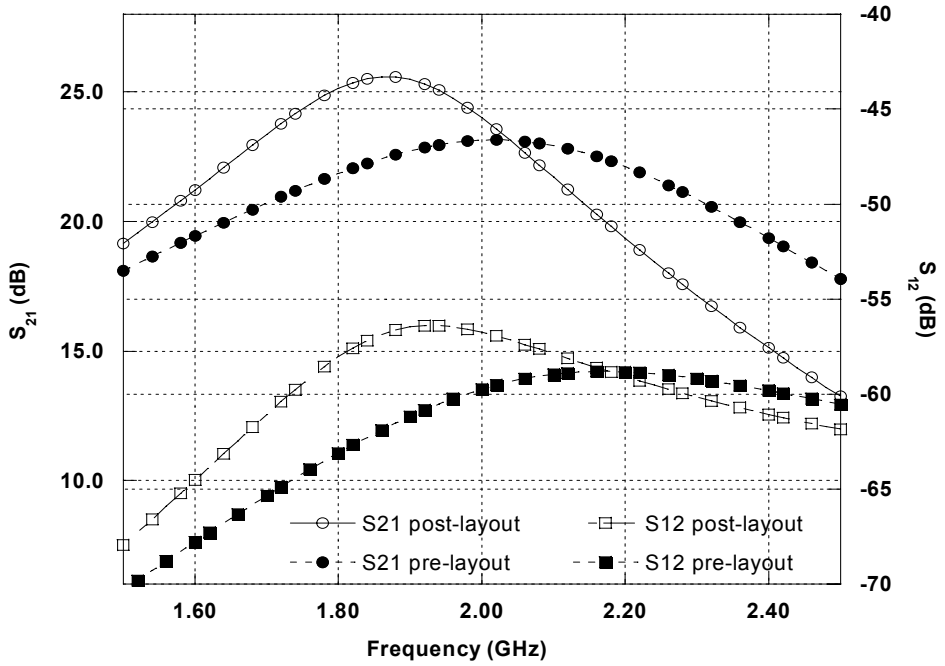

Figure 4.26: Post-layout forward gain and reverse isolation of LNA2.

The input and output return losses; S_{11} and S_{22} of the LNA are shown in Figure 4.27. For S_{11}, the value is -24.88 dB at the center frequency (slightly shifted to 1.94 GHz) and ranging from -13.78 dB to -13.08 dB along the 400 MHz bandwidth, starting from 1800 to 2200 MHz. The shifting of the center frequency is maybe attributed by unaccounted interconnect lines at the input.

For S_{22}, at the center frequency, -28.6 dB is obtained. Notice that the shifting of the center frequency is a bit worse which is centered at 1.82 GHz and cannot be avoided as the optimisation is limited by the inductors used, where their fixed values ranging from 1.65 nH to 10.7 nH with different Q values. Therefore, the optimisation can only be done by adjusting C_{D} and R_{l}. The output return loss achieved is, however, below -10 dB along the bandwidth targeted but with a slight reduction at 2.2 GHz to about -8.7 dB. This could be avoided by increasing the value of R_{l} but it will shift the center frequency a bit more.

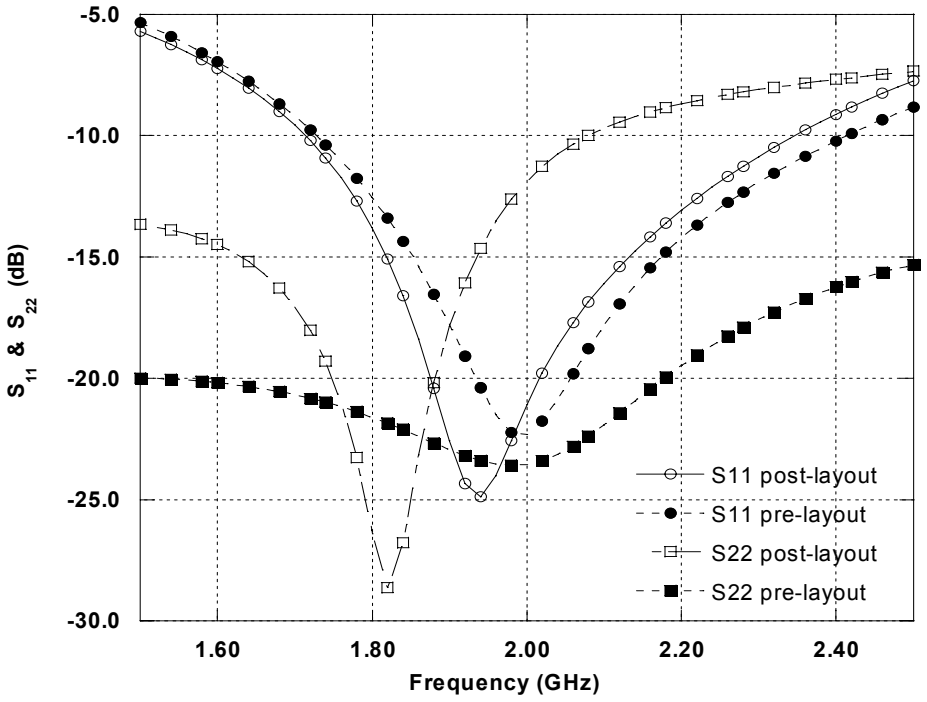

Figure 4.27: Post-layout input and output return losses of LNA2.

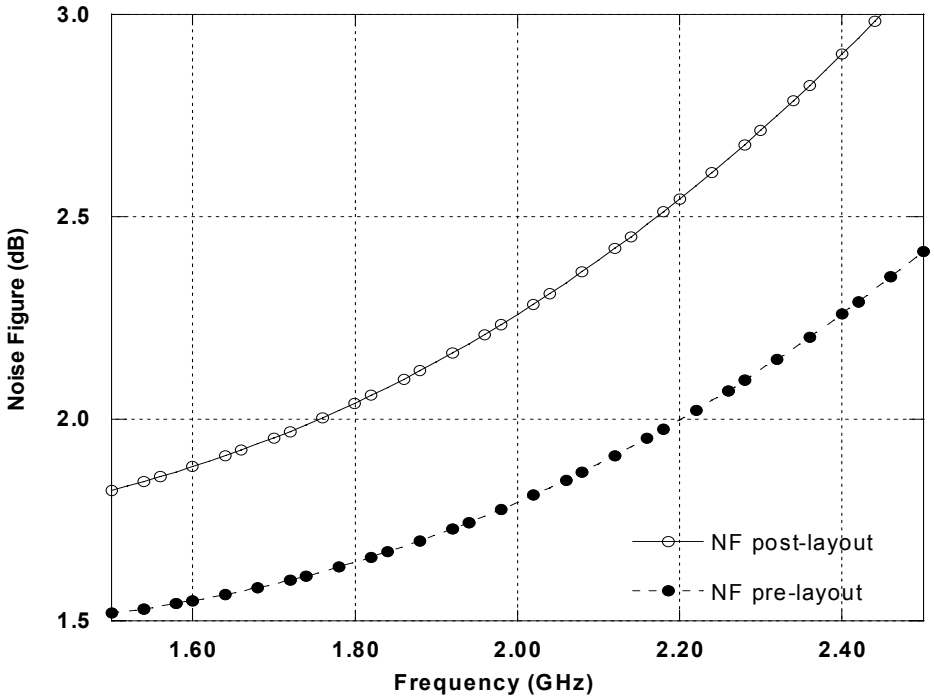

Figure 4.28: Post-layout noise figure of LNA2.

The noise figure of the circuit is around 2.26 dB for post-layout at the center frequency as shown in Figure 4.28. It can be seen that noise figures are ranging from 2.04 to 2.54 dB along bandwidth of 400 MHz. Notice that, for all specifications as in Figure 4.26 to 4.28, the results of pre-layout are also shown for comparison.

4.2.2 Multi-standard multi-band LNA4 design – 0.9 GHz with no buffer

For LNA4, the post-layout simulation results are shown in Figures 4.29 to 4.31. For power gain (S_{21}) as in Figure 4.29, the achieved value is about 10.07 dB at the center frequency. Notice that the center frequency is shifted to the left from the targeted frequency (900 MHz) to about 755 MHz. This is due to the quality factor of the inductors

used, which were derived at 2.4 GHz by the foundry while this design is resonated at 900 MHz. The reverse isolation (S_{12}) obtained is better than the typical value which is normally -30 dB. As shown in Figure 4.29, S_{12} of the circuit gives values ranging from about -51.39 to -50.99 along the 200 MHz bandwidth.

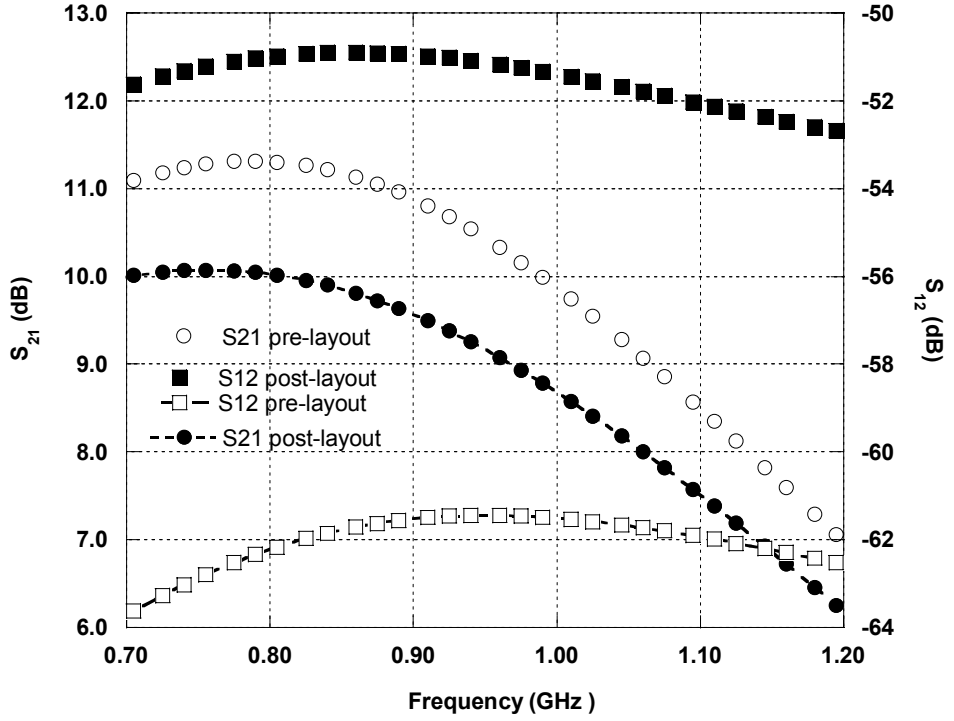

Figure 4.29: Post-layout forward gain and reverse isolation of LNA4.

The input and output return losses; S_{11} and S_{22} of the LNA are shown in Figure 4.30. For S_{11}, the value is -20.62 dB at the center frequency (slightly shifted to 895 MHz) and ranging from -12.78 dB to -12.58 dB along the bandwidth from 800 to 1000 MHz. The shifting of the center frequency is maybe attributed by unaccounted interconnect lines at the input. For S_{22}, at the center frequency, -32.97 dB (slightly shifted to 890 MHz) is obtained and ranging from -22.1 dB to -20.74 dB along the 200 MHz bandwidth. Notice

that the shift of the center frequency to 890 MHz cannot be avoided as the optimisation is limited by the inductors used, where their values ranging from 1.65 to 22.9 nH at 10 different values supplied by the foundry. Consequently, the optimisation can only be done by adjusting C_{D} and R_{l}. The output return loss (S_{22}) achieved, however, is well below -10 dB along bandwidth of 200 MHz and is good as targeted.

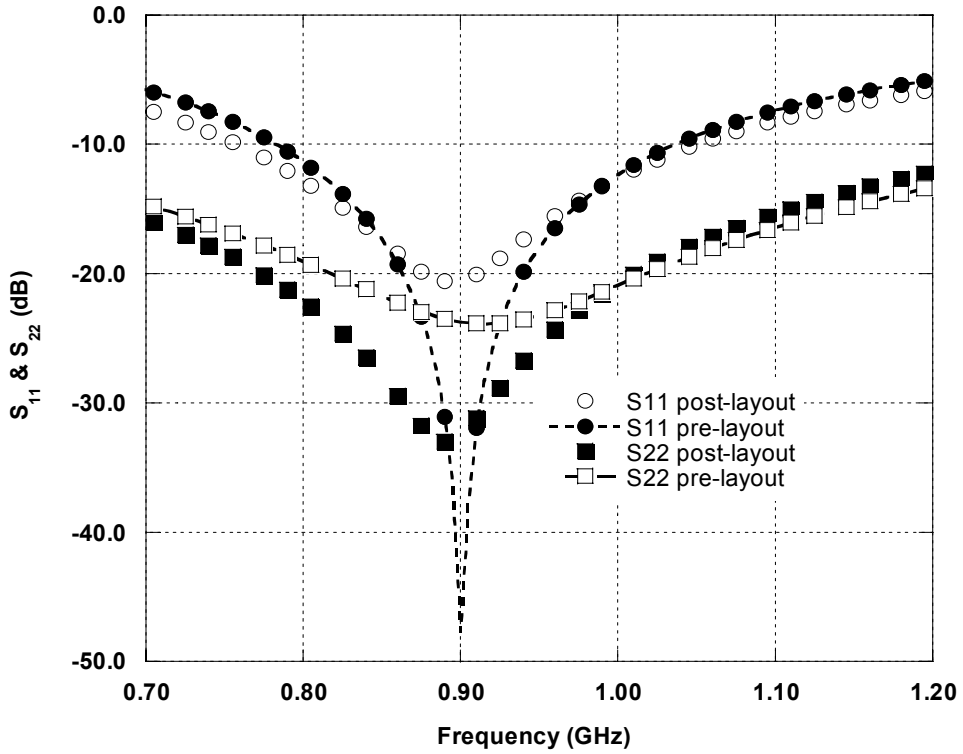

Figure 4.30: Post-layout input and output return losses of LNA4.

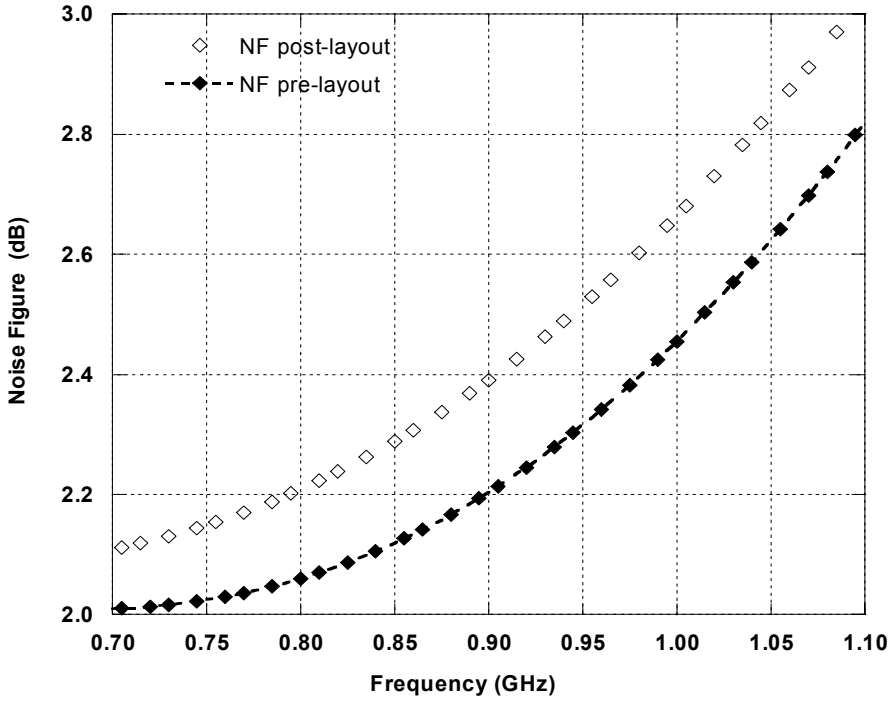

Figure 4.31: Post-layout noise figure of LNA4.

The noise figure of the circuit is around 2.39 dB at the center frequency as shown in Figure 4.31. This value considered quite well, as the inductor L_G is big which corresponds to high series resistance at the input. It can be seen that noise figures are ranging from 2.22 to 2.66 dB along bandwidth of 200 MHz. Also, notice that, for all specifications as in Figure 4.29 to 4.31, the results of pre-layout are also shown for comparison.

4.2.3 Multi-standard multi-band LNA5 design – 2 GHz with no buffer

The post-layout simulation results are shown in Figures 4.32 to 4.34. As shown in Figure 4.32, the power gain (S_{21}) is about 11.8 dB at the center frequency. Also, the

center frequency is shifted to the left from the targeted frequency (2 GHz) to about 1.7 GHz. This problem as mentioned earlier is due to the quality factor of the inductors used which were derived at different frequency while this design is resonated at 2 GHz. The gain obtained is well above 10 dB, as expected along the bandwidth needed which is about 400 MHz from 1800 to 2200 MHz both for pre and post-layout. The reverse isolation (S_{12}) obtained is better than the typical value which is normally -30 dB. Also shown in Figure 4.32, the S_{12} of the circuit which gives values ranging from about -52 to -48 dB along the interested bandwidth.

The input and output return losses; S_{11} and S_{22} of LNA5 are shown in Figure 4.33. For S_{11}, the obtained value is -41.7 dB at the center frequency (slightly shifted to 1.92 GHz) and ranging from -17.43 dB to -11.57 dB along bandwidth of 400 MHz from 1800 to 2200 MHz. The shifting of the center frequency is maybe attributed by unaccounted interconnect lines at the input. For S_{22}, at the center frequency, -13.65 dB is obtained. Notice that the shift of the center frequency is a bit increased which centered at 1.6 GHz and cannot be avoided, as the optimisation is limited by the inductors used, where their fixed values ranging from 1.65 nH to 15.8 nH with different Q values. Therefore, the optimisation can only be done by adjusting C_{D} and R_{l}. The output return loss attained, however, are below -10 dB along the bandwidth targeted but with a slight reduction at 2.2 GHz to about -9.5 dB. This could be avoided by increasing the value of R_{l} but it will shift the center frequency a bit more.

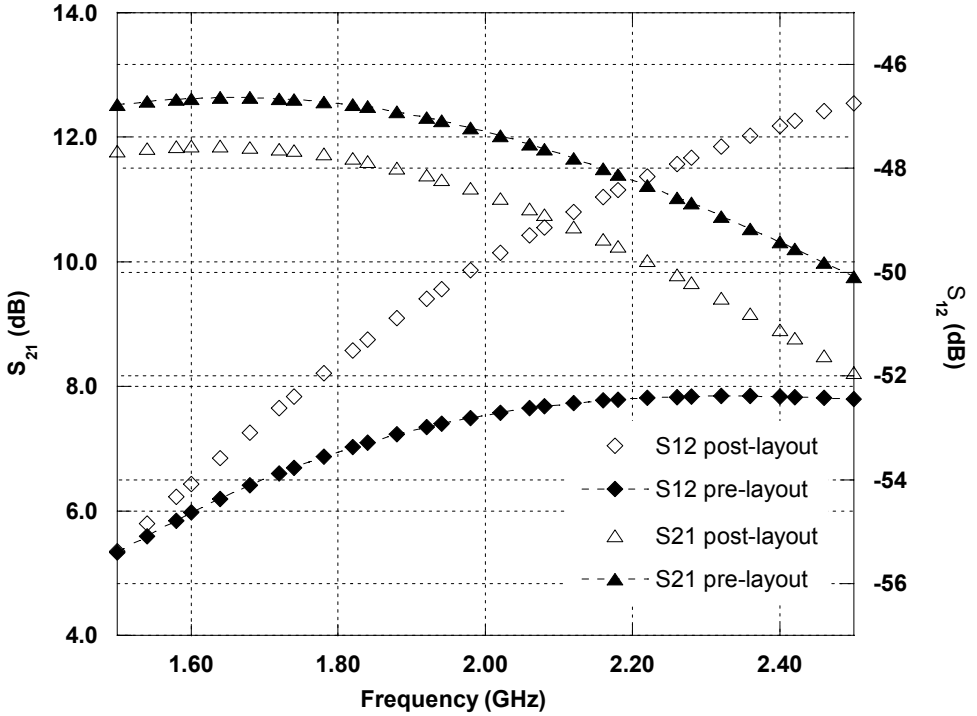

Figure 4.32: Post-layout forward gain and reverse isolation of LNA5 .

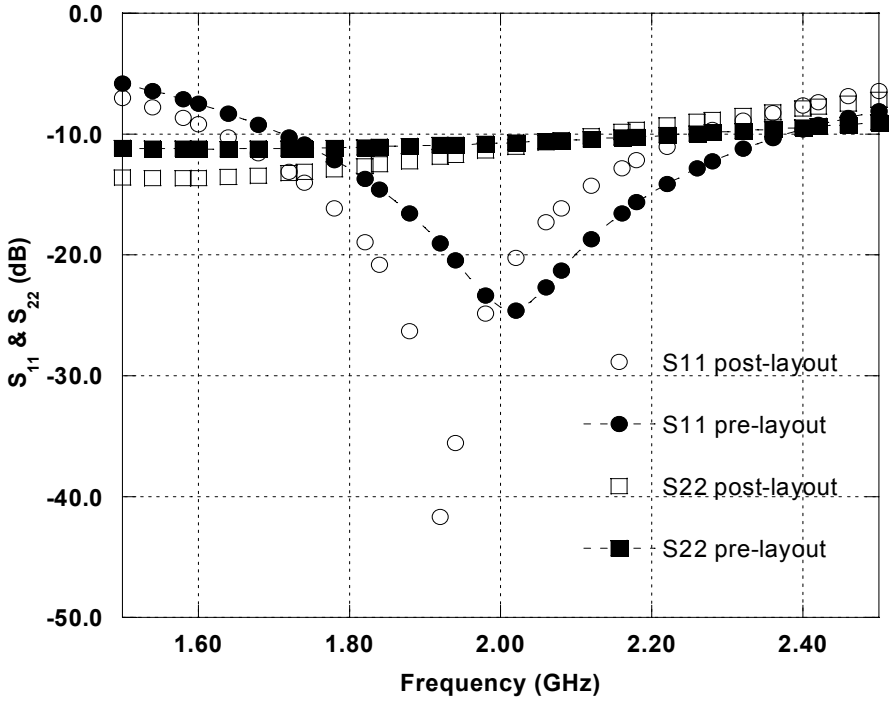

Figure 4.33: Post-layout input and output return losses of LNA5.

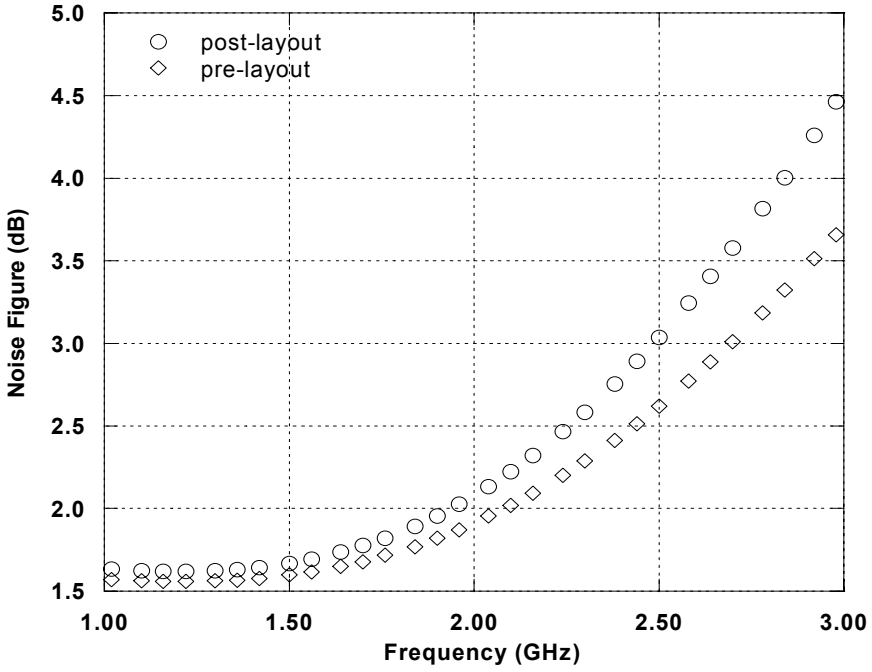

Figure 4.34: Post-layout noise figure of LNA5.

The noise figure of the circuit is about 2.08 dB at the center frequency as shown in Figure 4.34. It can be seen that noise figures are ranging from 1.86 to 2.4 dB along the bandwidth of 400 MHz.

4.3 Discussion of the results

Table 4.1 shows the performance summary of the wide band LNA1 to LNA5 as discussed in section 4.1 and 4.2.

Table 4.1: Performance summary of the wide band LNAs

	0.18 µm						0.25 µm	
	LNA2		LNA4		LNA5		LNA1	LNA3
	Pre	Post	Pre	Post	Pre	Post	Pre	Pre
$S_{21}\,(dB)$	23.2	25.6	11.3	10.07	12.6	11.8	23	12
$S_{12}\,(dB)$	- 63	- 59	- 62	- 51	- 53	- 51	- 47	- 52
$S_{11}\,(dB)$	- 35.6	- 24.9	- 47.7	- 20.62	- 24.4	- 41.7	- 25.2	- 14
$S_{22}\,(dB)$	- 26.9	- 28.6	- 23.9	-32.97	- 11.21	- 13.65	- 23	- 34
$NF\,(dB)$	1.79	2.26	2.2	2.39	1.91	2.08	0.6	0.7
$IIP3\,(dBm)$	- 7.08	n/a	+ 8.28	n/a	+ 8.4	n/a	- 5.1	+ 7.63
$P1dB\,(dBm)$	- 18.02	n/a	- 2.06	n/a	- 2.02	n/a	- 17.3	- 2.76
$Power\,(mW)$	14	14	12.8	12.8	12.2	12.2	23.75	20.8

For power gain, it shows that LNA3, LNA4 and LNA5 are having lower gain compared to LNA1 and LNA2. This could be explained by equation 3.40 in which $Z_L(s)$ is higher in LNA1 and LNA2. In other word, this is due to the fact that the technique used for output matching in LNA3, LNA4 and LNA5 utilised two inductors in parallel which yielded low net inductance in which lead to lower $Z_L(s)$ compared to LNA1 and LNA2. As explained in [92], (4.1) shows the ratio between the gate inductor and source inductor which is proportional to the gain of the LNA.

$$\text{Gain} = \frac{v_{out}}{v_{in}} = \frac{-g_m s L_D}{s L_S g_m} = -\frac{L_G}{L_S} \tag{4.1}$$

Therefore, LNA3, LNA4 and LNA5 are experiencing lower gain compared to LNA1 and LNA2 due to the lower inductance at the load. But these gains, however, are still within targeted values (see Chapter 2, Table 2.5).

In term of noise figure, LNA2, LNA4 and LNA5 are having higher NF compared to LNA1 and LNA3. This could be easily explained as LNA2, LNA4 and LNA5 are designed using real inductors compared to LNA1 and LNA3 which are designed using ideal inductors. Therefore, the series resistance of the inductors were taken into account in the calculation of the NF of the LNA2, LNA4 and LNA5, while in LNA1 and LNA3 no series resistance is involved. This situation could be observed by using equation 3.42. In addition, Figure 4.35 shows the simulation results of the noise figure based on different values of the source inductors, L_S. This simulation shows that when a lower value of L_S is used, a lower NF is obtained. However, referring to the design of wide band LNAs as in Table 4.1, the optimum values exist for the designs are based on the trade-off made in order to achieve the targeted LNA's specifications (see Table 2.5). Also, Figure 4.35 shows the effect of L_S used on the gain of the LNA4 as explained in previous paragraph. However, the effect of L_S on the gain is much greater than on the NF. Therefore, the value of L_S has to be picked carefully for particular design.

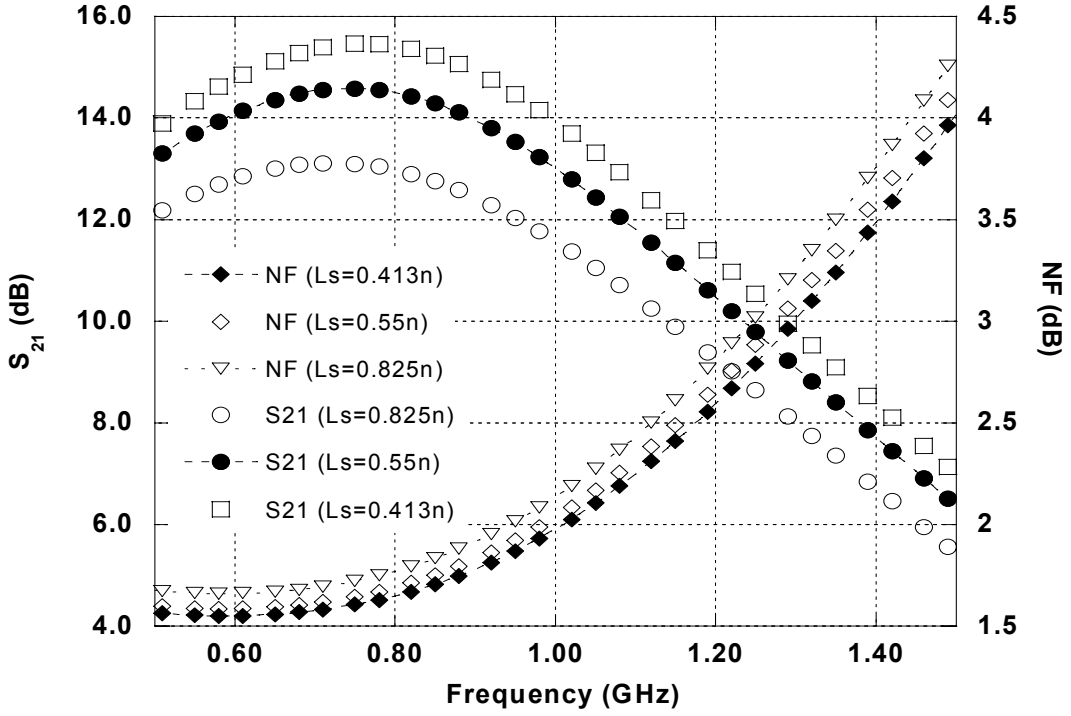

Figure 4.35: Noise figure simulation with different values of L_S .

For input and output return losses (S_{11} and S_{22}**),** as shown in Table 4.1**,** the achieved values are well below -10 dB but with the exception at certain frequency of the interested bandwidth. For instance, for post-layout simulation of LNA5, the achieved value is about -9.5 dB at 2.2 GHz for S_{22}. In relation to output return loss (S_{22}**),** Figures 4.36 and 4.37 show a simulation results of the output return loss using different values of R_1 and L_1 as well as their effect on the gain. In these figures, the effect of R_1 and L_1 on S_{22} and gain are clearly determines the performance of the LNA. Therefore, a careful step in determining the optimum values of R_1 and L_1 is important. In addition, these simulation results refer to the technique used for output matching in LNA3, LNA4 and LNA5 which linked to the equation 3.46.

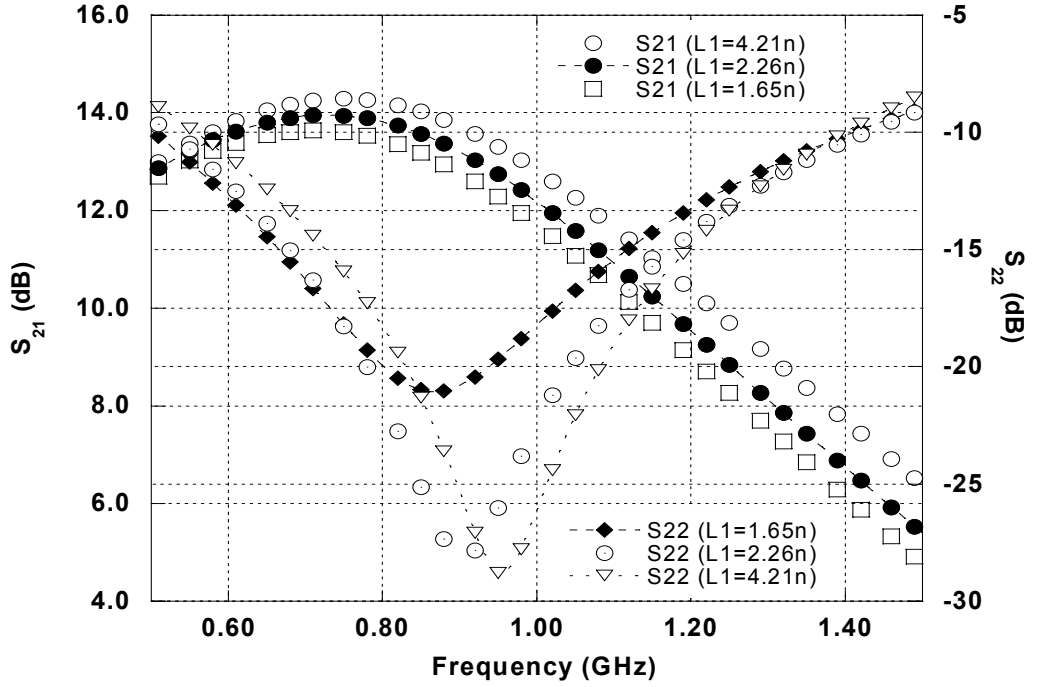

Figure 4.36: Output return loss (S_{22}): fix R_1 but different values of L_1 .

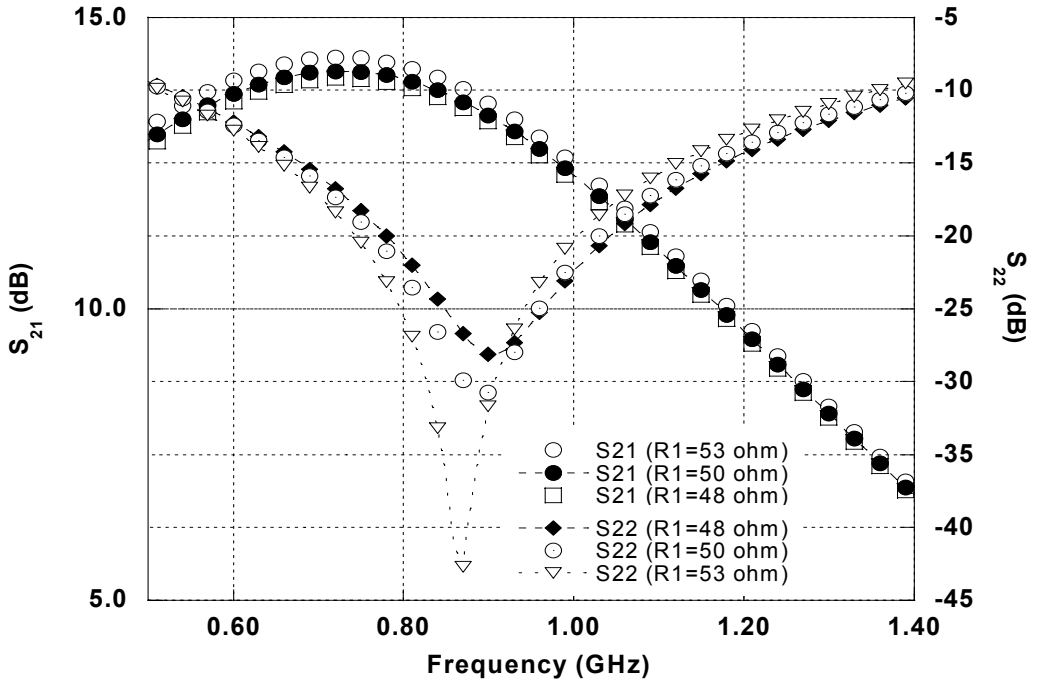

Figure 4.37: Output return loss (S_{22}): fix L_1 but different values of R_1 .

Regarding linearity, $IIP3$ and $P1dB$, the achieved values are much better and exceeding the specifications using the technique introduced in LNA3, LNA4 and LNA5 compared to LNA1 and LNA2 which use the buffer technique. For instance, based on the same technology, in LNA2, the achieved $IIP3$ is about -7.08 dBm while in LNA5, +8.4 dBm is achieved. In LNA2, the linearity is primarily limited by M_3, due to the gain which precedes it [25]. But, in LNA5, no buffer is used, thus producing a better linearity. In addition, the achieved values for linearity are always a representation of the trade-off made between power consumption, impedance matching and linearity requirements of the LNA.

4.4 Conclusion

This chapter presented the results and discussion of the pre-layout and post-layout of the wide band LNA1 to LNA5. Despite little deviations in some results, the overall results obtained in the pre and post-layout show good agreement with the targeted specifications, which were highlighted in Chapter 2 (see Table 2.5). In addition, the results achieved are representation of the trade-off made between s-parameters, linearity, NF and power consumption.

CHAPTER 5:

MEASUREMENT RESULTS OF THE FABRICATED LNAs

5.0 Introduction

A detailed results and discussion on the pre-layout and post layout simulations were presented in Chapter 4. Also, the successful designs of 5 LNAs based on wide band approach using IDCS technique were presented.

It has been stated that proper characterisation of RF circuits is an important step within the design process. The designed devices based on the technology library provided by the foundry have been fabricated. The measurements of the fabricated LNAs verify if the simulations hold and the ICs hardware have been fabricated without significant process variations. Measurement equipment with performances beyond that of the device under test (DUT) is required, that make the measurement of high-speed RF circuits challenging and expensive [93].

This chapter presents the measurement results of the fabricated LNA2, LNA4 and LNA5 which were designed and implemented using 0.18 μm CMOS technology provided by

the foundry. All the measurements were done on-chip by using multiple biasing voltages for comparison. Please notice that, only LNA2, LNA4 and LNA5 were fabricated and measured in this work whereby LNA1 and LNA3 (based on 0.25 µm CMOS technology) were not fabricated as access to fabrication using 0.25 µm CMOS technology is not provided by the foundry. This chapter is organised as follow: Section 5.1 starts with a measurement setup. Section 5.2 then presents the measurement results of the fabricated LNAs. A discussion about the measurement results is given in Section 5.3 and conclusion is made in Section 5. 4.

5.1 Measurement Setup

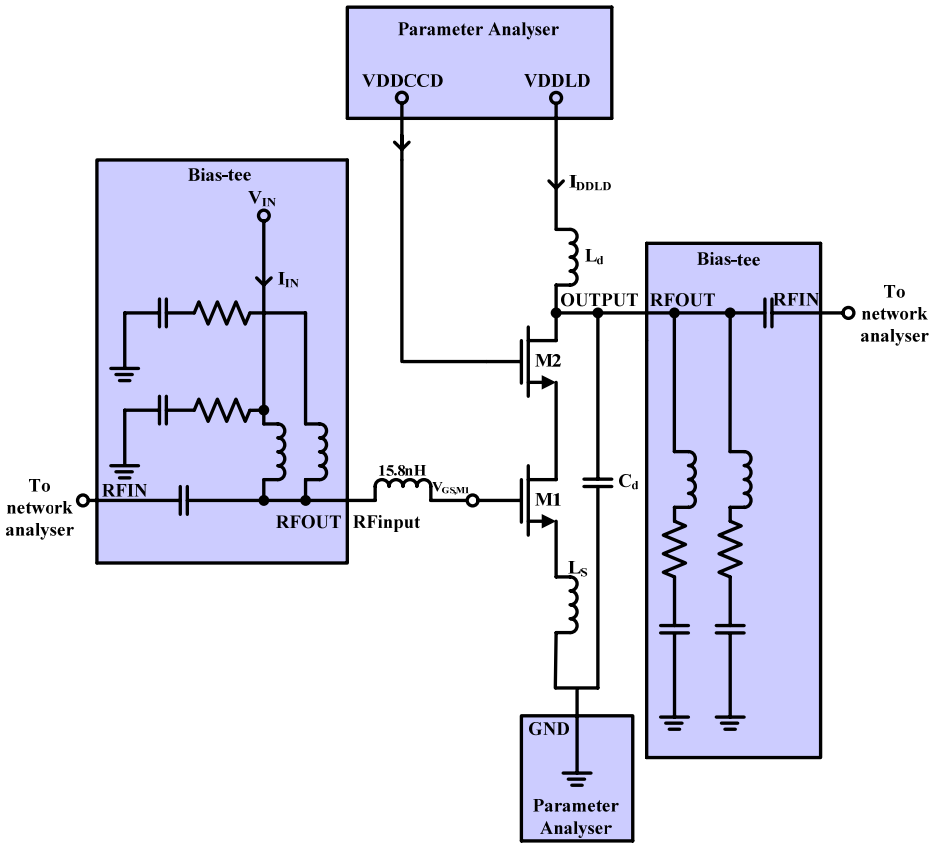

Figure 5.1: Measurement strategy [95].

Gain, return loss, and P1dB of the LNA can be measured using a standard scalar S-parameters test set [94]. Figure 5.1 shows the measurement setup which was carried out at CEDEC using ground-signal-ground (GSG) probe at 150 µm pitch [95]. Three different biasing voltages were applied as a bias-tee.

5.2 Measurements results of the fabricated LNAs

As stated earlier, the measurement strategy was done by using the bias tee for biasing the LNA. Three biasing voltages which are 0.6, 0.65 and 0.7V have been used for the purpose of the measurement. However, the testing set (i.e. biasing voltages used) for each LNA is different based on the arrangement made with CEDEC (test and measurement center Malaysia).

5.2.1 Multi-standard multi-band LNA2 IC measurement – 2 GHz with buffer

In this testing, (the DC measurement, s-parameters and linearity), only one biasing voltage (V_{IN}) was used which is 0.7V. On the other hand, three biasing currents for buffer, I_{DC} (see LNA2 circuit in Chapter 3) were applied to see how this current play a role in changing the gain and output impedance matching for the circuit as seen in Figure 5.2 to 5.10.

For DC measurement, the results are shown in Figure 5.2. In this measurement, interestingly, it shows that the increment of the current of the buffer circuit (I_{dc}) has a

linear effect on the load current (I_{load}). Therefore, the buffer used in LNA2 is not suitable for low power LNA design, as it produces unwanted power in the circuit and should be avoided. Furthermore, this effect is not seen in the pre-layout and post layout simulation and is not expected.

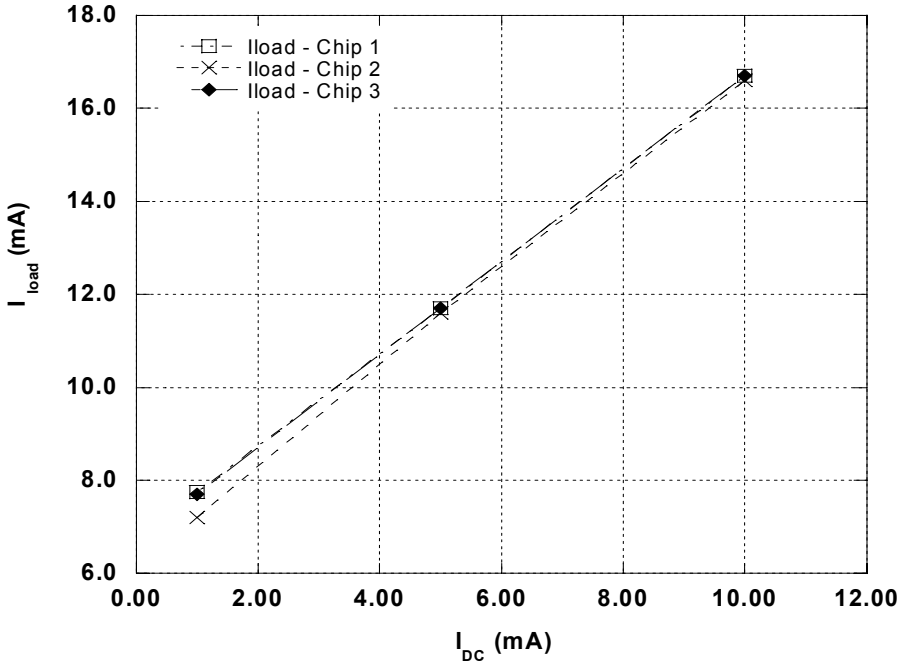

Figure 5.2: Measured I_{load} versus I_{dc}.

For power gain (S_{21}), the achieved values for the three measured chips (with 1 mA of the buffer circuit current) are about 8.64 to 9.16 dB at the center frequency as shown in Figure 5.3 and Tables 5.1 and 5.2 respectively. These achieved values reflect the optimum performance of the circuit. In other words, the gain obtained is the manifestation of the best s-parameter (S_{21}) in relation with the other s-parameters achieved for the LNA2. For instance, if more current injected in the buffer circuit, i.e. the

S_{11} achieved will no longer considered as the optimum value for the LNA2. This matter will be explained later in the following paragraphs. For the achieved S_{21}, notice that the center frequency is shifted to the left from the targeted frequency (2 GHz) to about 1.8 GHz for all the measured chips. This is due to the quality factor of the inductors used, which are derived at 2.4 GHz by the foundry while this design is resonated at 2 GHz. Meanwhile, Figures 5.4 and 5.5 show the achieved values for the gain with different bias current for the buffer circuit of LNA2. Notice that the increment in the I_{dc} caused the gain to increase. The increase of the gain could be explained by the increment in the load current as depicted in Figure 5.2.

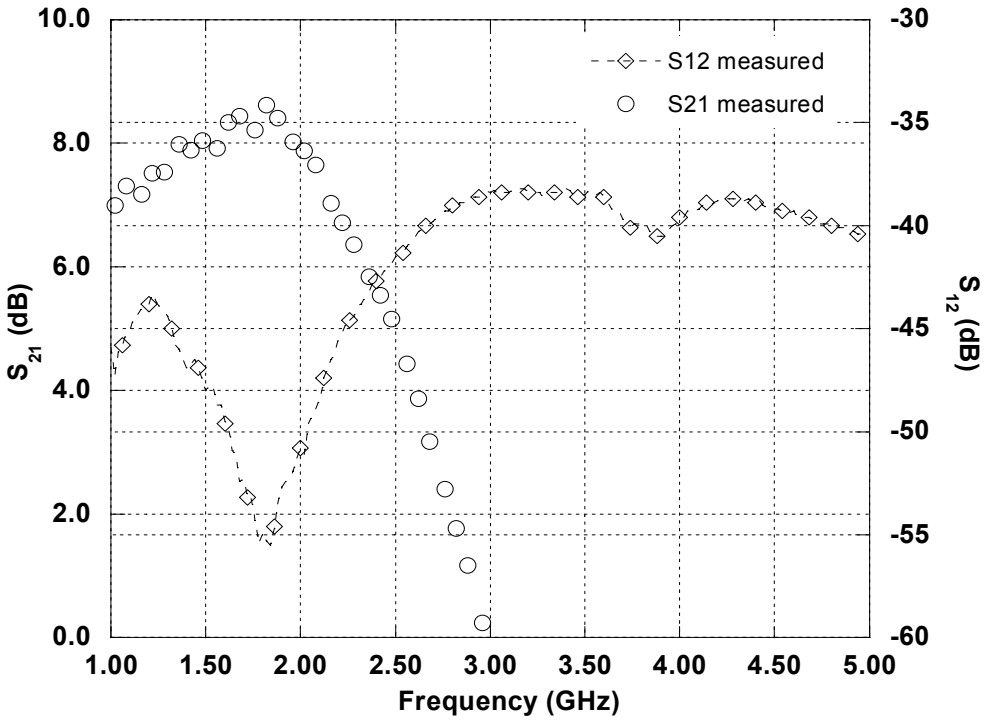

Figure 5.3: Forward gain and reverse isolation of LNA2 with I_{dc} =1mA.

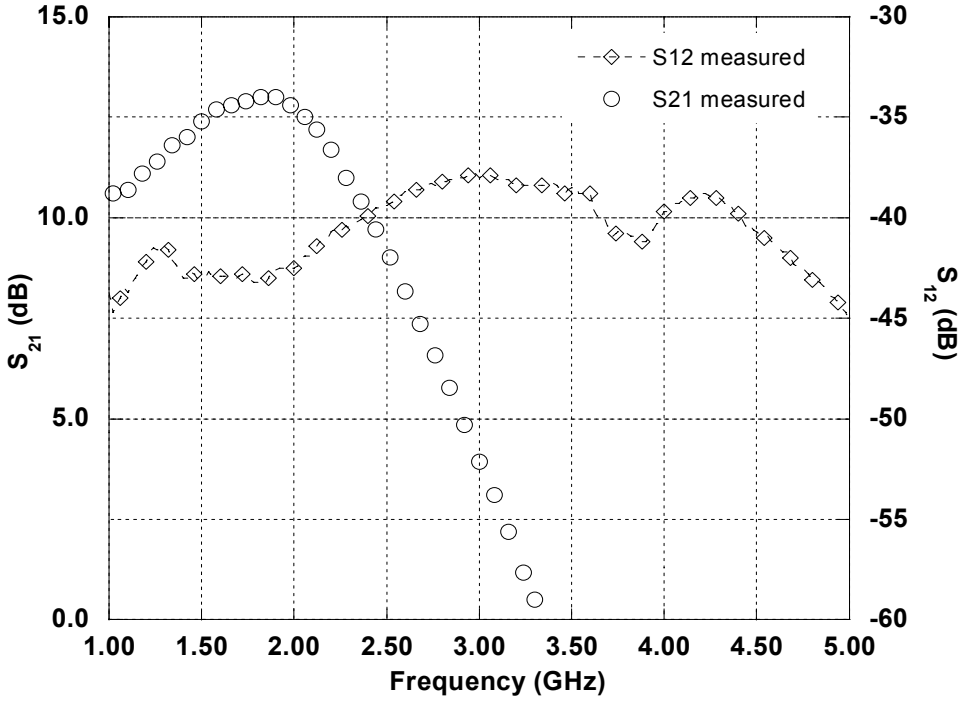

Figure 5.4: Forward gain and reverse isolation of LNA2 with I_{dc} =5mA.

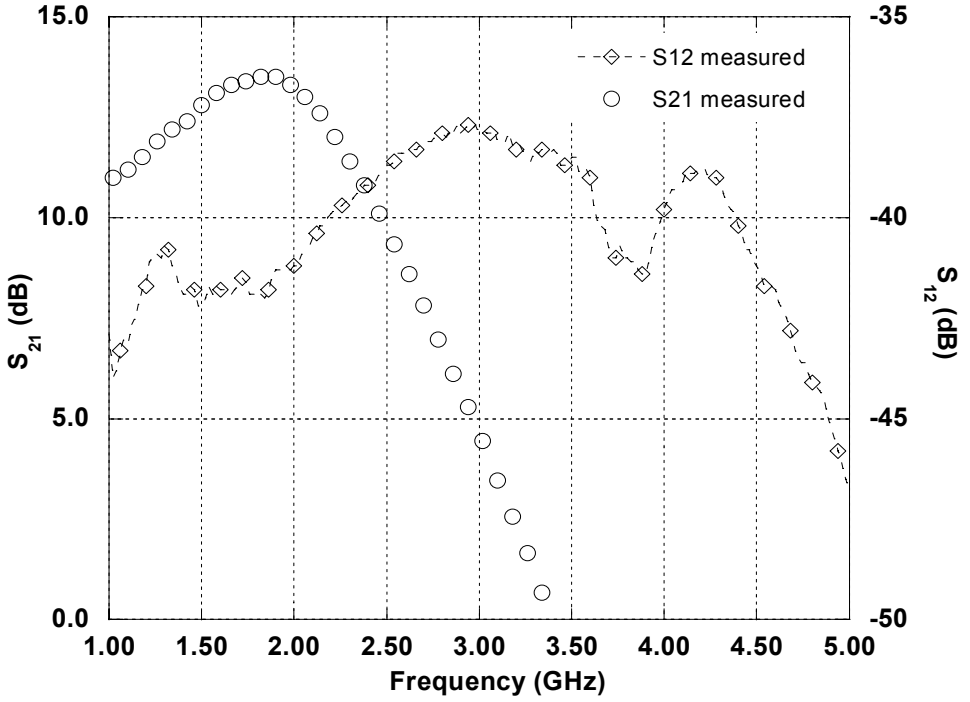

Figure 5.5: Forward gain and reverse isolation of LNA2 with I_{dc} =10mA.

The reverse isolation (S_{12}) obtained are better than the typical value which is normally range between -20 to -30 dB for all the measured chips. As shown in Figure 5.3 to 5.5, S_{12} of the circuits gives values ranging from about -55 to -40 dB along the interested bandwidth.

For the optimum values of the input and output return losses; S_{11} and S_{22} of the LNA, the results are shown in Figure 5.6. For S_{11}, the obtained value is -34.5 dB at the center frequency (slightly shifted to 2.06 GHz) and ranging from -21.8 dB to -16.6 dB for 1800 to 2200 MHz.. The shift of the center frequency maybe due to the unaccounted interconnects lines at the input. For S_{22}, at the center frequency (slightly shifted to 2.03 GHz), -26.4 dB is obtained and ranging from -21.7 dB to -20.2 dB along the interested bandwidth.

In the meantime, Figures 5.7 to 5.8 and Tables 5.1 to 5.2 show the results of S_{11} and S_{22} measured with different bias of the buffer circuit. The achieved values for the S_{22} are below the target of -10 dB and therefore is not acceptable for the circuit. The reason for more current injected to the circuit is to improve the linearity performance of the LNA2 but by doing that, low values of S_{22} are obtained. The increase in the linearity could be seen later in the following results explanation due to the increase in the buffer current. In other words, the trade-off has been made to achieve the best performance of the circuit.

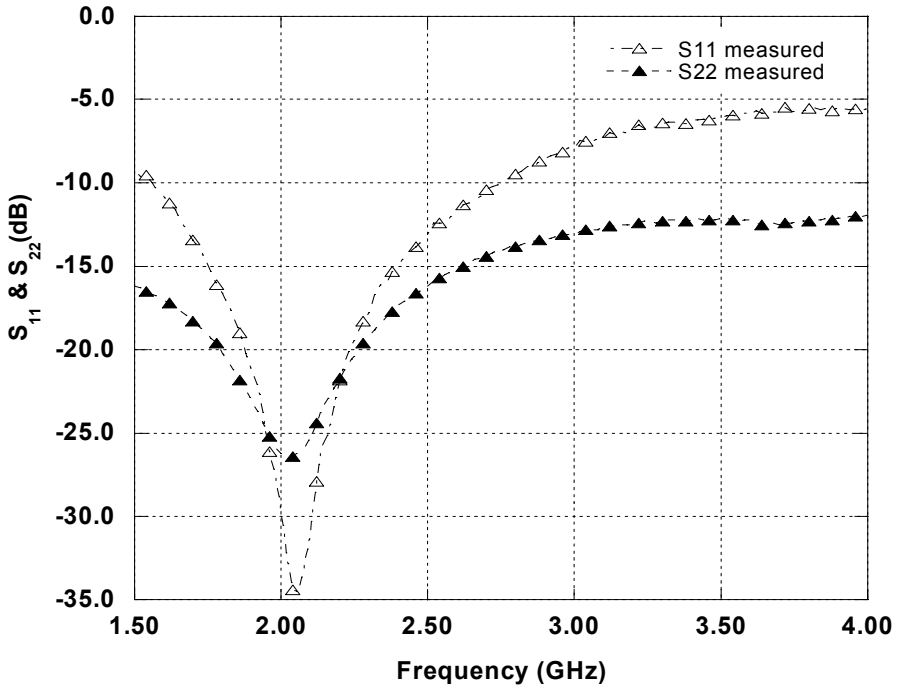

Figure 5.6: Input and output return losses of the LNA2 with I_{dc}=1mA.

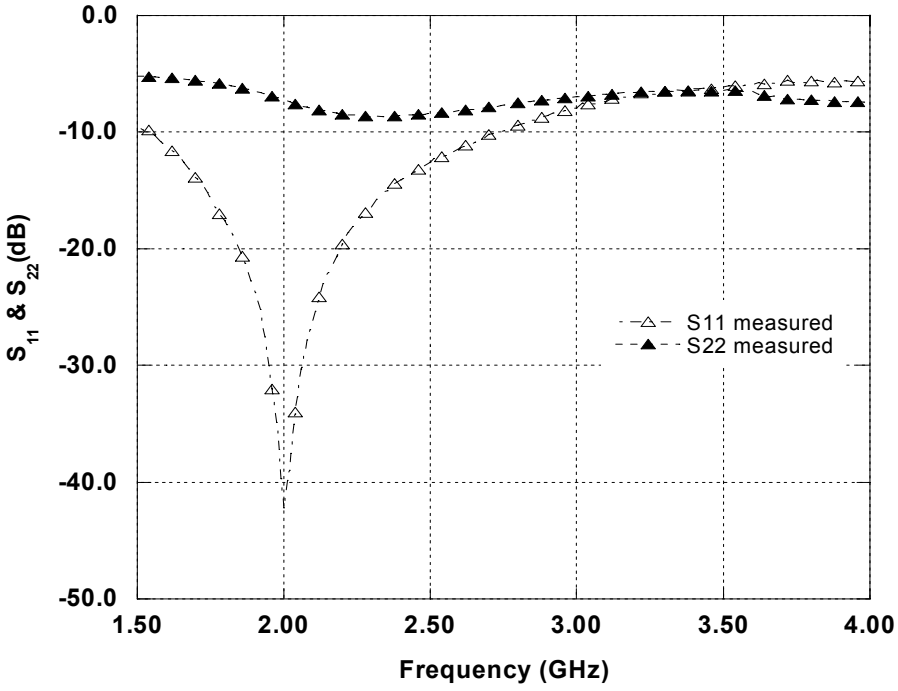

Figure 5.7: Input and output return losses of the LNA2 with I_{dc}=5mA.

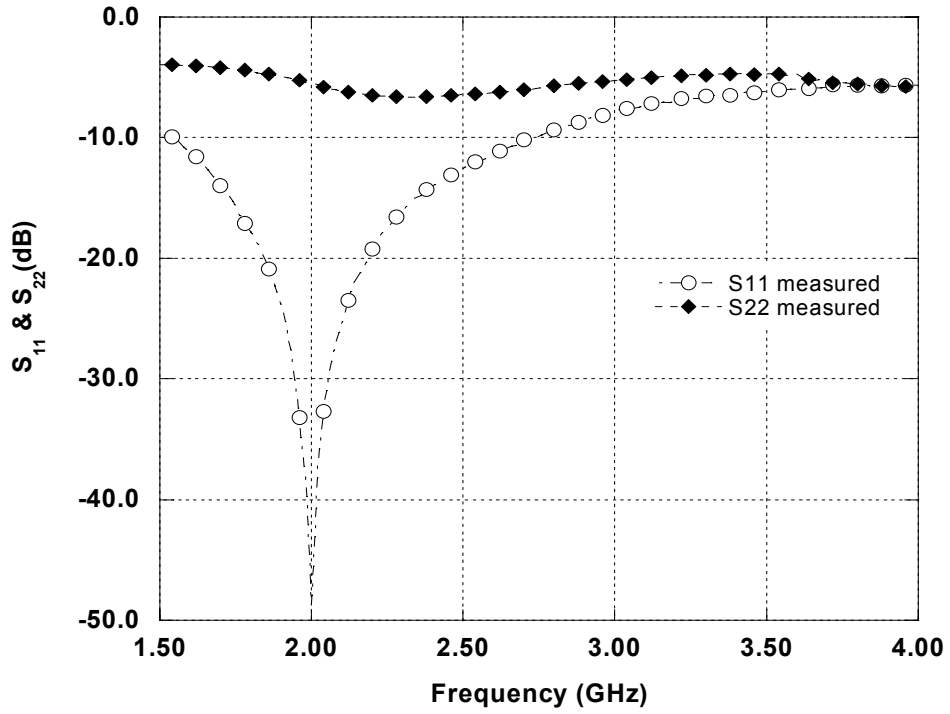

Figure 5.8: Input and output return losses of the LNA2 with I_{dc}=10mA.

Table 5.1: Performance summary of the measurement results for chip 2 of the LNA2.

	Chip 2		
	1mA	**5mA**	**10mA**
$S_{21}\ (dB)$	8.7@1.8 GHz	13.4@1.92 GHz	14.1@1.9 GHz
$S_{12}\ (dB)$	- 33.3@1.54 GHz	- 31.65@1.88 GHz	- 32.7@2.14 GHz
$S_{11}\ (dB)$	- 28.8@2.14 GHz	- 37@2.14 GHz	- 46.4@2.12 GHz
$S_{22}\ (dB)$	- 31.9@2.12 GHz	- 10.4@2.34 GHz	- 7.8@2.34 GHz

Table 5.2: Performance summary of the measurement results for chip 3 of the LNA2.

	Chip 3		
	1mA	**5mA**	**10mA**
$S_{21}\ (dB)$	9.16@1.8 GHz	13.8@1.72 GHz	14.3@1.72 GHz
$S_{12}\ (dB)$	- 31.7@2.24 GHz	- 29.2@2.88 GHz	- 28.6@2.88 GHz
$S_{11}\ (dB)$	- 24.9@2.26 GHz	- 27.6@2.18 GHz	- 27.7@2.18 GHz
$S_{22}\ (dB)$	- 32.8@1.82 GHz	- 10.5@2.08 GHz	- 8.5@2.08 GHz

For the linearity requirement, the achieved $IIP3$ is about -1.2 dBm and is shown in Figure 5.9. While in Table 5.3, the corresponding values for the $IIP3$ using different values of the buffer current are shown. For $P1dB$, the achieved value is -11.8 dBm as shown in Figure 5.10, and in Table 5.3, the corresponding values for the $P1dB$ using different values of the buffer current are shown.

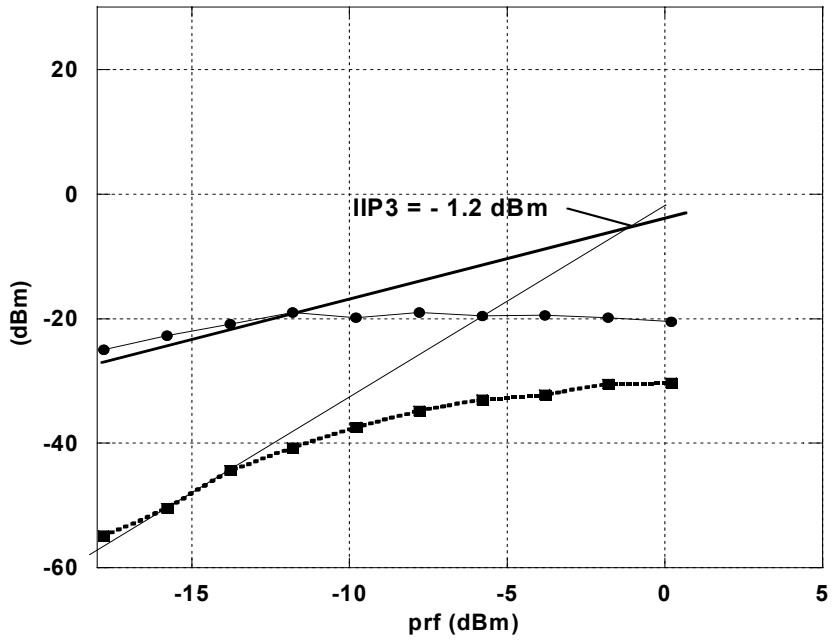

Figure 5.9: *IIP3* of LNA2 with I_{dc}=1mA.

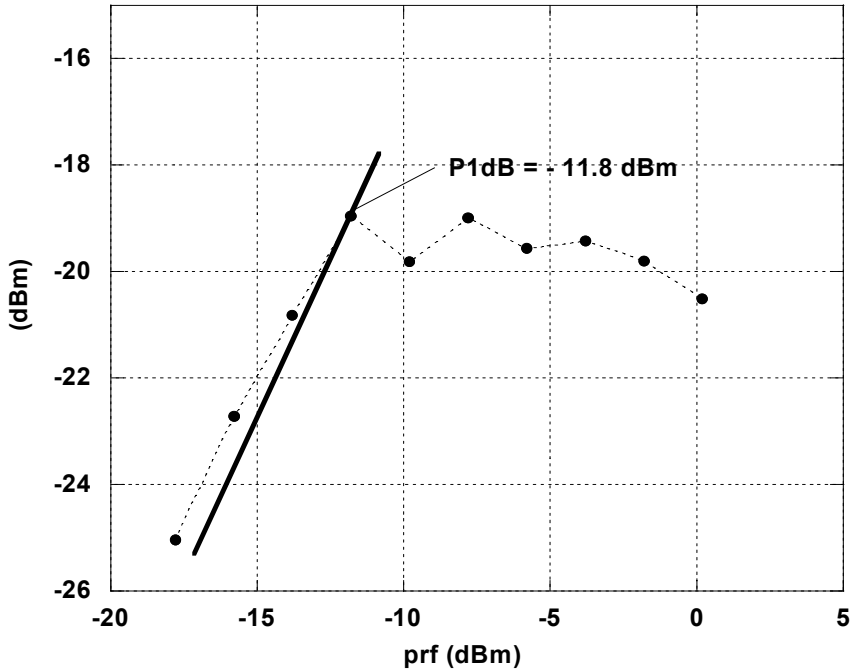

Figure 5.10: *P1dB* of LNA5 with I_{dc}=1mA.

Table 5.3: Linearity performance summary of the other current bias for LNA2

	$IIP3$ (dBm)	$P1dB$ (dBm)
5 mA	+ 2.5	- 7.8
10 mA	+ 4.5	- 5.5

5.2.2 Multi-standard multi-band LNA4 IC measurement – 0.9 GHz with no buffer

In this LNA4 testing, for the DC measurement and s-parameters, three different biasing voltages were used for LNA4, while for linearity, only one biasing has been used.

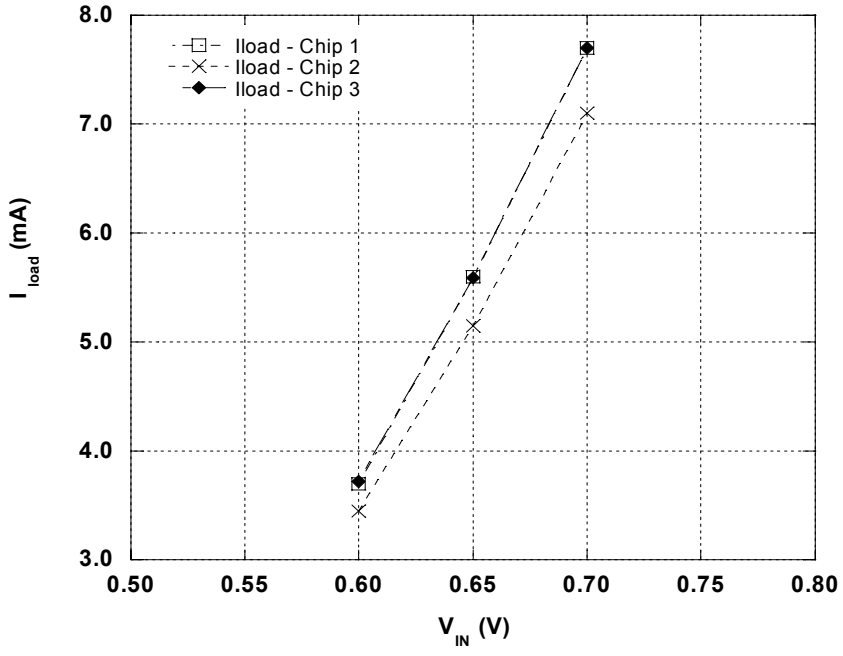

Figure 5.11: Measured I_{load} versus V_{IN} (bias) for LNA4.

The DC measurement results are shown in Figure 5.11. For this measurement, three different voltages of the bias-tee were used. The result shows the linear characteristic of I_{load} versus V_{IN}.

The optimum results for s-parameters are shown in Figure 5.12. For power gain (S_{21}), the achieved value is about 7.4 dB at the center frequency, obtained at 0.7V bias. The center frequency is however, shifted to the left from the targeted frequency (900 MHz) to about 661 MHz. This is due to the quality factor of the inductors used, which are derived at 2.4 GHz by the foundry while this design is resonated at 2 GHz. The other contribution to the shifting is because of the unaccounted parasitic of the passive devices used i.e. capacitors and inductors. For other biasing settings as in Figures 5.13 to 5.14, the results obtained are; 6.5 dB for 0.65V (shifted to the left to about 661 MHz), and 5.3 dB for 0.6V (shifted to the left of about 699 MHz) respectively.

The reverse isolation (S_{12}) obtained as shown in Figures 5.12 to 5.14, are well above the typical value (along the interested bandwidth of 200 MHz) which is normally between -20 to -30 dB for all three biasing used. Furthermore, Tables 5.4 and 5.5 show the corresponding values of the measurement results of the other measured chips for S_{21} and S_{12} parameters.

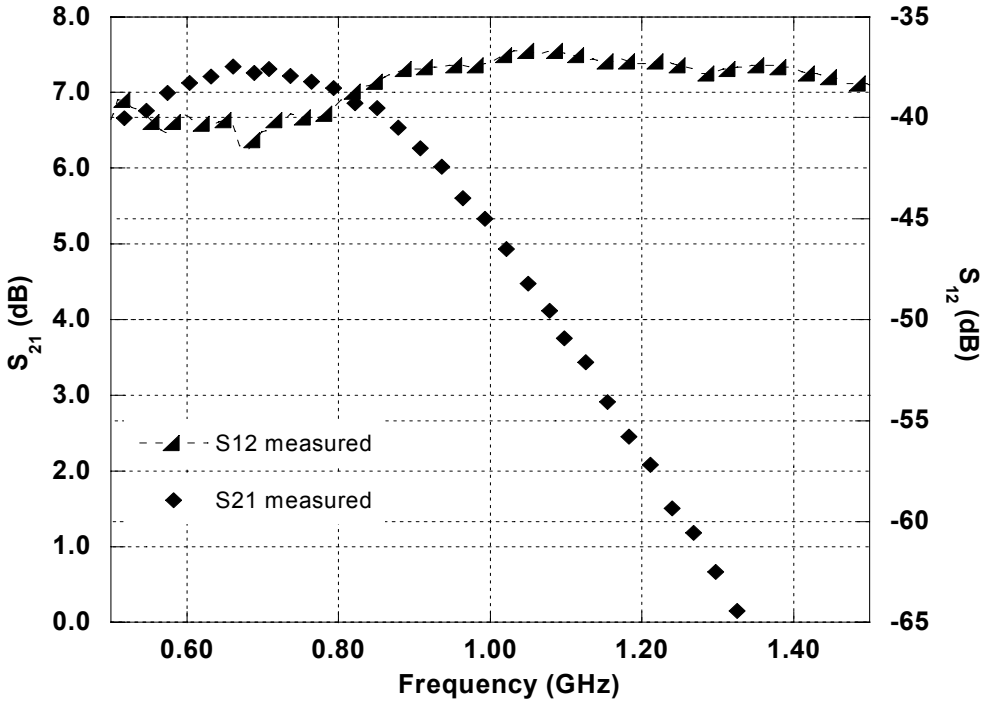

Figure 5.12: Forward gain and reverse isolation of LNA4 with 0.7V bias.

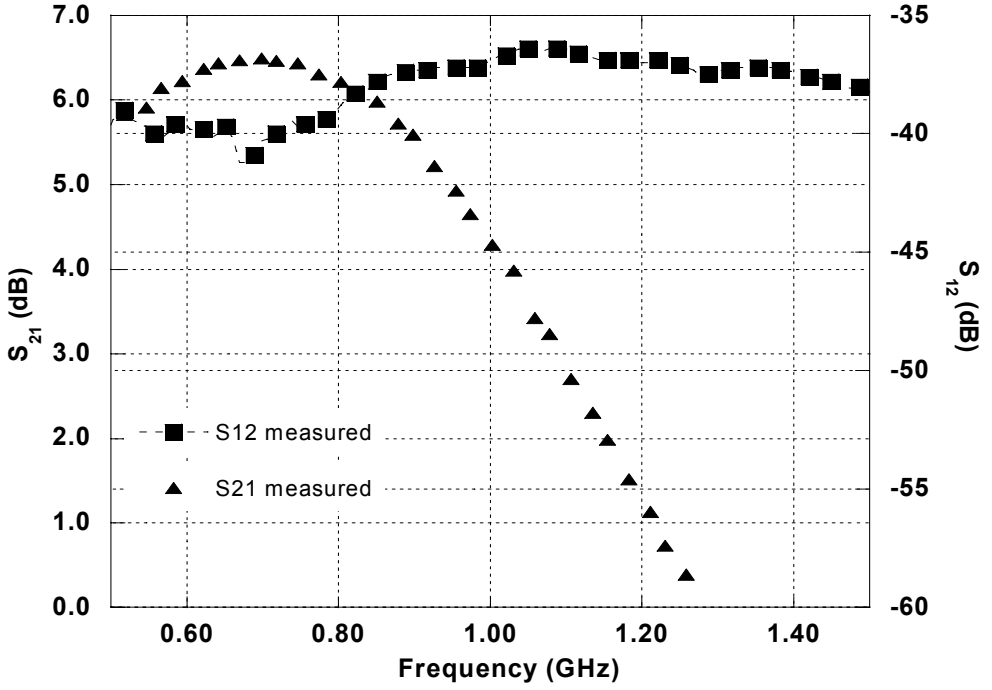

Figure 5.13: Forward gain and reverse isolation of LNA4 with 0.65V bias.

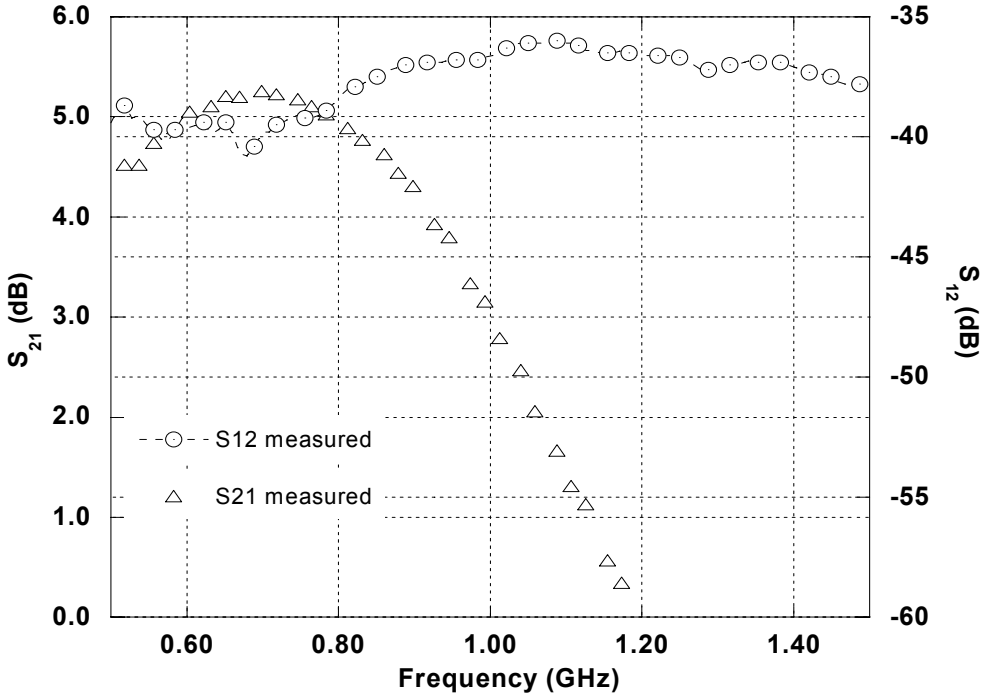

Figure 5.14: Forward gain and reverse isolation of LNA4 with 0.6V bias.

The optimum values of the input and output return losses; S_{11} and S_{22} of the LNA are shown in Figure 5.15. For S_{11}, at 0.7V, -19.4 dB is obtained with the center frequency shifted to about 870 MHz. For S_{22}, at 0.7V, -24.7 dB is obtained with the center frequency shifted to 822 MHz. Also, S_{22} values ranging from about -16.3 dB to -12.5 dB along the interested bandwidth (800 to 1000 MHz).

The other results for different biasing are shown in Figures 5.16 and 5.17. At 0.65V, for S_{11}, the obtained value is -17.9 dB (center frequency shifted to 851 MHz). Then, for 0.6V bias, -16 dB is obtained for S_{11} with a shifted center frequency of 841 MHz. Then, for 0.65V bias, the obtained S_{22} is -24.5 dB at the center frequency (shifted to 822

MHz) while for 0.6V bias, the obtained S_{22} is -24.2 dB at the center frequency (shifted to 822 MHz).

Regarding the center frequencies, the frequency shift is maybe due to the unaccounted interconnect lines and parasitic of the passive devices used as well as the element of quality factor of the inductors used, where their fixed values ranging from 1.65 nH to 22.9 nH with different Q values. Therefore, for impedance matching at the input and output, the optimisation can only be made by adjusting C_{ex}, C_{D} and R_{l}. For both return losses, S_{11} and S_{22}, the achieved values are well below -10 dB as targeted along the bandwidth of 200 MHz, even though the center frequencies were shifted from 900 MHz. In addition, the measurement results of other chips are shown in Tables 5.4 and 5.5 for comparison. As could be seen in the graphs plotted and the tables presented, the reverse isolation and output return loss show rather small dependence on the drain source current compared to gain and input return loss. This is because S_{12} and S_{22} depends only on the passive components of the amplifier. The gain and input return loss are bias dependent, which means that the higher the bias current, the higher the gain and better input matching obtained.

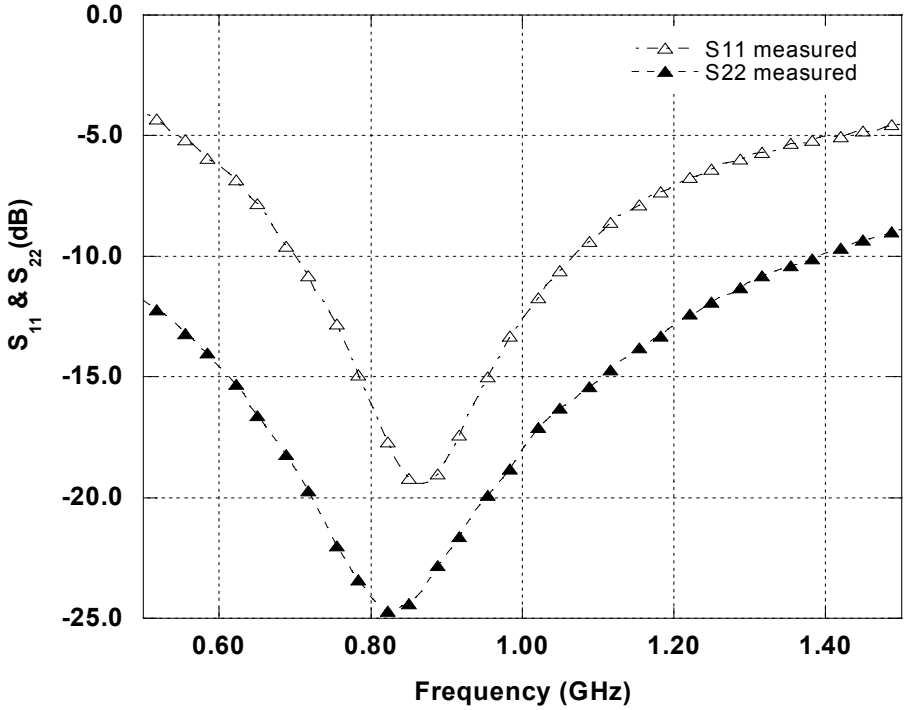

Figure 5.15: Input and output return losses of the LNA4 with 0.7V bias.

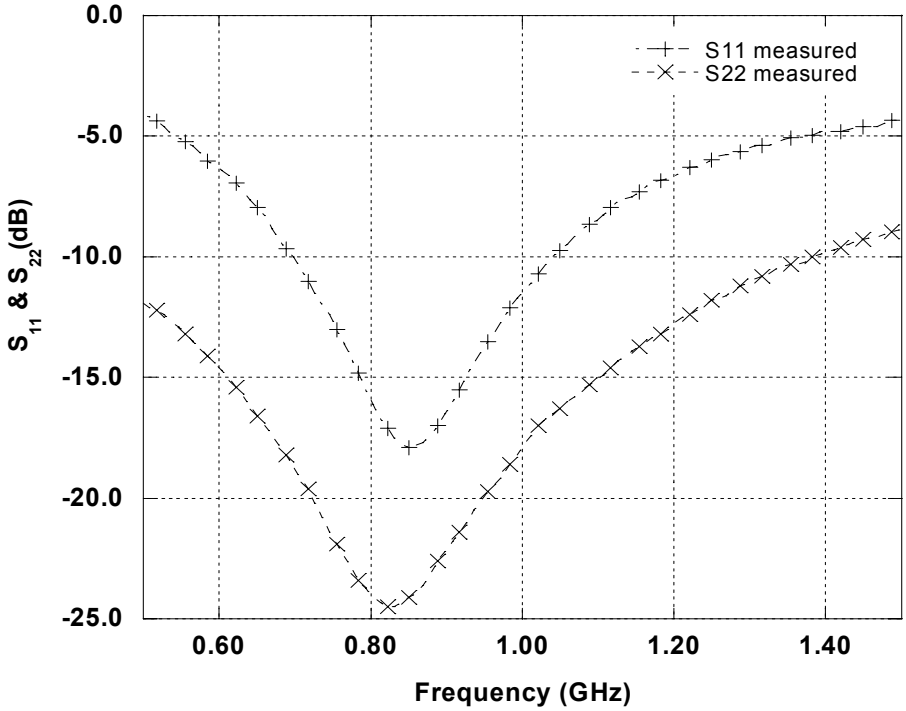

Figure 5.16: Input and output return losses of the LNA4 with 0.65V bias.

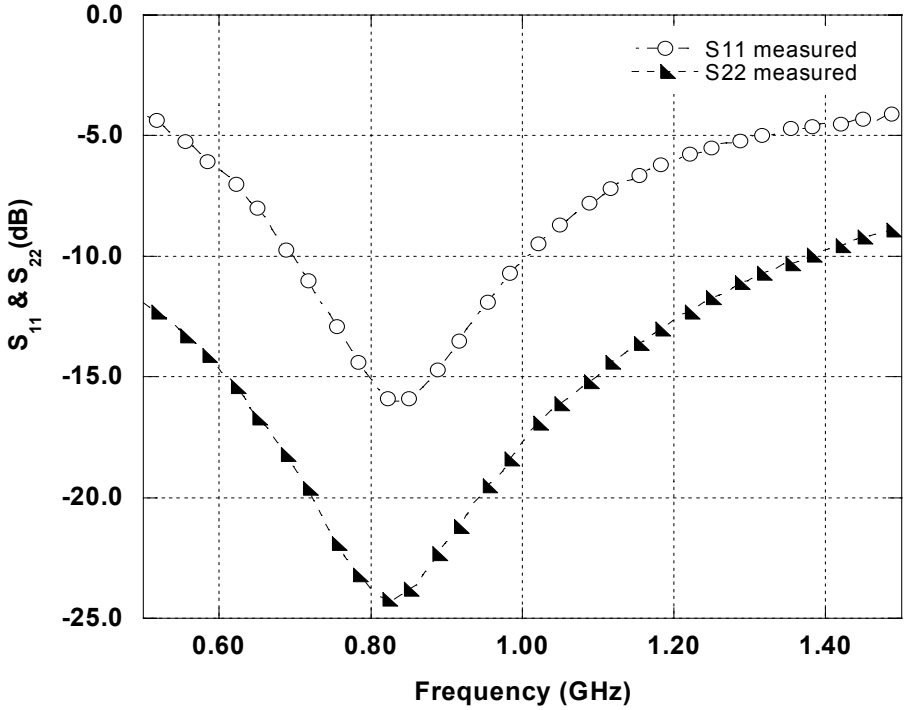

Figure 5.17: Input and output return losses of the LNA4 with 0.6V bias.

Table 5.4: Performance summary of the measurement results for chip 2 of the LNA4.

	Chip 2		
	0.6V	**0.65V**	**0.7V**
$S21\ (dB)$	3.1@718 MHz	4.4@718 MHz	5.3@689 MHz
$S12\ (dB)$	- 39@518 MHz	- 39@518 MHz	- 38@518 MHz
$S11\ (dB)$	- 16.4@813 MHz	- 17.5@851 MHz	- 19.3@851 MHz
$S22\ (dB)$	- 17.4@784 MHz	- 17.5@794 MHz	- 17.6@794 MHz

Table 5.5: Performance summary of the measurement results for chip 3 of the LNA4.

	Chip 3		
	0.6V	**0.65V**	**0.7V**
$S_{21}\ (dB)$	4.9@689 MHz	6.1@689 MHz	6.9@689 MHz
$S_{12}\ (dB)$	- 34@1.08 GHz	- 33@1.04 GHz	- 34@1.03 GHz
$S_{11}\ (dB)$	- 13.1@879 MHz	- 14.6@889 MHz	- 15.4@898 MHz
$S_{22}\ (dB)$	- 31@841 MHz	- 30.4@841 MHz	- 31.6@841 MHz

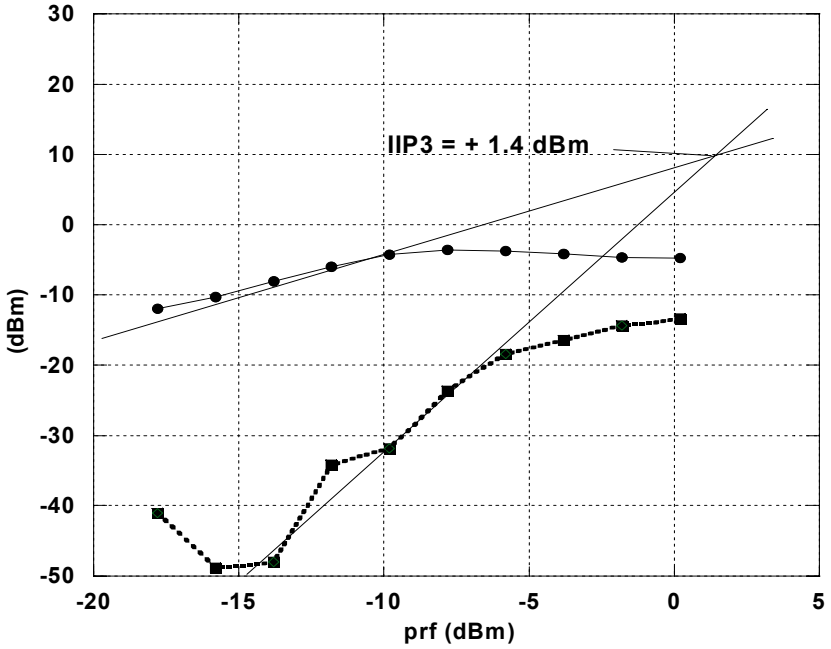

Figure 5.18: *IIP3* of LNA4 with 0.7V bias.

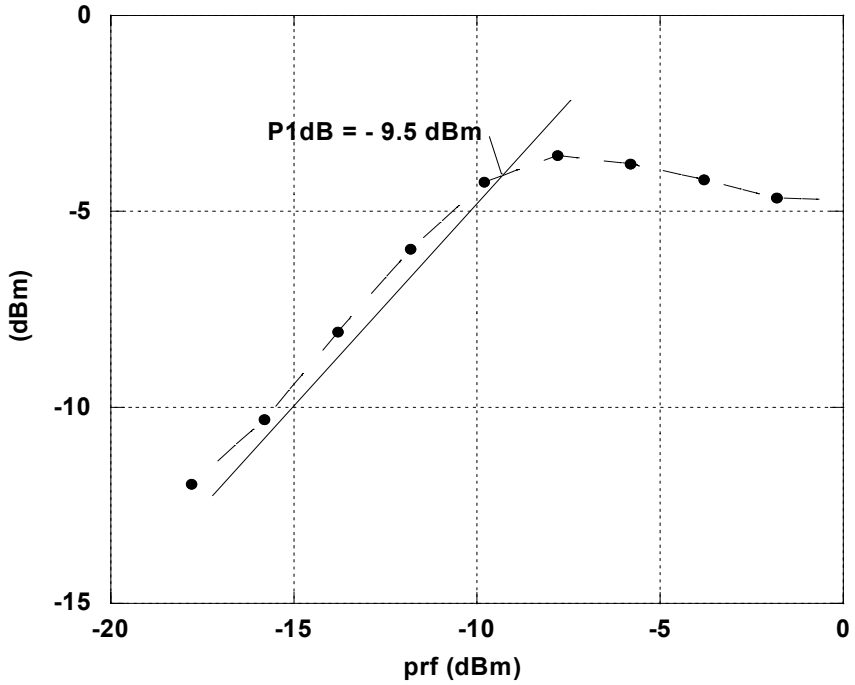

Figure 5.19: $P1dB$ of LNA4 with 0.7V bias.

Table 5.6: Linearity performance summary of the other chip for LNA4

	0.7V	
	$IIP3$ (dBm)	$P1dB$ (dBm)
Chip 2	+ 2.1	- 7.8

For the linearity requirement, the achieved $IIP3$ is +1.4 dBm and is shown in Figure 5.18. For $P1dB$, the achieved value is -9.5 dBm as shown in Figure 5.19. In Table 5.6, the performance summary of linearity of the other measured chip is presented.

5.2.3 Multi-standard multi-band LNA5 IC measurement – 2 GHz with no buffer

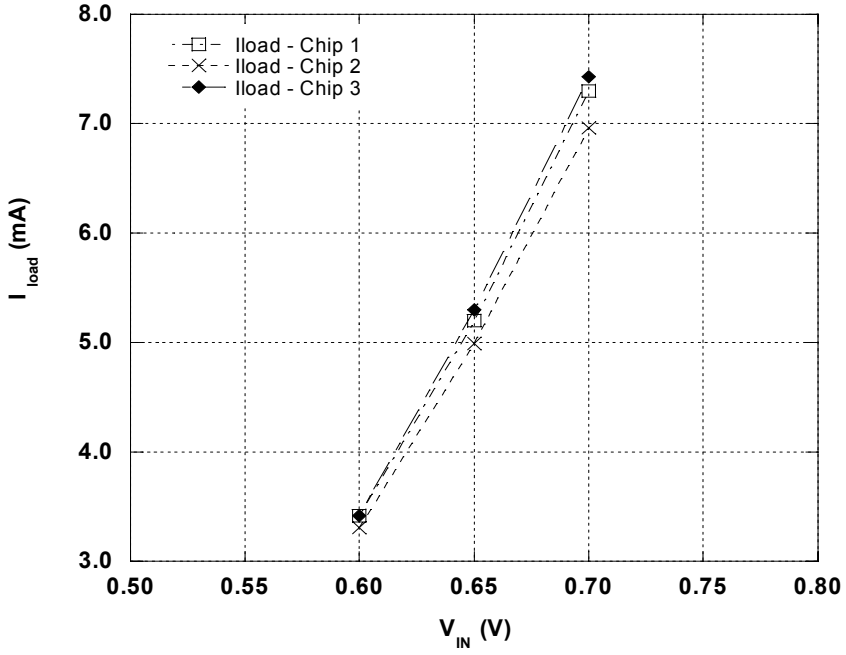

Figure 5.20: Measured I_{load} versus V_{IN} (bias) for LNA5.

In this testing, three different biasing voltages were used for LNA5. For the DC measurement, the results are shown in Figure 5.20. In this measurement, three different voltages of the bias-tee were used. The result shows the linear characteristic of the I_{load} versus V_{IN}.

The optimum results of power gain (S_{21}), is shown in Figure 5.21. The achieved value of S_{21} is about 8.63 dB at the center frequency. Notice that the center frequency is slightly shifted to the right from the targeted frequency (2 GHz) to about 2.02 GHz. For other S_{21} results based on different biasing voltages, Figures 5.22 and 5.23 show the corresponding values; 7.7 dB for 0.65V (shifted to 2.02 GHz), and 6.4 dB for 0.6V

(centered at 2.0 GHz) respectively. Meanwhile, the other S_{21} results of other measured chips are shown in Tables 5.7 and 5.8 for comparison.

The reverse isolation (S_{12}) values obtained (below -20 dB) as shown in Figures 5.21 to 5.23 as well as in Tables 5.7 and 5.8 are typical. As shown, S_{12} of the circuit gives values ranging from about -23 to -21 dB along the interested bandwidth of 400 MHz.

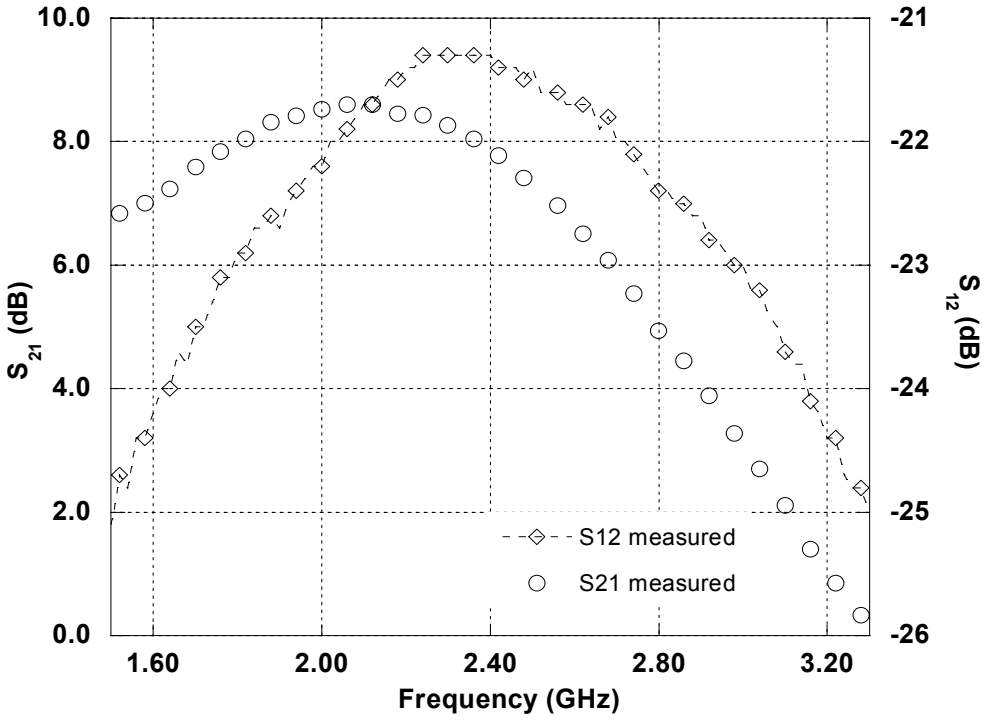

Figure 5.21: Forward gain and reverse isolation of LNA5 with 0.7V bias.

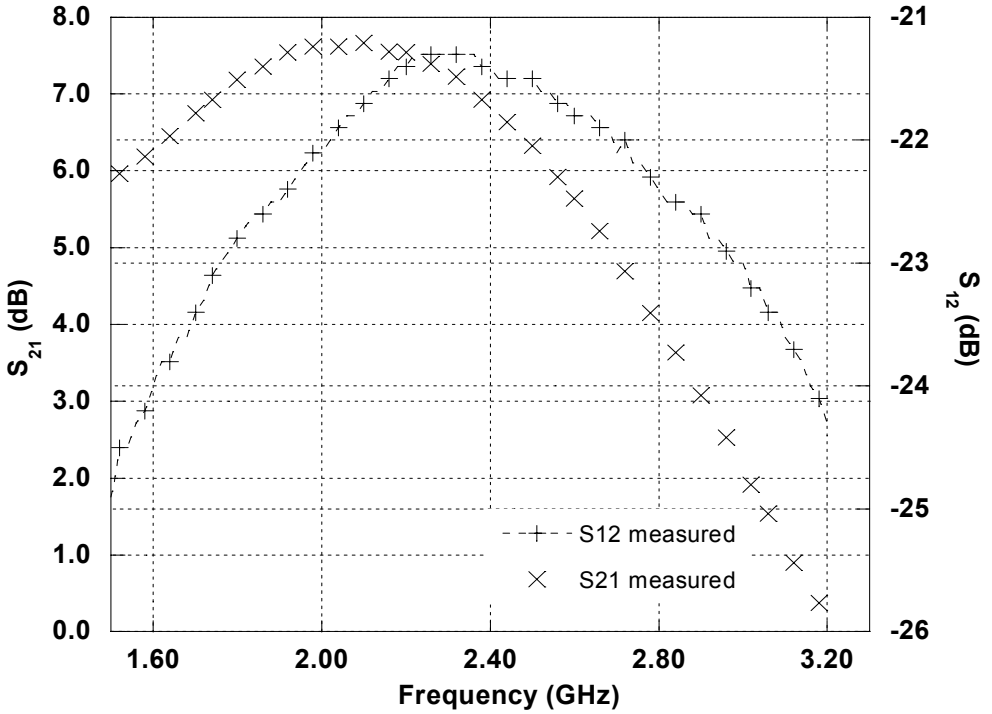

Figure 5.22: Forward gain and reverse isolation of LNA5 with 0.65V bias.

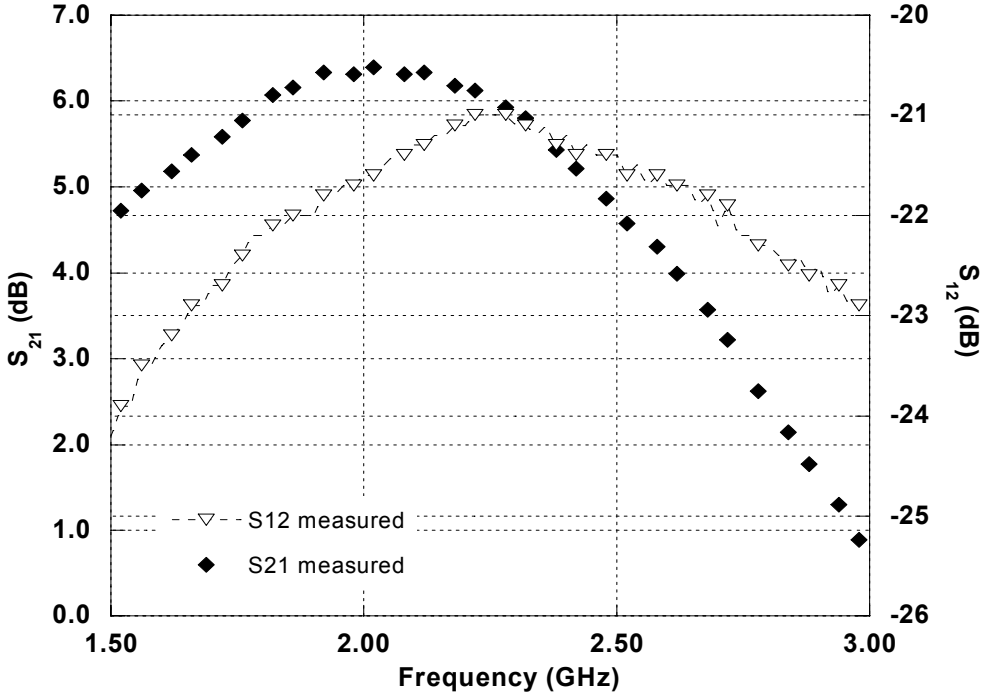

Figure 5.23: Forward gain and reverse isolation of LNA5 with 0.6V bias.

The optimum value of the input return loss, S_{11} of the LNA5 is shown in Figure 5.24. For S_{11}, at 0.7V, center frequency is shifted to about 2.18 GHz. The obtained value is -14.2 dB. Then, the other results of S_{11} can be seen in Figures 5.25 and 5.26. At 0.65V, the value obtained is -14.6 dB (center frequency shifted to 2.24 GHz). Then, for 0.6V, -14.6 dB is obtained at center frequency shifted to 2.24 GHz. Comparing the three biasing voltages, S_{11} achieved are not much different in terms of bandwidth and peak values at the center frequency except that the shifts of the center frequency are different with different biasing voltages.

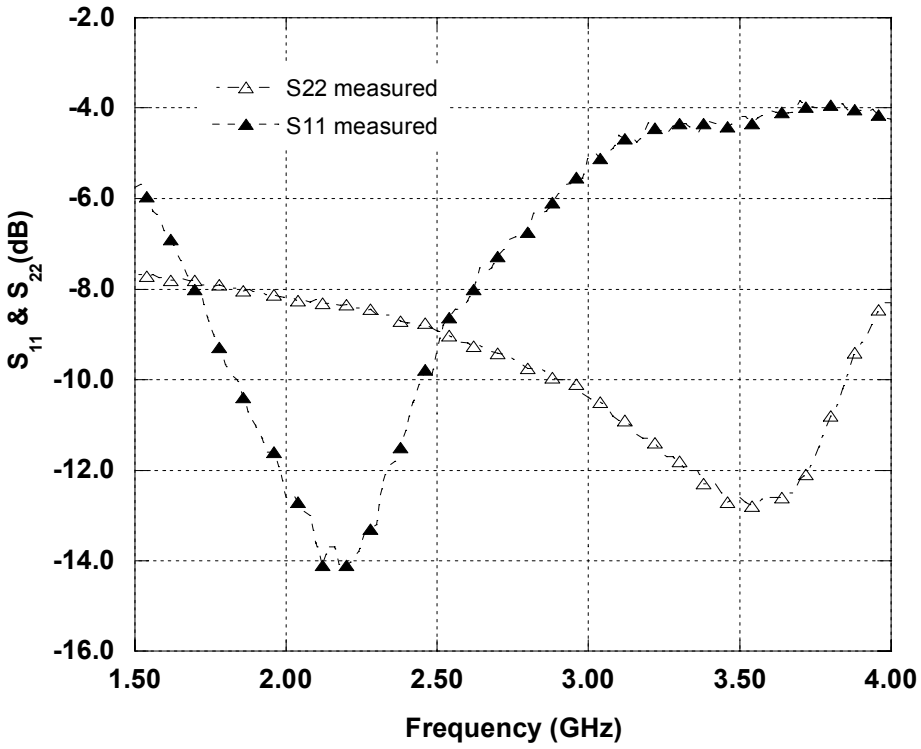

Figure 5.24: Input and output return losses of the LNA5 with 0.7V bias.

For optimum output return loss, with 0.7V bias, the obtained S_{22} is -12.8 dB at the center frequency (shifted to 3.54 GHz). For other S_{22} results, Figures 5.25 and 5.26 show the corresponding values. At 0.65V bias, the obtained S_{22} is -13.3 dB at the center frequency (shifted to 3.54 GHz) while for 0.6V bias, the obtained S_{22} is -13.7 dB at the center frequency (shifted to 3.54 GHz). In addition, the measurement results of the other chips are shown in Tables 5.7 and 5.8 for comparison.

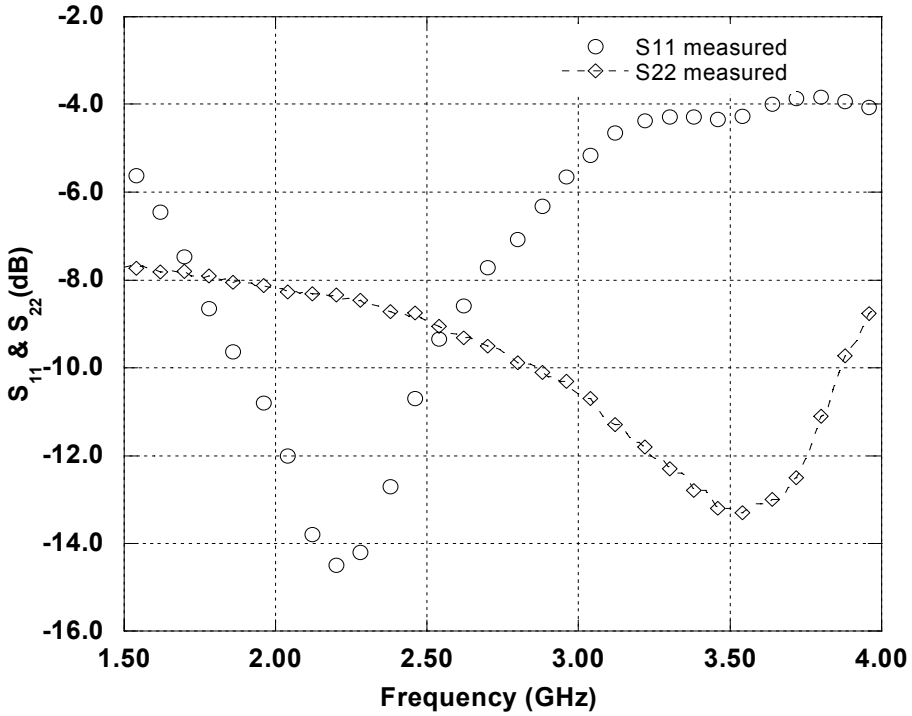

Figure 5.25: Input and output return losses of the LNA5 with 0.65V bias.

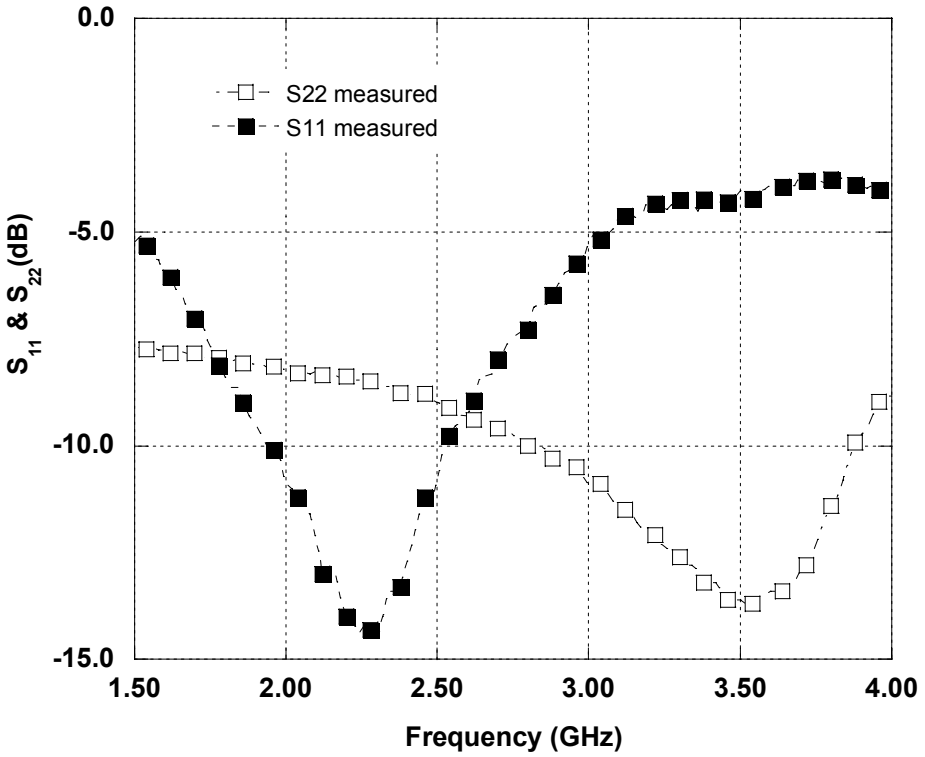

Figure 5.26: Input and output return losses of the LNA5 with 0.6V bias.

Table 5.7: Performance summary of the measurement results for chip 2 of the LNA5.

	Chip 2		
	0.6V	**0.65V**	**0.7V**
$S_{21}\ (dB)$	5.3@2.0 GHz	6.5@2.0 GHz	7.1@2.1 GHz
$S_{12}\ (dB)$	- 24.0@2.76 GHz	- 24.1@2.72 GHz	- 24.1@2.72 GHz
$S_{11}\ (dB)$	- 14.6@2.08 GHz	- 14.6@2.18 GHz	- 14.7@2.2 GHz
$S_{22}\ (dB)$	- 12.0@3.44 GHz	- 12.4@3.44 GHz	- 12.7@3.44 GHz

Table 5.8: Performance summary of the measurement results for chip 3 of the LNA5.

	Chip 3		
	0.6V	**0.65V**	**0.7V**
$S_{21}\ (dB)$	6.6@2.02 GHz	7.7@2.02 GHz	8.3@2.02 GHz
$S_{12}\ (dB)$	- 23.7@2.9 GHz	- 23.7@2.9 GHz	- 23.8@2.9 GHz
$S_{11}\ (dB)$	- 14.2@2.18 GHz	- 14.6@2.24 GHz	- 14.6@2.3 GHz
$S_{22}\ (dB)$	- 12.8@3.54 GHz	- 13.3@3.54 GHz	- 13.7@3.54 GHz

For the linearity requirement, the measured $IIP3$ is +5.7 dBm for the 0.7V bias as shown in Figure 5.27. At 0.65V, the achieved value is +4.3 dBm and -0.5 dBm is obtained for 0.6V bias as shown in Figures 5.28 and 5.29 respectively. For $P1dB$, as shown in Figures 5.30 to 5.32, the measured values are: at 0.7V is -3.9 dBm; for 0.65V is -6.0 dBm; and for 0.6V is -9.9 dBm respectively. In addition, Table 5.9 shows the comparable results for linearity of other measured chips. These achieved values for the linearity are better than LNA2 (for similar technology and optimum bias of 0.7V) and exceeds the specification. In other words, the design has been optimised to obtain $IIP3$ and $P1dB$ as best as possible for the circuit.

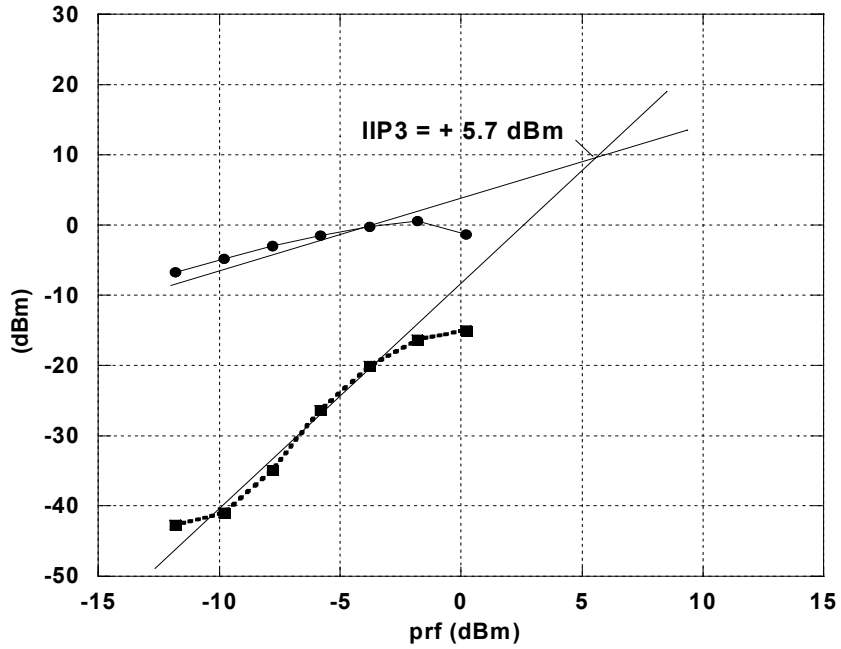

Figure 5.27: *IIP3* of LNA5 with 0.7V bias.

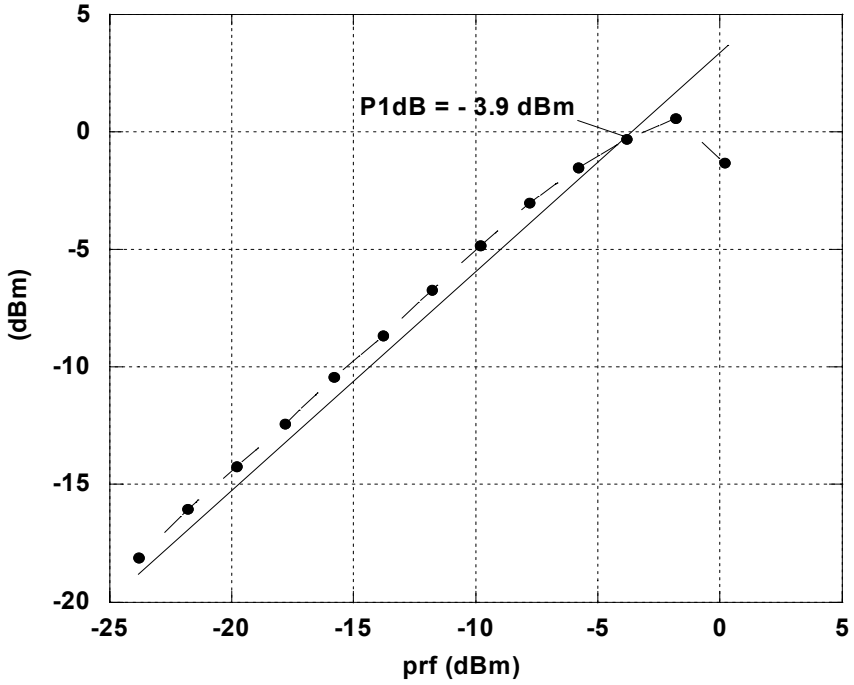

Figure 5.28: *P1dB* of LNA5 with 0.7V bias.

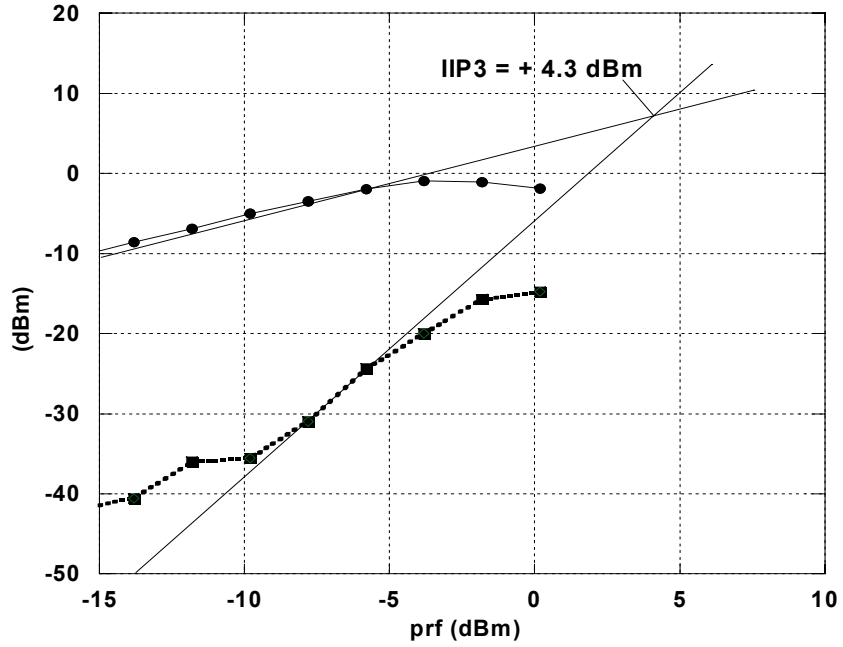

Figure 5.29: *IIP3* of LNA5 with 0.65V bias.

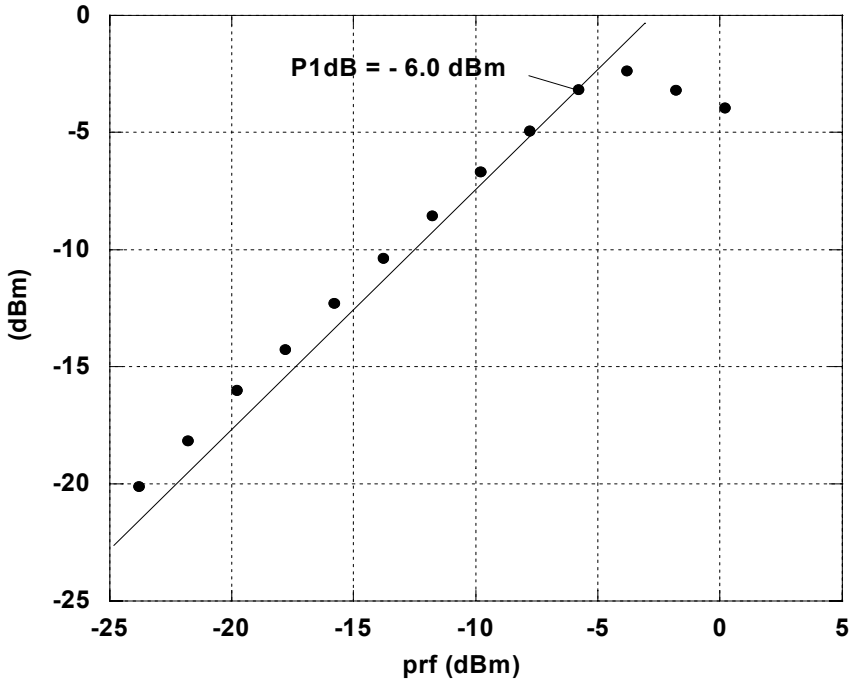

Figure 5.30: *P1dB* of LNA5 with 0.65V bias.

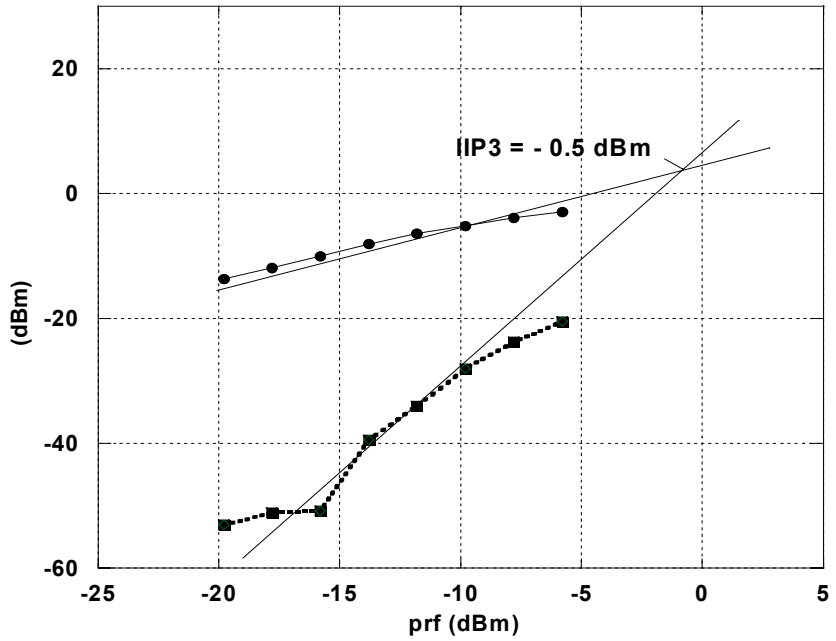

Figure 5.31: *IIP3* of LNA5 with 0.6V bias.

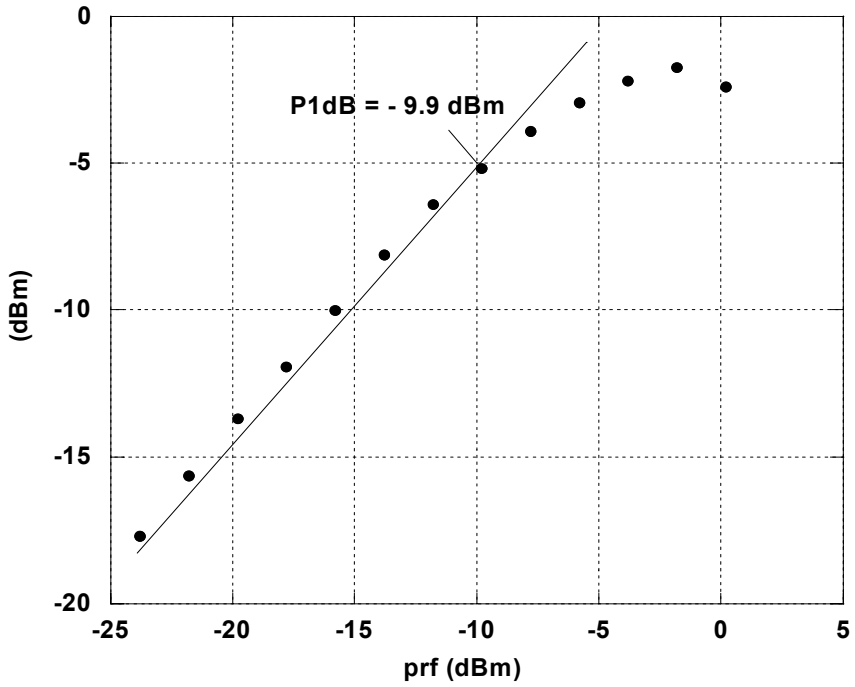

Figure 5.32: *P1dB* of LNA5 with 0.6V bias.

Table 5.9: Linearity performance summary of the other chips for LNA5

	0.6V		0.65V		0.7V	
	$IIP3$ (dBm)	$P1dB$ (dBm)	$IIP3$ (dBm)	$P1dB$ (dBm)	$IIP3$ (dBm)	$P1dB$ (dBm)
Chip 2	+ 2.5	- 7.8	+ 4.5	- 5.9	+ 6.2	- 4.0
Chip 3	+ 2.8	- 7.7	+ 4.8	- 5.9	+ 6.5	- 4.1

Figures 5.33 to 5.35 show the die photograph of the measured LNA2, LNA4 and LNA5.

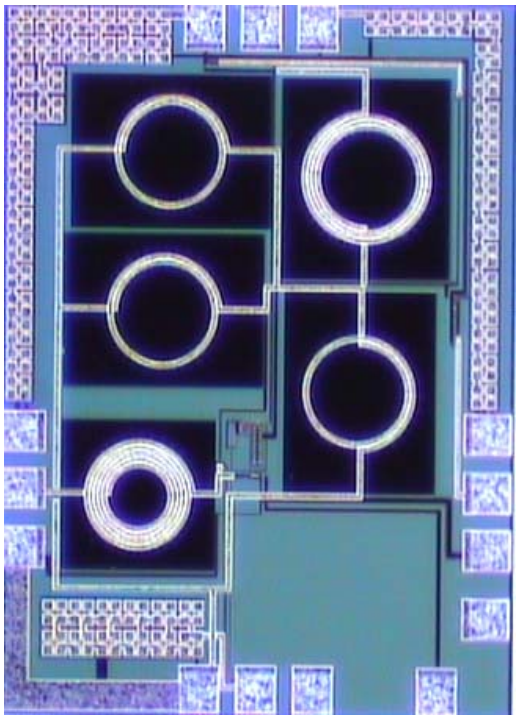

Figure 5.33: Die photograph of LNA2.

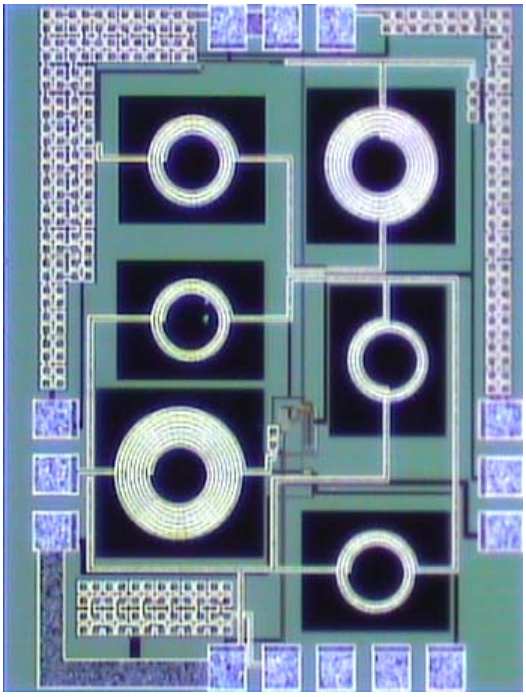

Figure 5.34: Die photograph of LNA4.

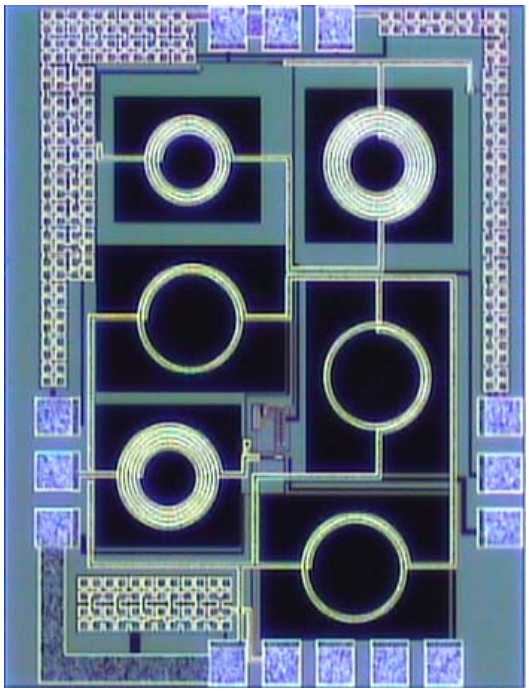

Figure 5.35: Die photograph of LNA5.

5.3 Discussion of the results

Table 5.10 shows the performance summary of the wideband LNA2 to LNA5. The measurement results of power gain (S_{21}) show that LNA2 achieved the best gain in comparison with LNA4 and LNA5. However, for LNA2, the gain achieved is less than that achieved in the pre-layout simulation. The gain loss is maybe attributed by the losses from the 2 probe cables (2 dB loss) and from the parasitic capacitance of the load inductor and the buffer circuit. If we look back at the equation 3.40, the gain loss could be explained by the changes in the current of M_3 which then alters the C_{gs3}, in which modifies the $Z_L(s)$. This means that there has to be an off-chip impedance matching if the circuit is to be used. Furthermore, the losses of the gain also contributed by the parasitic in which could also be linked to equation 3.40. On the other hand, the measured gain of LNA4 and LNA5 just have loss of about 4-5 dB compared to the simulated gain. Therefore, the technique used to develop LNA4 and LNA5 is more efficient in term of achievable gain. However, the gain comparison of LNA4 and LNA5 shows that, the achieved gain of LNA5 is better than LNA4 as the result shows a difference (simulated to measured result) of 4 dB compared to 5 dB for LNA4. This suggests that LNA4 needed more power to achieve the same gain as LNA5.

In term of input and output return losses, S_{11} and S_{22}, Table 5.10 shows that, for LNA2, the measured result of S_{11} is very close to simulated result (the difference of 11.7 % between simulated and measured results). On the other hand, for LNA4 and LNA5, the differences (simulated to measured result) are quite significant. This could be explained

by the performance of the inductors (different values with different Q) used for the input matching in LNA4 and LNA5. In addition, the technique used for the design of these LNAs also play an important role in term of performance of S_{11}. Meanwhile, for S_{22}, Table 5.10 shows that, for LNA2, the difference between measured result and simulated result are quite significant. This also could be explained again with using equation 3.40 whereby C_{gs3} play an important role as the changing in the current of the buffer circuit could alters the output impedance of LNA2. But for LNA4 and LNA5, the differences (3.34 % and 22.3 % respectively between simulated and measured result) are small and are close to each other. Again, it proves that the technique used for LNA4 and LNA5 designs is better regarding S_{22} (in term of simulated to the measured result) compared to technique used for LNA2 where S_{22} is controlled by the buffer circuit. In other words, small variation in the buffer current could easily change the S_{22} of LNA2.

Regarding S_{12}, Table 5.10 shows a significant differences between the measured results and simulated results. However, this is not critical as the achieved measured results are either typical or better than typical value, which is around -20 to -30 dB. It can be seen from Table 5.10, the LNA4 achieved good S_{12} and is better than typical value compared to other LNAs.

In term of linearity ($IIP3$ and $P1dB$), Table 5.10 shows a quite interesting result for LNA2 whereby the measured result is better than the simulated result. But for LNA4, the measured result is quite far from the simulated. This suggests that LNA4 need more power to achieve a better linearity. However, the achieved result for LNA4 is still good.

Meanwhile LNA5 is also showing a quite significant difference between the measured result and simulated result. Nonetheless, the achieved measured result for LNA5 is still good and within specification targeted (See Table 2.5 in Chapter 2).

Table 5.10: Performance summary of the wide band LNAs

	LNA2		LNA4		LNA5	
	Sim.	**Mea.**	**Sim.**	**Mea.**	**Sim.**	**Mea.**
$S_{21}\,(dB)$	23.2	9.16	11.3	7.4	12.6	8.63
$S_{12}\,(dB)$	- 63	- 31.7	- 62	- 41.7	- 53	- 23
$S_{11}\,(dB)$	- 22.3	- 24.9	- 47.7	-19.4	- 24.4	- 14.6
$S_{22}\,(dB)$	-23.6	- 32.8	- 23.9	-24.7	- 11.21	- 13.7
$IIP3\,(dBm)$	- 7.08	- 1.2	+ 8.28	+ 1.4	+ 8.4	+ 5.7
$P1dB\,(dBm)$	- 18.02	- 11.8	- 2.06	- 9.5	- 2.02	- 3.9

Table 5.11 shows the performance summary of the achieved measured bandwidth of the wide band LNA2 to LNA5. Overall, the targeted bandwidths were achieved as planned and for some parameters are better than expected. However, the exception is applicable for S_{21} as the targeted gain along the bandwidth (400 MHz for LNA2 and

LNA5 and 200 MHz for LNA4) is not achieved as expected. With the improved gain of the LNA circuits in this work, the bandwidth targeted will be achieved.

Table 5.11: Achieved bandwidths of the wide band LNAs

Bandwidth	LNA2		LNA4		LNA5	
	Sim.	Meas.	Sim.	Meas.	Sim.	Meas.
S_{21} - (GHz)	2	> 0.4@8 dB	0.29	> 0.2@7 dB	1.44	> 0.4@8 dB
S_{12} - (GHz)	2	2	0.5	0.8	2	2
S_{11} - (GHz)	0.5	1.18	0.28	0.35	0.64	0.6
S_{22} - (GHz)	2	2	0.5	0.97	1.18	0.94

Table 5.12 shows the performance summary of the measurement results of other narrowband LNAs in CMOS and BiCMOS technologies in comparison with results obtained in this project. This information is from the latest publications in recent years and targeted for GSM and 3G systems. From this Table 5.12, the wide band LNAs (LNA2 to LNA5) show a good performance in comparison with other designs in terms of input and output return losses and linearity ($IIP3$) respectively. For gain, the achieved values in this project are bit lower compared to those in other publications. However, the gains achieved here are very close to the targets which at least 10 dB. If the cable loss (2 dB, due to the measurement) is taken into account, then the achieved values could easily reach 10 dB.

Table 5.12: Comparison with other publications

	This work			References				
	LNA2	**LNA4**	**LNA5**	[34]		[65]	[69]	
Technology	**0.18 µm CMOS**			0.18 µm CMOS		0.18 µm CMOS	0.25 µm BiCMOS	
Freq. (GHz)	**2**	**0.9**	**2**	0.9	1.8	2.1	1.8	2.1
$S_{21}\,(dB)$	**9.16**	**7.4**	**8.63**	14	13	12	12.6	14.2
$S_{11}\,(dB)$	**- 24.9**	**-19.4**	**- 14.6**	-12	-14	-6.5	-18.9	-14
$S_{22}\,(dB)$	**- 32.8**	**-24.7**	**- 13.7**	-15	-14	-24	n/a	n/a
$IIP3\,(dBm)$	**- 1.2**	**+ 1.4**	**+ 5.7**	-14	-14	-2.5	-4	-6.5

5.4 Conclusion

This chapter presents the measurement results of the three fabricated wide band LNAs. Overall, the measurement results show a good agreement with the simulated results as presented in Section 5.3. However, some of the parameters still need an improvement i.e. gain. This could be done by improving the circuit power by increasing the current of the circuit. But this action should be taken carefully as not to contradict with the low power design. Another approach is to carefully design the layout to reduce the circuit parasitic. In addition, as the design of the circuit were using ready made passive components from the design kit provided by the foundry, there are limitations in the

optimisation process of the circuits. Therefore, the problem could be solved by designing custom made passive components for particular LNA at particular frequency especially the inductor as it is the challenging component due to the problem with low quality factor.

In conclusion, despite of some limitations (i.e. fixed inductors values used) in designing the LNA2, LNA4 and LNA5 using the 0.18 μm technology, it shows that the achieved measurement results are promising.

Also, this chapter presents only the wide band LNAs to cater for the lower band and upper band designs of multi-standard multi-band LNAs which are from 800 to 1000 MHz and 1800 to 2200 MHz respectively. These bands should cover the most standards currently in use for mobile communications world wide (see Table 2.1 and 2.2 in Chapter 2). In relation to that, the next chapter will cover the design and implementation of a reconfigurable LNA that has the capability to support those entire standards in just one single system.

CHAPTER 6:

RECONFIGURABLE MULTI-STANDARD MULTI-BAND LNA

6.0 Introduction

In Chapters 3 to 5, the theories, designs and implementations of the multi-standard multi band LNAs have been presented. The designs of these wide band LNAs implemented for two bands of interest which are lower frequency band from 800 to 1000 MHz and upper frequency band from 1800 to 2200 MHz respectively. The ultimate objective of this research is to design and implement a single reconfigurable multi-standard multi-band LNA. This LNA will be designed in such a way that it has the capability to support the two bands of interest as mentioned before. In other words, reconfigurability is achieved by changing of hardware configuration to support these frequency bands.

This chapter presents the design and implementation of a reconfigurable LNA for mobile receiver. Section 6.1 elaborates on the design and implementation of such device.

Section 6.2 presents the simulation results. Section 6.3 provides discussion of the results. Conclusion is provided in Section 6.4.

6.1 Design and implementation of reconfigurable multi-standard multi-band LNA

6.1.1 Design consideration

In order to design multi-standard multi-band LNA with a good performance, a good topology for such device is needed to support the required specifications. As discussed earlier in Chapter 3, IDCS topology has been proven to be a good choice in designing multi-standard multi-band LNA. However, these wide band LNAs were not designed as a single LNA but two LNAs instead (900 MHz for lower band and 2 GHz for upper band) to cover most of the standards currently in use world wide for mobile communications. Also, they were designed in such a way to ensure the feasibility of IDCS topology (which was typically used for designing a narrowband LNA) as wide band LNA. Based on the wide band LNA designs principle, implementations, results and discussions were presented in Chapters 3 to 5. Here a single reconfigurable multi-standard multi-band LNA for wireless mobile communications is proposed, based on the two LNAs presented in Chapters 3 to 5. To design such LNA, design considerations should be taken as follow:

- Which IDCS technique is to be used? In this case, IDCS technique introduced in Chapter 3, in particular the technique used i.e. for LNA4 (900 MHz) and LNA5 (2

GHz) is chosen as it has been proven to provide a good performance collectively in terms of NF, linearity and s-parameters.

- Reconfigurability: The concept of reconfiguration here means, finding a way to realise the multi-standard multi-band in two modes of operation without degrading the LNA performance with respect to a single multi-standard wide band LNA. Those two modes of operation are: Mode 1 which is operating in lower band (800 to 1000 MHz) and Mode 2 which is operating in upper band (1800 to 2200 MHz).
- LNA parameters: In this matter, as only one active circuit (i.e. one cascode LNA) will be used at a time, hence there will be a trade-off between power consumption and design parameters (refers to Figure 6.1), such as W / L of the transistor M_1, L_G, L_S, L_D, L_1, R_1, C_{ex1}, C_{ex2}, C_{D1}, and C_{D2}. This means that, it will be even harder to find the best values of passive components especially inductors which should compromise between two bands of standards (lower and upper frequency bands) as the design will use the same fixed inductors (refer to Appendix–C) provided by the foundry.
- Full integration: As the LNA is targeted to be fully integrated; the trade-off between minimum NF and full integration is to be considered. To achieve full integration of the LNA, component sharing is implemented by introducing active switches in the circuit. The introduction of these active components will theoretically introduce an extra noise to the circuit. Therefore, the design of those switches also need to be carefully done to reduce the noise as much as possible.

6.1.2 A reconfigurable multi-standard multi-band LNA

One of the important properties of the wide band LNA (i.e. LNA4 and LNA5) which have been designed in Chapter 3 is the use of the external gate-source capacitance (C_{ex}). This property is used to obtain the input matching by providing the extra degree of freedom at the input circuit. The fact that this C_{ex} can be exploited to design a reconfigurable LNA for two bands of interest will therefore be discussed here. The LNA is designed to operate in upper band as a default mode because in this mode, it uses lower inductance (theoretically will give lower series resistance) at the input. The idea is to use the same coils (L_G and L_S), the same transistors M_1 and M_2 and by altering the value of the external gate-source capacitance allows the LNA to operate in lower band mode. In this way, a simple reconfigurable LNA is obtained. The coils' sharing has an advantage because chip area is reduced and the need for another coil is avoided.

Figure 6.1 shows the circuit considered as a single mode LNA, where C_{ex1} and C_{ex2} are the external gate-source capacitances at the input which represents the capacitances required for the upper band and lower band modes respectively. C_{D1} and C_{D2} are the load capacitances at the output which represent capacitances for upper band and lower band modes respectively. L_G, L_S, L_D, L_1 and R_1 are the input and load inductors and load resistor which represents the shared components for upper and lower band modes. Transistors $SW0$, $SW1$, and $SW2$ are the switches which will be used to switch on and off to change the external gate-source capacitance at the input of

the LNA as well as the load at the output of the LNA respectively. These switches determine the mode of the LNA function, either in upper band or lower band mode.

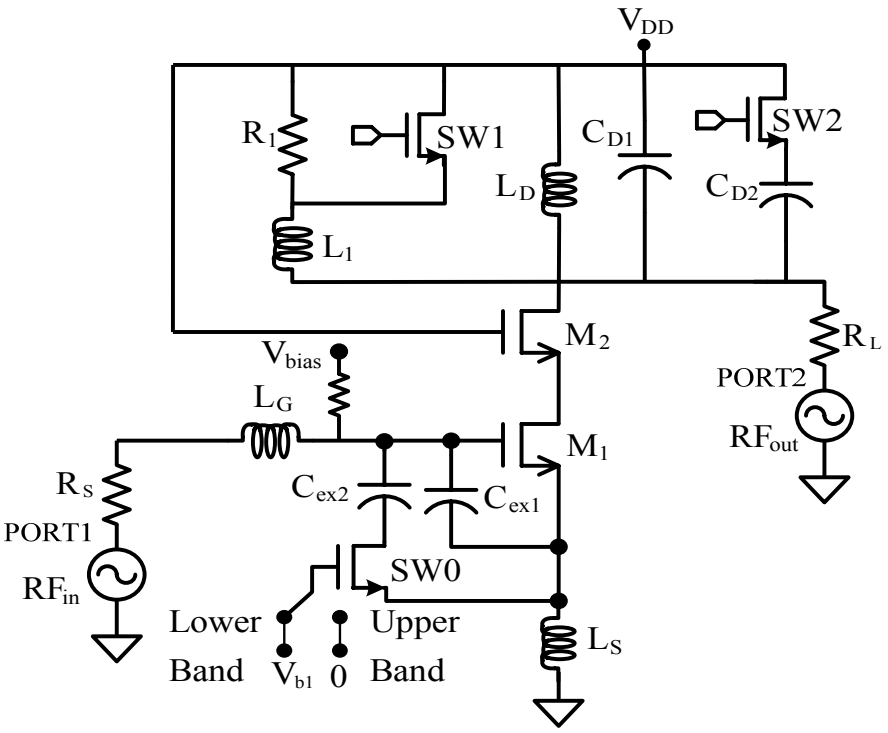

Figure 6.1: Circuit diagram of a reconfigurable multi-standard multi-band LNA

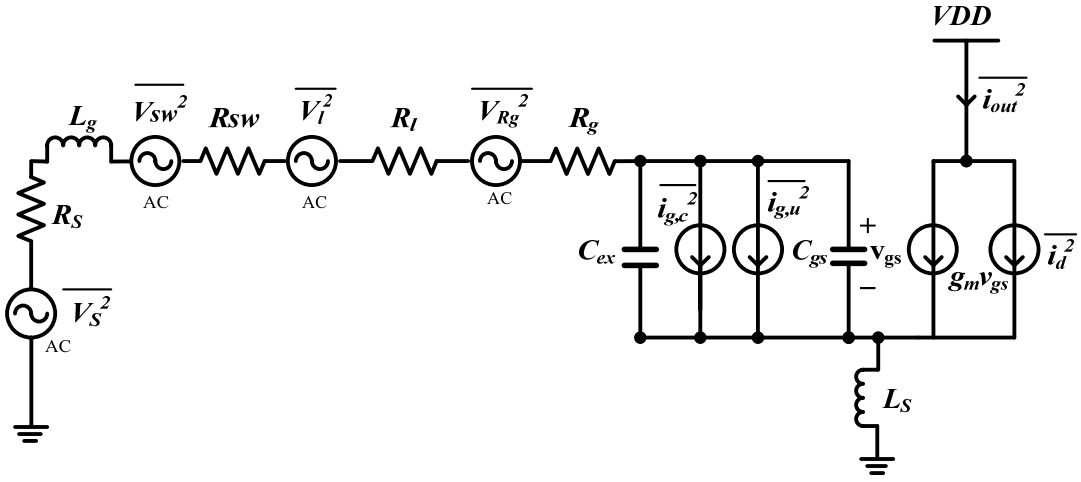

Figure 6.2: Revised IDCS small-signal model for reconfigurable LNA

Figure 6.2 shows the corresponding small-signal model for the reconfigurable LNA. In this model, new parameter is introduced for the calculation of NF. This parameter is R_{SW}, which represents the resistance of the transistor $SW0$. This condition applies when the LNA is operating at lower band mode only. Therefore equations (6.1) and (6.2) are extracted based on (3.25) and (3.42) to define the noise factor (*F*) and NF respectively. For upper band mode, the same expressions of (3.25) and (3.42) are used for the calculation of NF [25] [72].

$$F = 1 + \frac{R_{sw}}{R_S} + \frac{R_l}{R_S} + \frac{R_g}{R_S} + \frac{\gamma}{\alpha}\frac{\chi}{Q_L}\left(\frac{\omega_o}{\omega_T}\right) \tag{6.1}$$

$$NF = 10\ log[F] = 10\ log\left[1 + \frac{R_{sw}}{R_S} + \frac{R_l}{R_S} + \frac{R_g}{R_S} + \frac{\gamma}{\alpha}\frac{\chi}{Q_L}\left(\frac{\omega_o}{\omega_T}\right)\right] \tag{6.2}$$

In term of input impedance matching, Figure 6.2 shows the introduction of C_{ex}. This parameter represents the total external gate-source capacitance which sets the input impedance matching of the LNA. The values of capacitors C_{ex1} and C_{ex2} have to be determined in such away that the matching conditions for upper band and lower band are satisfied. Depending of the condition of $SW0$ whether in ON of OFF mode, the LNA will operate either at upper band frequency or lower band frequency.

Therefore, the following expressions are revised for the impedance matching at the input of the LNA based on (3.44) and (3.45).

At upper band mode ($SW0$ =OFF),

Then
$$C_{ex} = C_{ex1} = C_{gs_{ex,upper}} \tag{6.3}$$

and
$$Z_{in,upper} \approx s\left(L_G + L_S\right) + \frac{g_{m1}L_S}{C_{gg1} + C_{gs_{ex,upper}}} + \frac{1}{s\left(C_{gg1} + C_{gs_{ex,upper}}\right)} \tag{6.4}$$

$$R_S = \frac{g_{m1}L_S}{C_{gg1} + C_{gs_{ex,upper}}} = 50\ \Omega \tag{6.5}$$

At lower band mode ($SW0$ =ON),

Then
$$C_{ex} = C_{ex1} + C_{ex2} = C_{gs_{ex,lower}} \tag{6.6}$$

and
$$Z_{in,lower} \approx s\left(L_G + L_S\right) + \frac{g_{m1}L_S}{C_{gg1} + C_{gs_{ex,lower}}} + \frac{1}{s\left(C_{gg1} + C_{gs_{ex,lower}}\right)} \tag{6.7}$$

$$R_S = \frac{g_{m1}L_S}{C_{gg1} + C_{gs_{ex,lower}}} = 50\ \Omega \tag{6.8}$$

where $C_{gs_{ex,upper}}$ is the external gate-source capacitance when the LNA operate in upper band mode and $C_{gs_{ex,lower}}$ is the external gate-source capacitance when the LNA operate in lower band mode. Here, g_{m1}, $C_{gg1} = C_{gs1} + C_{gd1} + C_{gb1}$, L_G and L_S are the transconductance, total gate capacitance, and gate and source-degenerative inductors, respectively. The total gate capacitance is the summation of gate-source, gate-drain and gate-bulk capacitances, respectively.

In term of output impedance matching, $SW1$ and $SW2$ play an important roles in determining the load at the output. The on and off of these switches will set the output

impedance matching of the LNA either to operate at upper band or lower band mode. The LNA is operating as follows:

- To set the output impedance of the LNA at upper band mode, $SW1$ has to be in ON mode and $SW2$ in OFF mode. In this condition, the total resistance (resistor between the drain and source of $SW1$ and R_1) is representing the resistor which is in series with L_1. Together with C_{D1}, and L_D, it will set the output impedance matching for upper band mode. This technique is actually a new approach which has been introduced in Chapter 3 to avoid the use of buffer circuit for the output matching. Thus, the total resistance of $SW1$ and R_1 is actually representing the R_1 which is in series with L_1 as depicted in Figure 3.10 (Chapter 3).

- On the other hand, the output impedance of LNA operating at lower band mode is obtained when $SW2$ in ON mode and $SW1$ in OFF mode. In this condition, only R_1 is representing the resistance which is in series with L_1. Together with total load capacitance ($C_{D1} + C_{D2}$), and L_D, it will set the output impedance matching for lower band mode.

Therefore, to determine the impedance matching at the output of the LNA, expression (3.45) is revised to obtain the following new expressions for upper band and lower band modes.

For upper band,

Then
$$Y_{L,upper} = sC_{D1} + \frac{1}{r + sL_D} + \frac{1}{R_{sw1} \square R_1 + sL_1} \tag{6.9}$$

$$\begin{aligned} \therefore Z_{L,upper} &= \frac{1}{Y_{L,upper}} = \left(\frac{1}{sC_{D1}} \right) \square \left(r + sL_D \right) \square \left(R_{upper} + sL_1 \right) \\ &= \frac{R_{upper} r + s\left(R_{upper} L_D + L_1 r \right) + s^2 L_1 L_D}{1 + sC_{D1}\left(r + R_{upper} \right) + s^2 C_{D1}\left(L_1 + L_D \right)} \end{aligned} \tag{6.10}$$

For lower band,

Then
$$Y_{L,lower} = s\left(C_{D1} + C_{D2} \right) + \frac{1}{r + sL_D} + \frac{1}{\left(R_1 \right) + sL_1} \tag{6.11}$$

$$\begin{aligned} \therefore Z_{L,lower} &= \frac{1}{Y_{L,lower}} = \left(\frac{1}{sC_{D,lower}} \right) \square \left(r + sL_D \right) \square \left(R_{lower} + sL_1 \right) \\ &= \frac{R_{lower} r + s\left(R_{lower} L_D + L_1 r \right) + s^2 L_1 L_D}{1 + sC_{D,lower}\left(r + R_{lower} \right) + s^2 C_{D,lower}\left(L_1 + L_D \right)} \end{aligned} \tag{6.12}$$

where $R_{upper} = R_{sw1} \square R_1$, $R_{lower} = R_1$ and $C_{D,lower} = C_{D1} + C_{D2}$.

Thus to determine the gain of the LNA at upper and lower band, (3.47) is revised and the following expressions are obtained:

Gain of the upper band,

$$S_{21} = 2\frac{v_{out}}{v_{in}} \equiv G_{m21}(s).Z_{L,upper}(s) \tag{6.13}$$

Gain of the lower band,

$$S_{21}=2\frac{v_{out}}{v_{in}} \equiv G_{m21}(s).Z_{L,lower}(s) \tag{6.14}$$

6.1.3 Circuit implementation of reconfigurable multi-standard multi-band LNA

The reconfigurable multi-standard multi-band LNA which will be operating in two modes of operation: lower band at 900 MHz and upper band at 2 GHz, has been designed and implemented using 0.18 μm CMOS technology and simulated in Spectre RF. The components values are obtained based on the following design steps, design equations as in (6.15) to (6.19), design flow and expressions from Chapter 3 (some rewritten here).

The design steps are as follows:

- Choose a correct starting value of overdrive voltages ($V_{gs}-V_t$) to satisfy the requirement for good linearity [96] [97].
- Find the aspect ratio W/L, and the transconductance (g_m) of transistor M_1 based on a given power budget that should satisfy the operation of two bands of interest (upper band and lower band) [25].
- Find the best value of L_S that could satisfy the simultaneous noise and input matching. Together with this, the additional capacitance C_{ex} that gives extra degree of freedom for noise and input matching for both bands should be chosen correctly. This value should compromise between the available power gain and

the size of L_S. One more consideration is the fact that large value of C_{ex} leads to gain reduction [27].

- Find the best value of L_G that could satisfy the simultaneous noise and input matching for both bands of interest. This step is very hard as the inductors provided by the foundry are fixed to specific values (refer to Appendix–C).

Then together with the design steps, the following equations are used to determine the components values for the reconfigurable LNA [25] [27] [96] [97].

$$IIV3=\sqrt{\frac{8}{3}}\frac{1}{\alpha}V_{od}\left(1+\frac{1}{2}\alpha V_{od}\right)\left(1+\alpha V_{od}\right)^2$$
$$\therefore IIP3 \approx V_{od} \tag{6.15}$$

$$W_{opt}=1.5(\omega_o L C_{ox} R_s Q_{in,opt,P_D})^{-1} \approx \frac{1}{3\omega L C_{ox} R_S} \tag{6.16}$$

$$\omega_o^2=\frac{1}{C_{gs}(L_G+L_S)} \tag{6.17}$$

$$\omega_T \approx \frac{g_m}{C_{gs}}=\frac{g_m}{\frac{2}{3}WLC_{ox}} \tag{6.18}$$

$$C_{gs,t}=C_{gs,int}+C_{ex} \tag{6.19}$$

where $C_{gs,t}$ and $C_{gs,int}$ are the total gate-source capacitance of the LNA and intrinsic gate-source capacitance of M_1.

First, (6.15) to (6.19) are used to determine the LNA's components values for the upper band which operates at 2 GHz. For example, the width of the transistor and the C_{ex} of the LNA to operate at 2 GHz were obtained to be 350 μm and 60 fF. Accordingly, the components values for lower band which operates at 900 MHz were obtained as shown in Table 6.1.

From (6.17) and (6.18) the transconductance (g_m) of lower band and upper band have been calculated and the calculations show that $g_{m,lower} > g_{m,upper}$. Also, total gate-source capacitance ($C_{gs,t}$) of lower band is higher than $C_{gs,t}$ of upper band. This applies on C_{ex} where $C_{ex,lower} > C_{ex,upper}$. Therefore, the tail current of the LNA operating at lower band frequency has to be higher than the tail current of the LNA operating at upper band frequency.

For that reason, in each mode of operation, two values of tail current have been used. Those values are: 8.75 mA and 10.45 mA for upper band, and 12.43 mA and 14.7 mA for lower band respectively. The higher value used for lower band is to compensate for the gain reduction due to higher value of C_{ex} used at the input. In relation to this matter, as shown in [27], for C_{ex}=1.5C_{gs}, the maximum available gain of the LNA is degraded by 1 dB.

Table 6.1: Component values for reconfigurable multi-standard multi-band LNA

Case	Condition	
Frequency	Upper band (2 GHz)	Lower band (0.9 GHz)
M_1 (W/L)	(350/0.18) μm	
M_2 (W/L)	(350/0.18) μm	
SW0 = SW2 (W/L)	(60/0.18) μm	
SW1 (W/L)	(25/0.36) μm	
L_1	4.21 nH	
L_D	15.8 nH	
L_G	12.9 nH	
L_S	0.55 nH	
$C_{D,upper}$ / ($C_{D,lower} = C_{D1}+C_{D2}$)	100 fF	(100 + 915) fF
$C_{ex,upper}$ / ($C_{ex,lower} = C_{ex1}+C_{ex2}$)	60 fF	(0.06 + 2.63) pF
$R_T = (R_{sw1}* \| R_1) / R_1$	62 || 79 Ω	79 Ω

$R_{sw1}*$ is obtained from simulation.

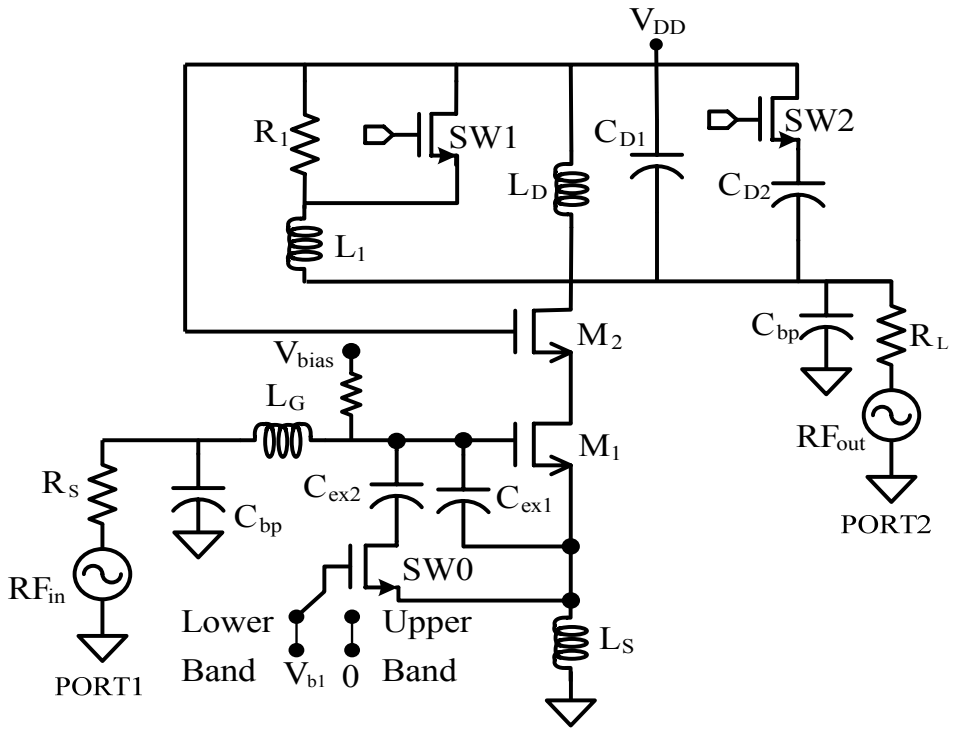

Figure 6.3: Complete circuit implementation of a reconfigurable LNA

Table 6.1 presents the corresponding components values used for reconfigurable multi-standard multi-band LNA. Figure 6.3 shows a complete circuit implementation of the reconfigurable LNA where bond pads capacitance at the input and output are included.

6.2 Simulation results

In the design of reconfigurable multi-standard multi-band LNA, the simulation was carried out using Spectre RF from Cadence design suite. Figures 6.4 to 6.17 illustrate the simulation results for the s-parameters, NF and linearity ($P1dB$ and $IIP3$) respectively.

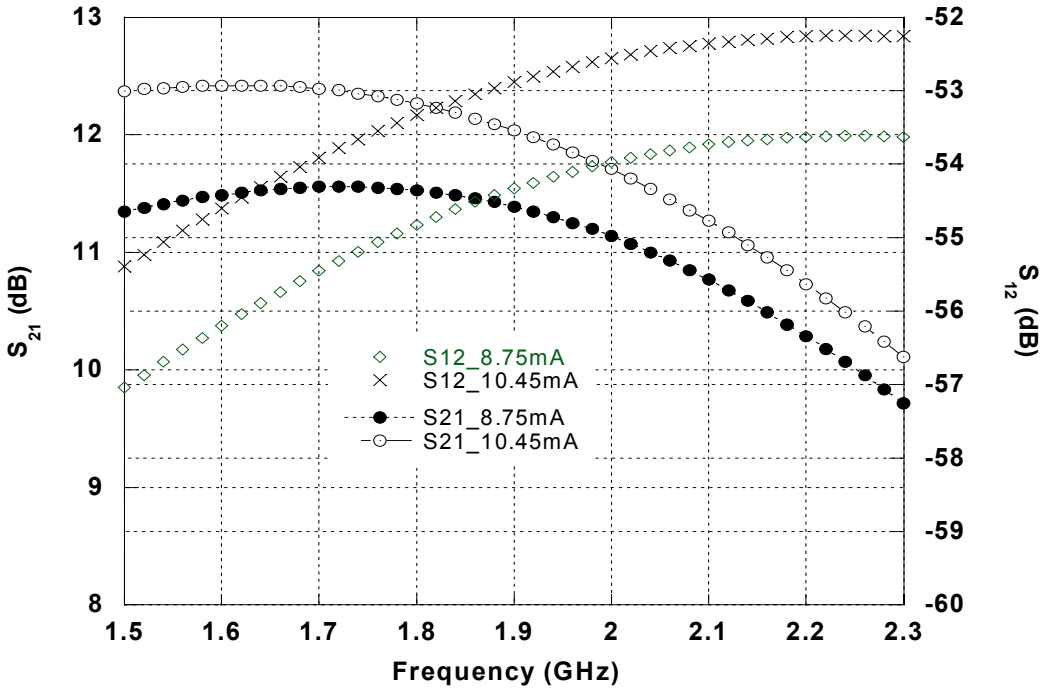

Figure 6.4: Forward gain and reverse isolation of reconfigurable LNA for upper band at 2GHz.

Figure 6.4 presents the S_{21} or power gain achieved in the simulation at upper band frequency of 2 GHz. The illustration shows value of about 12.4 dB at peak and remains approximately between 10.2 to 11.5 dB along the design bandwidth. Notice that the center frequency is shifted to 1.6 GHz. The reason behind this is due to the quality factor of the inductors used, which are derived at 2.4 GHz while this design is resonated at 2 GHz. Figure 6.4 also shows the reverse isolation or S_{12}. The attained value is about -52 dB at peak frequency and is believed to be a good reverse isolation as it exceeds the requirement which is typically -30 dB. Also shown are the simulation results for S_{21} and S_{12} simulated using different value of tail current.

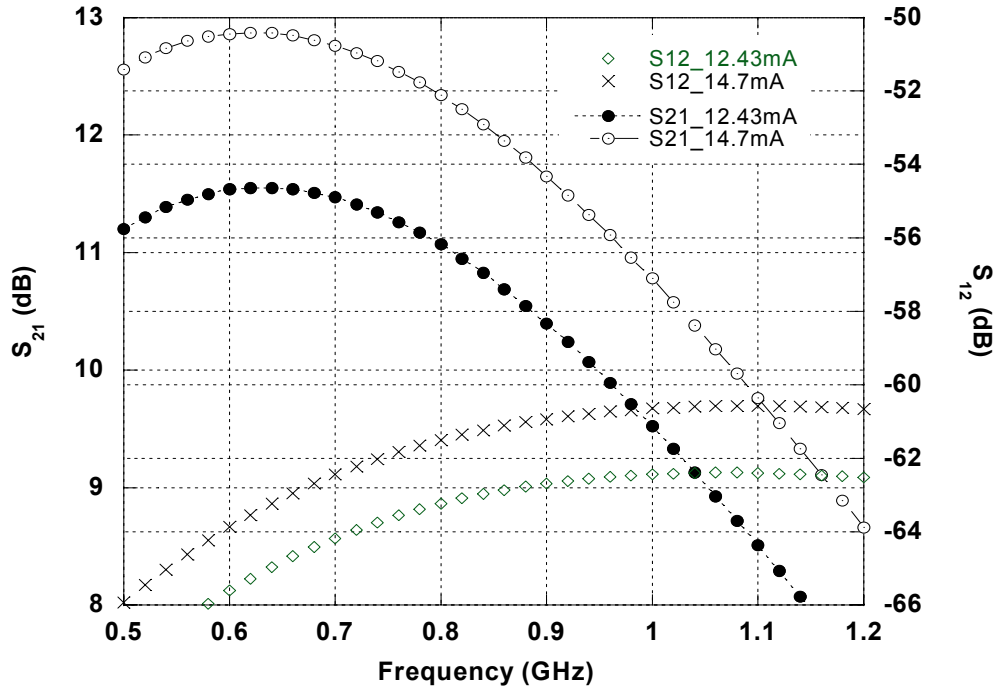

Figure 6.5: Forward gain and reverse isolation of reconfigurable LNA for lower band at 0.9GHz.

On the other hand, Figure 6.5 presents S_{21} or power gain achieved in the simulation at lower band frequency of 900 MHz. The graph shows value of about 12.9 dB at peak and remains approximately between 10.8 to 12.3 dB along the design bandwidth. Notice that the center frequency is shifted to 0.65 GHz. Also, this is due to the quality factor of the inductors used, which are derived at 2.4 GHz, while this design is resonated at 900 MHz. Figure 6.5 also shows the reverse isolation or S_{12}. The simulated value obtained is about -61 dB at peak frequency and is a good reverse isolation as it exceeds the requirement which is typically -30 dB. Also shown are the simulation results for S_{21} and S_{12} using different value of tail current.

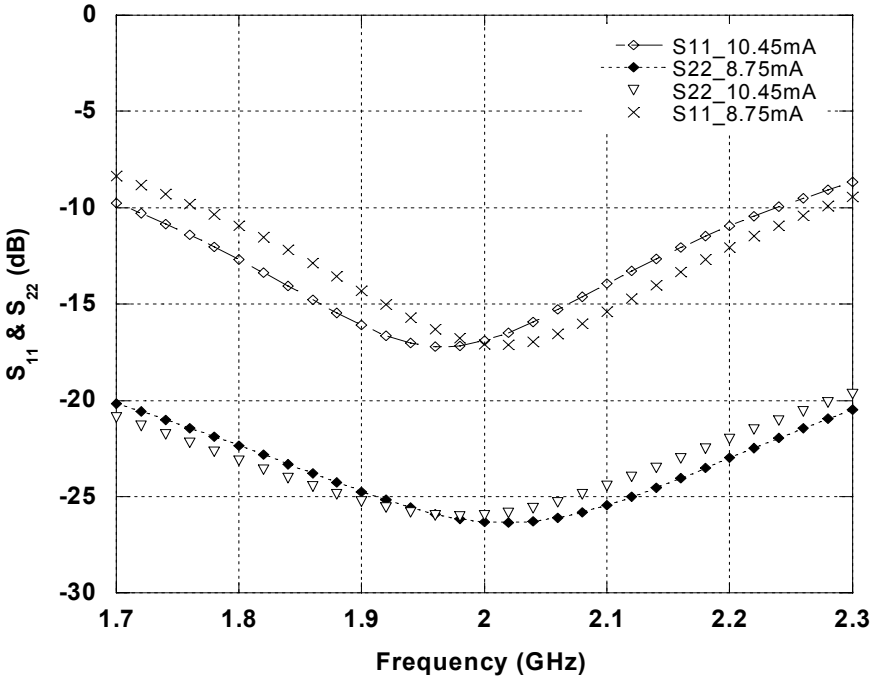

Figure 6.6: Input and output return losses of reconfigurable LNA for upper band at 2GHz.

Figure 6.6 shows the simulation results of input and output return losses of the LNA operating at upper band. The input return loss (S_{11}) achieved is -17.2 dB while output return loss (S_{22}) is about -26 dB at peak frequency. As shown in Figure 6.6, the input return loss remains under -10 dB which begins from 1.72 GHz and ends at 2.23 GHz. This yields more than the bandwidth required. For the output return loss, the bandwidth achieved is better, which is from 1.7 GHz to 2.3 GHz. However, the center frequencies for both parameters are slightly shifted to about 1.96 and 1.98 GHz for S_{11} and S_{22} respectively.

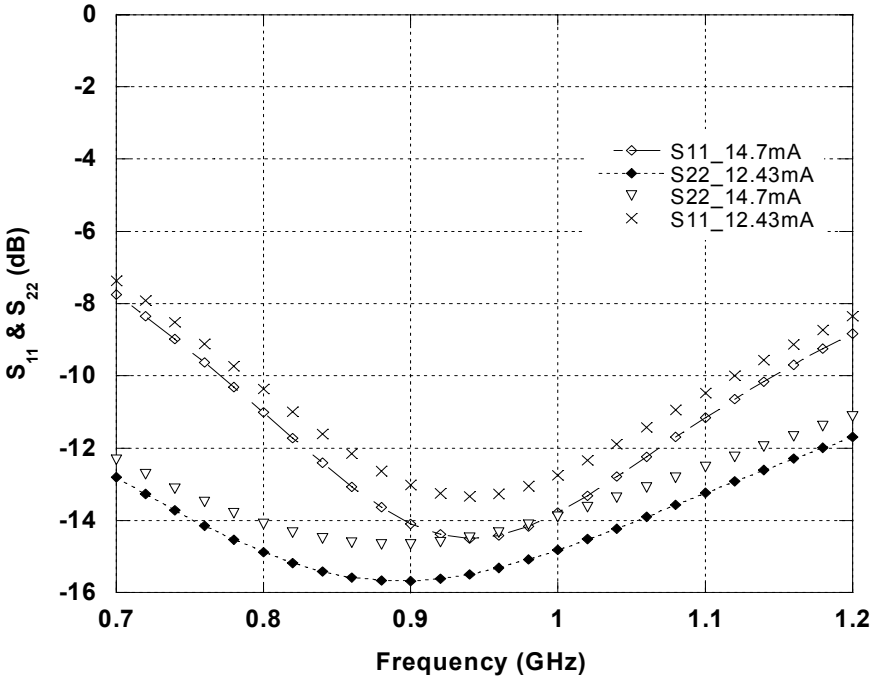

Figure 6.7: Input and output return losses of reconfigurable LNA for lower band at 0.9GHz.

Figure 6.7 shows the results of input and output return losses of the LNA operating at lower band. The input return loss (S_{11}) achieved is -14.5 dB while output return loss (S_{22}) is about -14.7 dB at peak frequency. As shown in Figure 6.7, the input return loss remains under -10 dB which begins from 780 MHz and ends at 1.14 GHz. This yields more than the bandwidth required. For the output return loss, the bandwidth achieved is better, which is from 700 MHz to 1.2 GHz. However, the center frequency for S_{11} is slightly shifted to about 940 MHz.

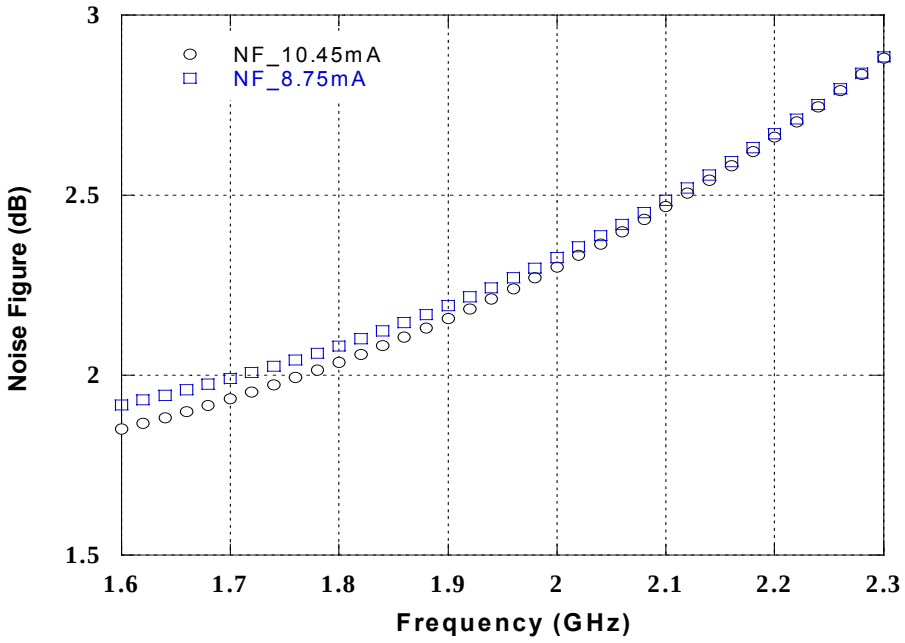

Figure 6.8: Noise figure of reconfigurable LNA for upper band at 2 GHz.

Figure 6.8 shows the NF of LNA for upper band. The achieved value is 2.3 dB. The NF is below 2.7 dB along the band of interest of 400 MHz. Meanwhile, Figure 6.9 shows the NF of LNA for lower band. The achieved value is 2.55 dB and is below 3 dB along the

200 MHz bandwidth of interest. The higher value of NF at lower band frequency is due to the resistance of the transistor $SW0$.

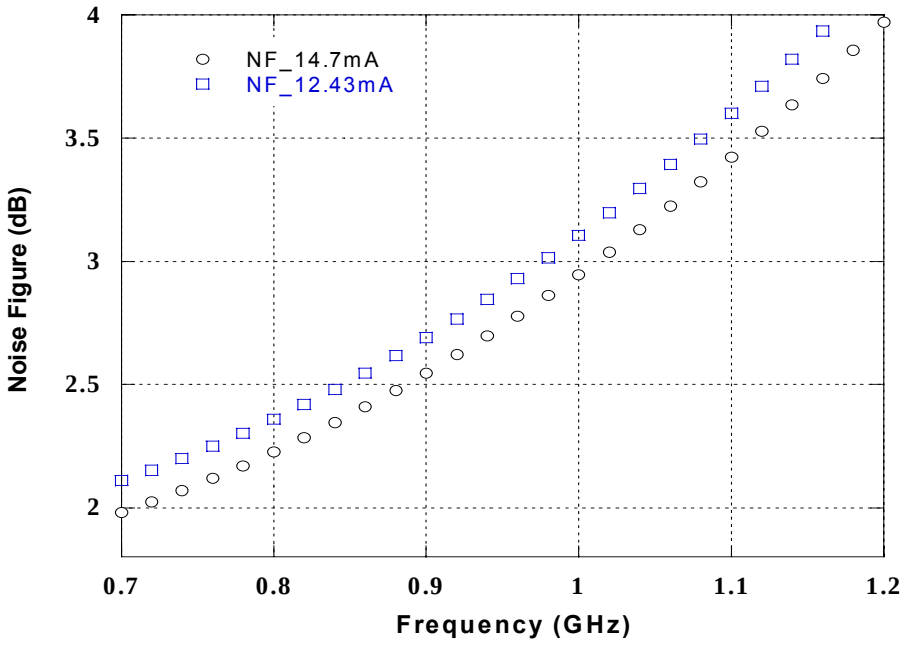

Figure 6.9: Noise figure of reconfigurable LNA for lower band at 0.9 GHz.

To check for the linearity requirement, a two-tone test for third-order intercept point was performed on the LNA. The two tones with equal power were applied at frequencies of 2 GHz and 2.05 GHz for upper band and 900 and 920 MHz for lower band respectively. For the upper band, the achieved $IIP3$ is +9.6 dBm as shown in Figure 6.10. It is good as it exceeds the targeted specification (refer to Table 2.5). Similarly, for lower band, the achieved $IIP3$ is +7.7 dBm as shown in Figure 6.11. It is also good as it exceeds the specification needed. Also shown in Figures 6.12 and 6.13 are the $IIP3$ values for the LNA simulated at different values of tail current.

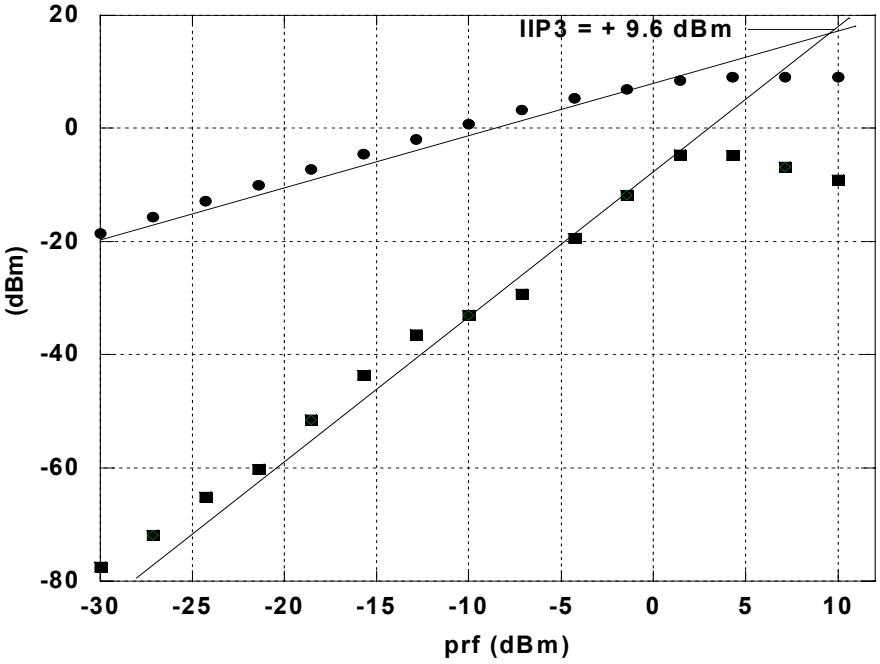

Figure 6.10: *IIP3* for upper band at 2 GHz with I_{load}=10.45 mA.

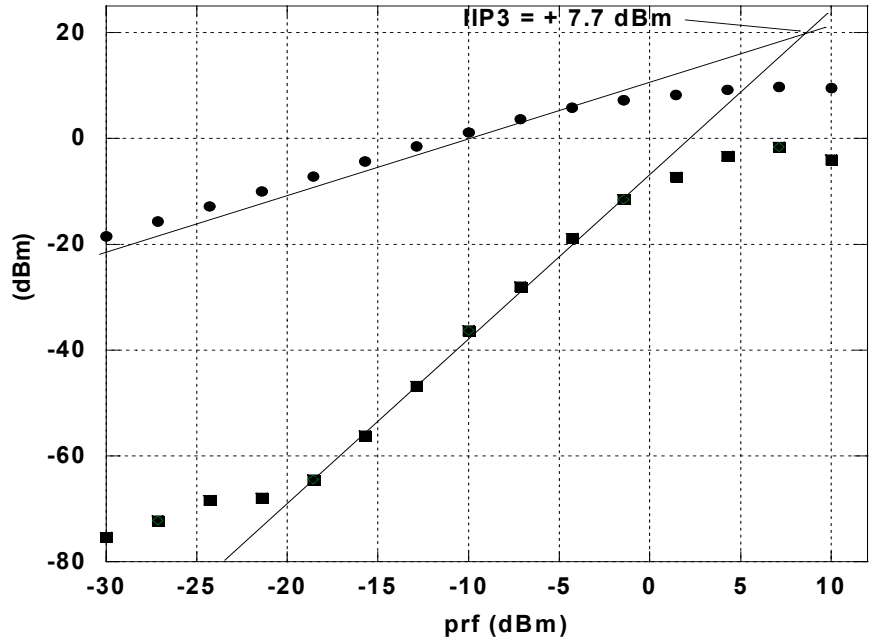

Figure 6.11: *IIP3* for upper band at 0.9 GHz with I_{load}=14.7 mA.

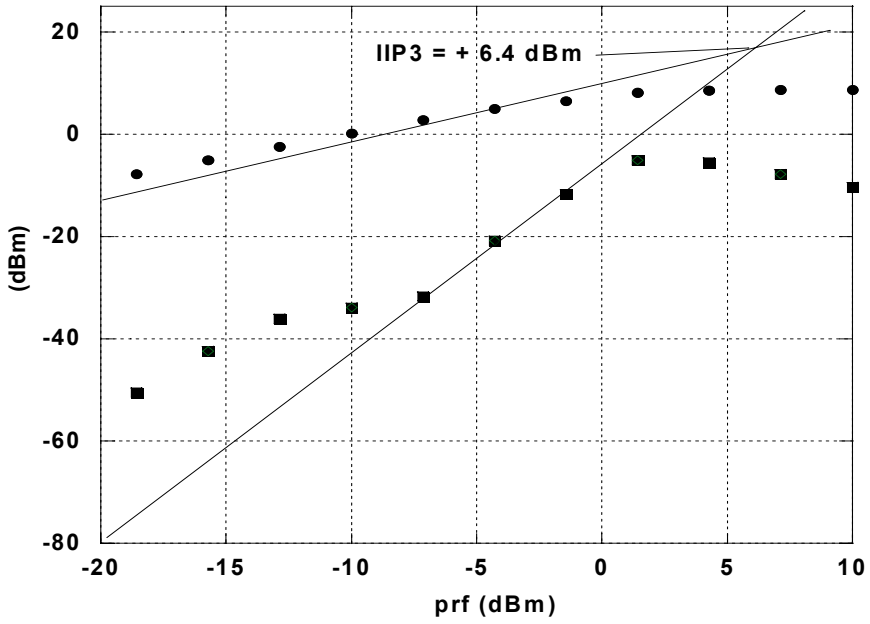

Figure 6.12: *IIP3* for upper band at 2 GHz with I_{load}=8.75 mA.

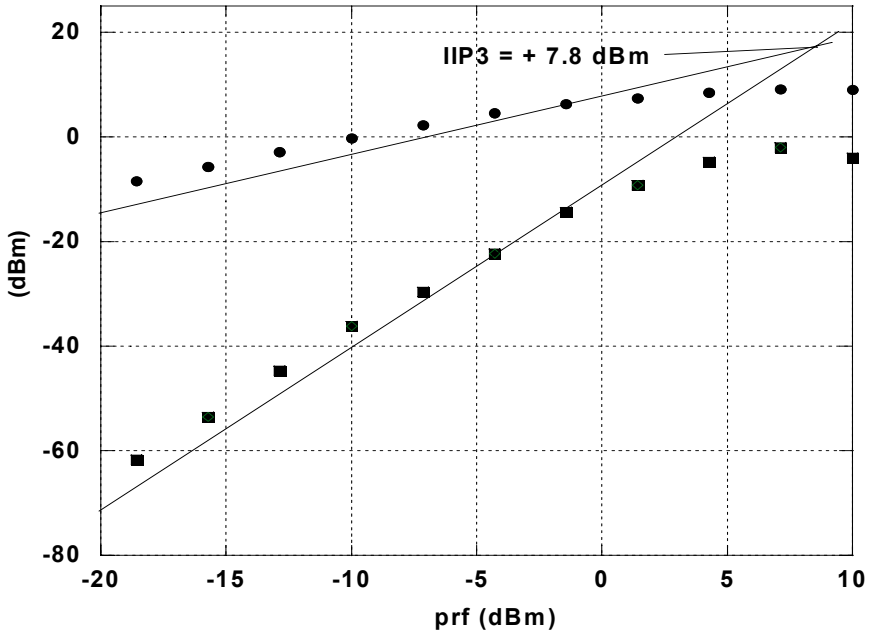

Figure 6.13: *IIP3* for upper band at 0.9 GHz with I_{load}=12.43 mA.

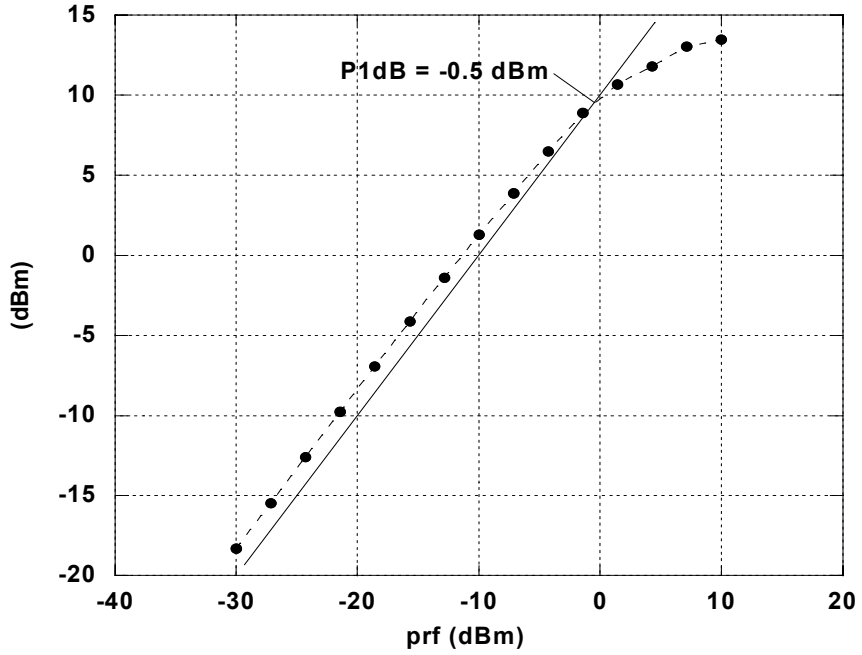

Figure 6.14: *P1dB* for upper band at 2 GHz with I_{load}= 10.45 mA.

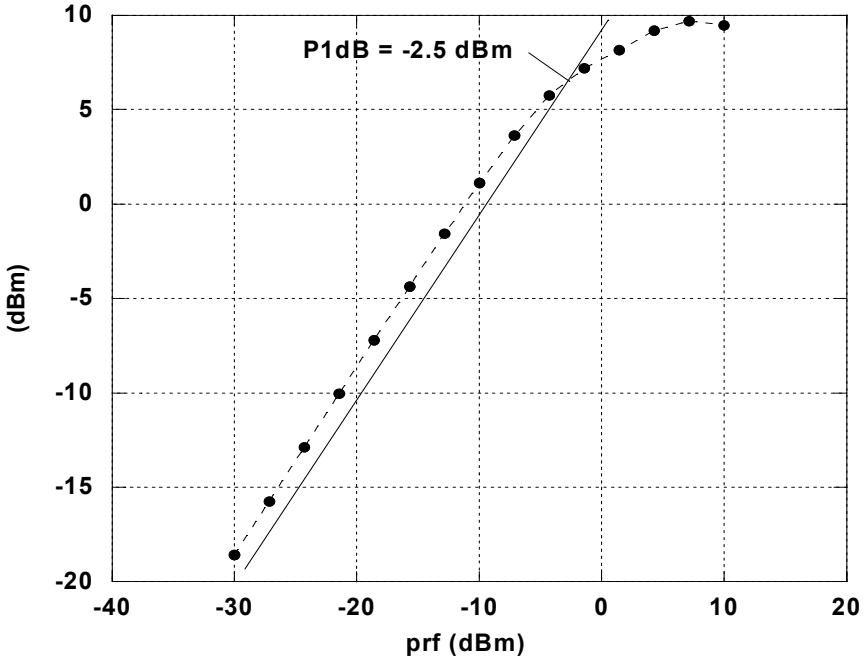

Figure 6.15: *P1dB* for upper band at 0.9 GHz with I_{load}= 14.7 mA.

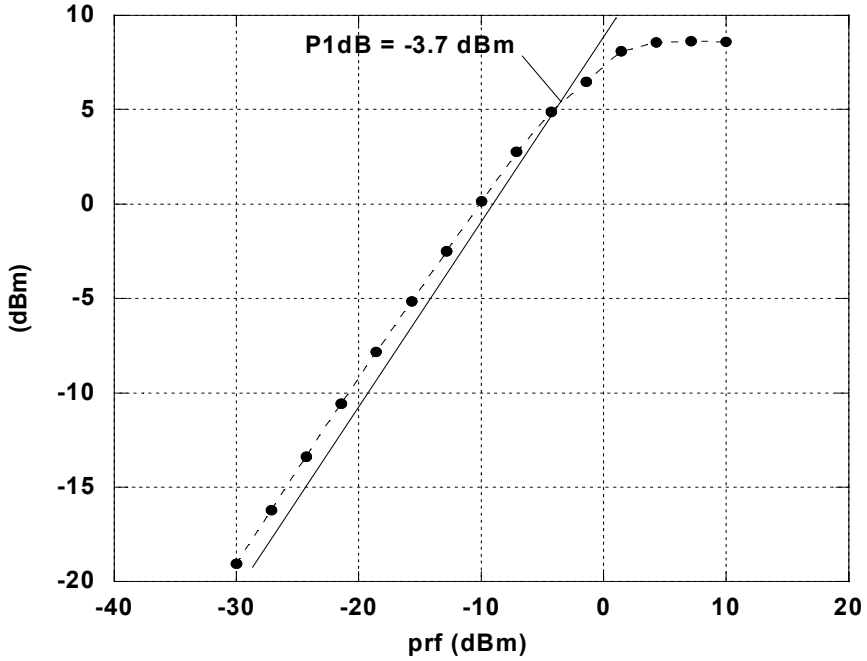

Figure 6.16: *P1dB* for upper band at 2 GHz with I_{load}= 8.75 mA.

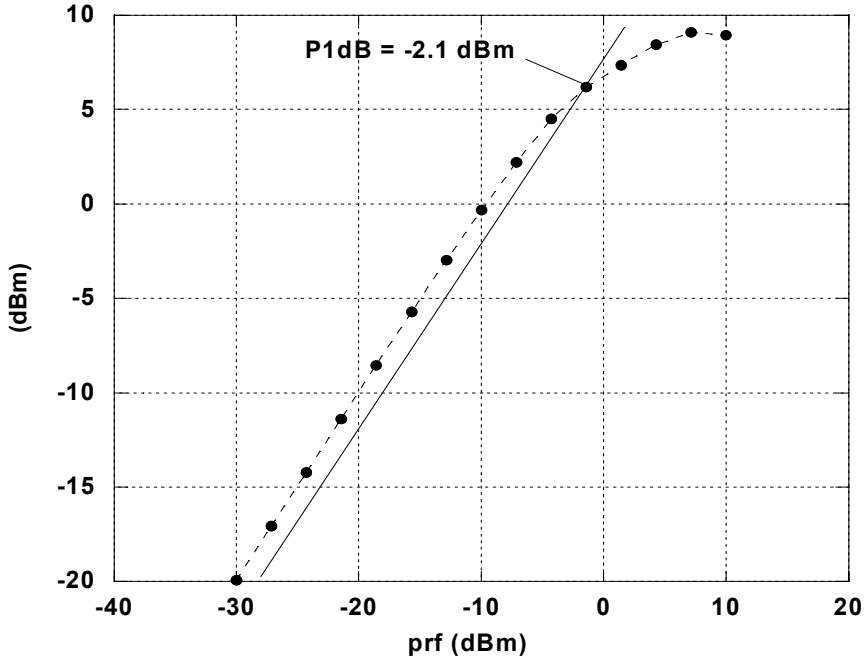

Figure 6.17: *P1dB* for upper band at 0.9 GHz with I_{load} = 12.43 mA.

Another measurement for linearity is the $P1dB$. As shown in Figures 6.14 and 6.15, the simulated values for $P1dB$ are -0.5 dBm for upper band and -2.5 dBm for lower band respectively. Also, notice that the achieved values exceed the targeted specification. In addition, for comparison, Figures 6.16 and 6.17 show the $P1dB$ of LNA simulated at different value of tail current.

6.3 Discussion of the results

Table 6.2 shows the comparable performance summary of the reconfigurable LNA versus the wide band LNA4 and LNA5.

For power gain, it shows that the reconfigurable LNA achieved a gain of almost similar to LNA5 for the 2 GHz operation. Meanwhile, for 900 MHz, the reconfigurable LNA achieved a 1.6 dB higher than that of LNA4. But, to achieve such a comparable gain for reconfigurable LNA at both modes of operation, power consumption will be higher compare to the wide band LNAs. This is due to different size of gate inductor (L_G) used for input matching which translates to a higher transconductance (g_m) of the transistor M_1. Moreover, to operate at lower band mode, the use of a higher value of external gate-source capacitance (C_{ex}), also contributes to higher power consumption due to the gain compensation. This is the price to gain full integration.

In terms of input and output return losses, the achieved results for reconfigurable LNA are comparable to the wide band LNAs. Meanwhile, for reverse isolation, the attained

results of the reconfigurable LNA are very close to the achieved results of the wide band LNA4 and LNA5.

Table 6.2: Performance summary of the reconfigurable LNA versus wide band LNAs

	Wide band LNAs		Reconfigurable LNA	
	LNA4 (900 MHz)	**LNA5 (2 GHz)**	**Lower band (900 MHz)**	**Upper band (2 GHz)**
$S_{21}\,(dB)$	11.3	12.6	12.9	12.4
$S_{12}\,(dB)$	- 62	- 53	- 61	-52
$S_{11}\,(dB)$	- 47.7	- 24.4	- 14.5	- 17.2
$S_{22}\,(dB)$	- 23.9	- 11.21	-14.7	- 26
$NF\ (dB)$	2.2	1.91	2.55	2.3
$IIP3\,(dBm)$	+ 8.28	+ 8.4	+ 9.6	+ 7.7
$P1dB\,(dBm)$	- 2.06	- 2.02	- 2.5	- 0.5
$Power\ (mW)$	12.8	12.2	26.5	18.8

Table 6.2 also shows a comparable result for NF between reconfigurable LNA and wide band LNAs. However, the achieved NF for both bands of the reconfigurable LNA is a bit higher than that of the wide band LNAs. This is due to the use of a higher value of gate

inductor L_G (higher series resistance) and the use of the switch $SW0$ at the input of the LNA. The use of the switch contributes extra noise to the circuit when the reconfigurable LNA operates at lower band mode due to the on resistance of $SW0$. However, looking at the simulated NF for lower band mode compared to upper band mode, the difference is marginal.

Regarding linearity, the attained results are comparable between reconfigurable LNA and wide band LNA4 and LNA5. For reconfigurable LNA, the achieved result for certain parameter, i.e. $P1dB$ is better than that of wide band LNA (-0.5 to -2.02 dBm). This could be explained by the use of more power consumption in the reconfigurable LNA compared to wide band LNAs.

6.4 Conclusion

In this chapter, the design and implementation of a reconfigurable multi-standard multi-band LNA has been presented. The design is basically build based on the wide band LNAs design introduced in Chapter 3. The reconfigurable LNA which use IDCS technique as the base, adopted new technique to achieve good output impedance matching and much better linearity without the need for buffer section. It has been shown that the reconfigurable LNA works in two modes of operation and proven by the simulation results.

This reconfigurable LNA is fully integrated and achieved a relatively minimal noise figure for a specified power budget. The concept of hardware sharing introduced for the purpose of gaining full integration reduces the chip area. This was done by using less and smaller inductors.

In terms of performance of the reconfigurable LNA, especially NF as one of the important parameter in the design, the simulation results show a good agreement with the targeted specification outline in Chapter 2.

CHAPTER 7

CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

7.0 Introduction

This chapter discusses the accomplishments of this research and how the work has addressed the objectives proposed in Chapter 1. Then, the conclusions that are drawn from the findings, as well as the limitations are presented. Also, recommendations for future work are outlined in this chapter.

The findings of this thesis, such as ideas, designs and implementations of the multi-standard multi-band LNAs have been reported in related publications as shown in the 'List of Publications' section of this thesis. Section 7.1 of this chapter presents the specific tasks carried out to accomplish the successful completion of this research and describes how the accomplished work has addressed the goals outlined in Chapter 1.

Then, Section 7.2 highlights some recommendations for future research directions and possible works that could be applied to the study described in this thesis.

7.1 Summary and achievements of the research

In Chapter 2, a comprehensive literature review of the present state-of-the-art of mobile devices concluded with the limitations in the current RF receiver for multi-standard system. For instance, the main architecture of mobile device uses parallel architecture which is complex, costly and consumes relatively high power. Therefore, the proposed RF receiver architecture could solve this problem by using a reconfigurable concept. The reconfigurable architecture will have the capability to support multiple standards in one system but with less components which results in simpler, more compact, less expensive and less power consumption.

Following Chapter 2, are the major works involving the designs and implementations of the LNA for multi-standard system which were presented through Chapters 3 to 6. The designs and implementations of such LNA were developed in two parts using two CMOS technologies–0.25 µm and 0.18 µm. First part involved the process of designing wide band LNAs in two bands of interest; lower frequency band (800 to 1000 MHz) and upper frequency band (1800 to 2200 MHz). These two frequency bands are specifically targeted for GSM and 3G systems which include most of the mobile communication standards currently in use worldwide. Then, after successfully designing the wide band LNAs, the reconfigurable LNA was developed based on the designs of the wide band

LNAs. This LNA which was implemented as a single circuit is made to have the capability to support two bands of interest by means of reconfigurability.

Finally, the research carried out in this work has specifically achieved the followings results:

1. The RF receiver system simulation which has been carried out to find the mutual relationship between RF receiver system and RF components specifications provides the minimum and optimum requirement of the LNA's specifications. This knowledge is essential to RF engineers to further understand the RF system and the specifications of RF components for such system. This will help in developing better RF system.

2. The development and implementation of wide band LNAs provides a new approach for designing the multi-standard multi-band LNA for a relatively wider band system especially for mobile communication standards. This is because most of the wide band designs were developed either for a combinations of few mobile standards and for standards other than mobile communication i.e. WLAN, etc. These wide band LNAs will reduce the number of LNA in the current system significantly and cover most of the standards currently in use world wide as clearly stated in Tables 2.1 and 2.2.

3. The development and implementation of the reconfigurable multi-standard multi-band LNA will further provide new methodology in the design of multi-standard LNA for multi-standard system. This LNA provides a much better reduction of the component count in the RF receiver system. Consequently, RF receiver architecture will be less complex, more power efficient and cost effective compared to the parallel architecture.

4. The unbuffered technique which was developed to provide the output impedance matching and improves the linearity performance of the wide band LNAs provides an improved methodology in the design of the LNA for multi-standard system. This technique which was also employed by the reconfigurable LNA consumes relatively lower power consumption compared to the design which uses buffer circuit for matching purposes.

In conclusion of this section, generally, even though the targeted works were accomplished, but there were issues and challenges in the design of such LNA. One of the biggest challenges is the use of specific fixed values of the inductors (with different Q values resonated at 2.4 GHz) particularly when dealing with the 0.18 μm technology provided by the foundry. The use of these inductors set the limits of the optimisations that could be made. In other words, the results obtained are compromised between the components used and the targeted specifications. Hence, there is a need for custom made inductors for particular LNA design. However, designing such inductors is not an

easy work. It is entirely new field of research. For instance, works in references [98] and [99] were devoted only for the designs and optimisations of the inductors.

In addition, apart from the fixed inductors, other issues such as trade-off between power consumption and linearity, full integration issue, parasitic components (when dealing with layout implementation), etc. make the design of the multi-standard multi-band LNA really challenging work.

7.2 Recommendations for future work

The work carried out in this research was mostly based on CMOS technology provided by the foundry. As part of the design kit, the inductors included are fixed to specific values. As mentioned before, one of the biggest challenges in the design of the LNA for multi-standard system was the use of these fixed value inductors. Therefore, the following further research is recommended as extension to this work:

1. Designing accurate custom made inductors for the reconfigurable LNA which could compromise between the bands of interest either at lower frequency band or upper frequency band. Therefore, the best optimisation of the circuit could be achieved. In addition, these inductors should be designed in such a way it has a better quality factor Q, thus it will reduce the NF of the circuit even more. With custom made inductors, optimisation of the circuit for even lower NF figure could

be easier especially when there is a need for a flat NF over the wide band of the interest (i.e. 400 MHz bandwidth for upper band).

2. In term of technology, it has been proven that the small technology i.e. 0.18 µm uses lower power consumption compared to 0.25 µm. Therefore, the design of LNA should be done using a smaller size technology i.e. 0.13 µm or 90 nm. But, as the device shrinking, lower transconductance of the transistor could put more challenges in the design of multi-standard multi-band LNA especially when dealing with the NF optimisation.

3. In relation to the quality factor of the inductors, there is a major work in RF Micro Electro Mechanical System (MEMS) carried out world wide. MEMS is an enabling technology used in the design of new generation of RF MEMS components such as inductors, capacitors, switches, etc. [100-101]. These MEMS components can achieve very high-Q, thus it is the best option to replace CMOS passives components in LNA implementation [101]. MEMS technology offers low cost, low power consumption, higher performance, smaller size devices and weight and is compatible with the current CMOS technology platform [100-103].

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APPENDIX A:

THE REFLECTION COEFFICIENT OF THE LOADED TRANSMISSSION LINE

Figure A.1 shows the loaded transmission line which could be used to obtain the reflection coefficient Γ [93].

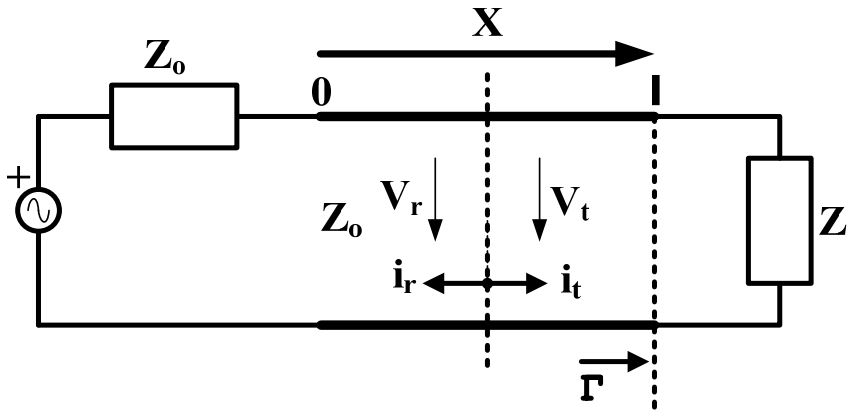

Figure A.1: Transmitted and reflected voltages and currents [93]

The resistive impedance is referred as Z_o. Therefore, at any particular location of x on the line we find,

$$V_X = V_t + V_r \qquad \text{(AA.1)}$$

and

$$I_X = I_t - I_r \tag{AA.2}$$

At the end of the line, the following equations have to be satisfied:

$$Z = \frac{V_t + V_r}{I_t - I_r} = Z_o . \frac{1+\Gamma}{1-\Gamma} \tag{AA.3}$$

where reflection coefficient is defined as

$$\Gamma = \frac{V_r}{V_t} = \frac{I_t}{I_r} \tag{AA.4}$$

and, in terms of impedances, we get

$$\Gamma = \frac{Z - Z_o}{Z + Z_o} \tag{AA.5}$$

APPENDIX B:

NON-QUASI STATIC EFFECT OF CMOS TRANSISTOR

Non-Quasi Static Effect (NQS) is important in the design of high frequency amplifier as it limits the gain and noise performance [75] [93]. Figure B.1 shows the first order model that represents the NQS effect.

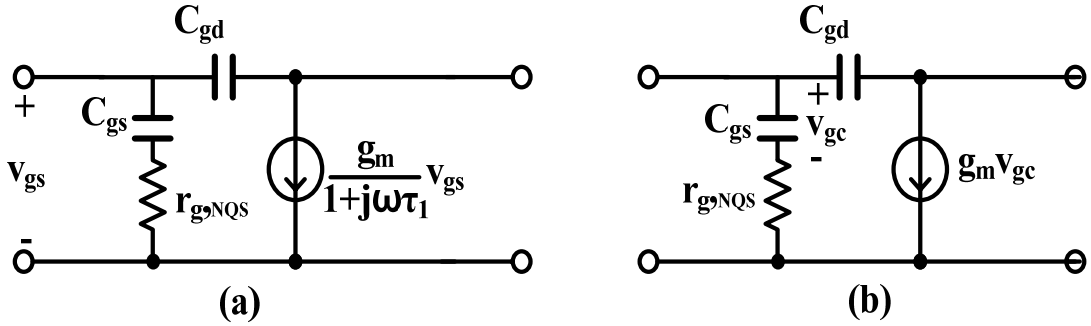

Figure B.1: A first order non-quasi static small-signal model for transistors operating in strong inversion: (a) valid in both linear and saturation region (b) valid in saturation region only [93].

As seen in Figure B.1, NQS model uses a resistance which is in series with the gate-source capacitance to model the NQS effect. This resistance is denoted as the NQS gate resistance and the effective resistance seen by the gate to source capacitance. Practically, in most cases, τ_1 of the model as shown in Figure B.1 (a) is replaced by $\tau_1 - \tau_2$ [75]. Therefore, equation (AB.1) mathematically described this resistance as

$$r_{g,NQS} = \frac{\tau_{g,NQS}}{c_{gs}} = \frac{\tau_1 - \tau_2}{c_{gs}} \tag{AB.1}$$

where τ_1 and τ_2 are given by

$$\tau_1 = \frac{2}{5}\frac{1}{\omega_T} f_1\left(\frac{V_{DS}}{V_{DS\,sat}}\right) \tag{AB.2}$$

$$\tau_2 = \frac{1}{5}\frac{1}{\omega_T} f_2\left(\frac{V_{DS}}{V_{DS\,sat}}\right) \tag{AB.3}$$

and ω_T is the cut-off frequency of the transistor. f_1 and f_2 are the functions of $V_{DS}/V_{DS_{sat}}$. In saturation region, f_1 and f_2 are simply equal to 1.

Finally, based on (AB.1) to (AB.3), we get

$$r_{g,NQS} = \frac{1}{5g_m} \tag{AB.4}$$

APPENDIX C:

PASSIVE COMPONENTS OF THE DESIGN KIT

This Appendix provides the information about the passive components from the design kit provided by Silterra Malaysia. Table AC.1 shows the performance summary of the inductors.

While for capacitor, the type of capacitor included in the design kit is metal-insulator-metal (MIM).Its value could be varied accordingly from 18 fF to 915 fF per device.

On the other hand, for resistor, two varieties of poly resistors are included in the design kit. They are poly resistor 1 with variable value start from 26.95 Ω to about 84.5 KΩ per device and poly resistor 2 with variable value start from 6.71 Ω to about 7.4 KΩ per device respectively.

Table AC.1: Performance summary of the inductors

Inductance (H) 2.4 GHz	Quality factor at 2.4 GHz
1.65	5.72
2.26	7.19
4.21	8.21
6.94	8.04
7.66	7.57
10.7	6.97
12.9	6.47
15.8	7.57
20.4	4.81
22.9	4.0

APPENDIX D:

S-PARAMETERS OF THE LNA

S-parameters as the important specifications of the LNA have the advantage that they can be measured by matching the source and load impedances to the reference impedance. A diagram of an s-parameters representation of a two-port network is shown in Figure D.1 [93] [104].

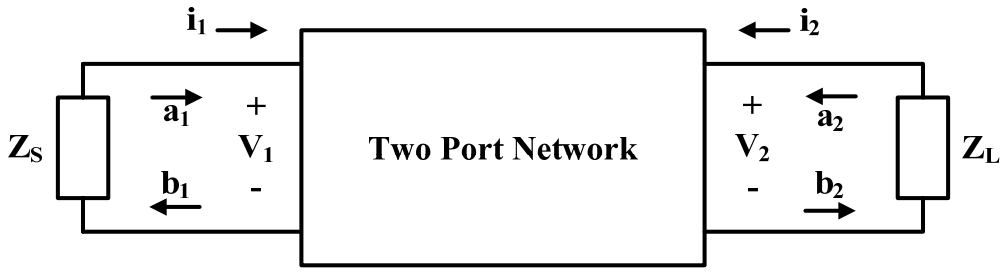

Figure D.1: S-parameters representation of a two-port network

Basically, the idea behind this representation is to measure the normalized incident voltage wave a_i entering the system at port i, as well as the corresponding reflected voltage wave b_i leaving port i. The normalized incident and reflected voltage waves a_i and b_i are related to the terminal voltage and currents at port i by the following equations:

$$a_i = \frac{v_i + Z_o i_i}{2\sqrt{Z_o}} \tag{AD.1}$$

$$b_i = \frac{v_i - Z_o i_i}{2\sqrt{Z_o}} \tag{AD.2}$$

where Z_o is the reference impedance (assumed real in this analysis, and usually equal to 50 Ω). For the network shown in Figure D.1, the contributions from the two ports can be combined to form (AD.3), in matrix form.

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{AD.3}$$

where $S_{11}, S_{12}, S_{21}, and\ S_{22}$ are measured across ports 1 and 2. Then, by expanding the scattering matrix, the following equations can be obtained:

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_{2=0}} \tag{AD.4}$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_{1=0}} \tag{AD.5}$$

$$S_{21} = \left.\frac{b_1}{a_1}\right|_{a_{2=0}} \tag{AD.6}$$

$$S_{22} = \left.\frac{b_1}{a_2}\right|_{a_{1=0}} \tag{AD.7}$$

where S_{11} is interpreted as the ratio between the reflected voltage wave and the incident voltage wave at port 1 with the output port properly terminated. It is also known as input return loss. The condition for a port being properly terminated is that its load impedance must match the characteristic impedance. The output or input impedance of the two-port network does not have to match the characteristic impedance. Meanwhile, S_{12} is known as reverse isolation, S_{21} as power gain, and S_{22} as output return loss respectively.

APPENDIX E:

LINEARITY OF THE LNA

Ideally, two-port networks are linear, and in many analyses this assumption is made because the input signal is small enough such that the non-linear effects of the two-port network can be ignored. However, in LNA design, linearity is a key issue because it must be able to maintain linear operation even in the presence of large input signals. The measurement of linearity are usually done by using two parameters, IIP_3 and $P1dB$. To get a better understanding on how these two specifications measured let us consider one signal $S_{in}(t)$ as in (AE.2) applied to the input of a two-port network [93] [104]. By doing that, non-linearity product could be observed at the output called intermodulation

$$S_{out} = A_1 S_{in} + A_2 S_{in}^2 + A_3 S_{in}^3 + \ldots. \quad \text{(AE.1)}$$

where A_1 , A_2 , A_3 are constants,

and

$$S_{in}(t) = S_1 \cos(\omega_1 t) + S_2 \cos(\omega_2 t) \quad \text{(AE.2)}$$

Therefore, output can be expanded in a power series as in (AE.1), and by substituting (AE.2) into (AE.1), the linear first term will be obtained as in (AE.3), represents the linear terms of the system, if the system is ideal or the system is completely linear.

$$A_1 S_{in}(t) = A_1 \left[S_1 \cos(\omega_1 t) + S_2 \cos(\omega_2 t) \right] \qquad \text{(AE.3)}$$

The second term is now therefore:

$$\begin{aligned} A_2 S_{in}^2 = {} & \frac{A_2 S_1^2}{2} \left[\cos(2\omega_1 t) + 1 \right] \\ & + \frac{A_2 S_2^2}{2} \left[\cos(2\omega_2 t) + 1 \right] \\ & + A_2 S_1 S_2 \left[\cos(\omega_1 + \omega_2) t + \cos(\omega_1 - \omega_2) \mathrm{t} \right] \end{aligned} \qquad \text{(AE.4)}$$

Then, expanding the third term, the following is obtained:

$$\begin{aligned} A_3 S_{in}^3 = {} & \frac{A_3 S_1^3}{4} \left[\cos(3\omega_1 t) + 3\cos(3\omega_1 t) \right] \\ & + \frac{A_3 S_2^3}{4} \left[\cos(3\omega_2 t) + 3\cos(3\omega_2 t) \right] \\ & + \frac{3}{4} A_3 S_1 S_2^2 \left[2\cos(\omega_1 t) + \cos(2\omega_2 + \omega_1) \mathrm{t} + \cos(2\omega_2 - \omega_1) \mathrm{t} \right] \\ & + \frac{3}{4} A_3 S_1^2 S_2 \left[2\cos(\omega_2 t) + \cos(2\omega_1 + \omega_2) \mathrm{t} + \cos(2\omega_1 - \omega_2) \mathrm{t} \right] \end{aligned} \qquad \text{(AE.5)}$$

From (AE.4) and (AE.5), it can be observed that second order intermodulation terms are produced at $(\omega_1 + \omega_2)$, and $(\omega_1 - \omega_2)$. While, third order intermodulation terms are produced at $(2\omega_1 \pm \omega_2)$, and $(2\omega_2 \pm \omega_1)$. The rest of the terms of (AE.4) and (AE.5) are harmonic distortions, other non-linearity products produced by the two port network. Figure E.1 shows the frequency positions of the distortion terms.

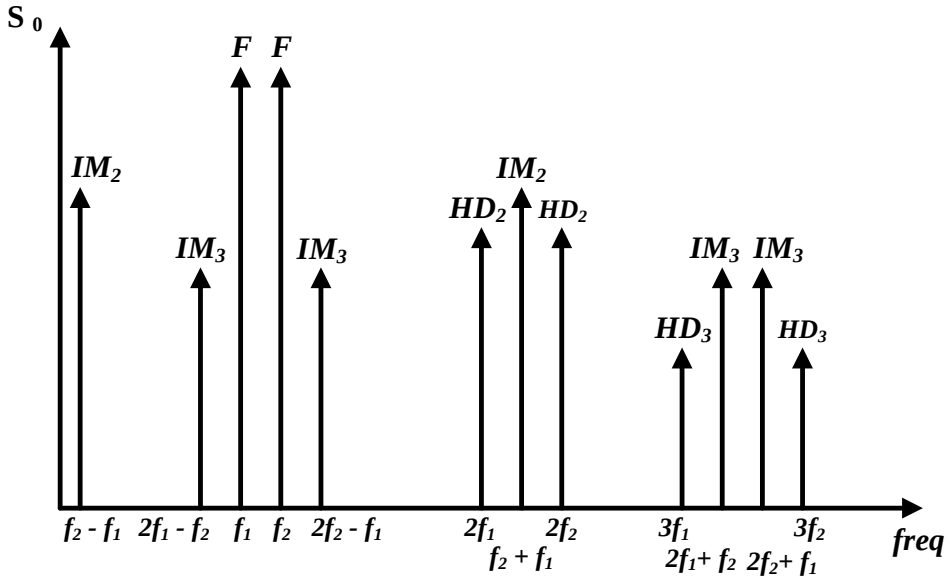

Figure E.1: Frequency locations of distortion terms [104]

The following equation defines the third order intermodulation:

$$IM_3 = \frac{Amplitude_{(2\omega_{1\pm}\omega_2),(2\omega_{1\pm}\omega_2)}}{Amplitude_{\omega_1,\omega_2}} \qquad \text{(AE.6)}$$

From (AE.6), the fractional intermodulation term is:

$$IM_3 = \frac{3A_3}{4A_1} S_1^2 \qquad \text{(AE.7)}$$

with the assumption that $S_1 = S_2$.

IIP3

The measurement of the amount of third order non-linearity in a two-port network is called third order intercept point. Since the third order non-linearity is proportional to the input signal cubed, while the fundamental is increasing only linearly with input signal, there will be a point at which the amplitudes of the fundamental and the third intermodulation meet. The input signal, S_1 , at which this occurs is defined as the input-referred third order intercept point (IIP_3). Solving for S_1 using (AE.7), the following equation for IIP_3 is obtained [93] [104].

$$IIP_3 = \sqrt{\frac{4}{3}\left|\frac{A_1}{A_3}\right|} \qquad \text{(AE.8)}$$

P1dB

It is known that the third order term in the power series can either cause gain compression or gain expansion depending on its sign. If we assume that the sign between A_1 and A_3 are different, then gain compression will occur, and then compression point can be measured. $P1dB$ is a measure of the power of the input signal such that it causes the third order non-linearity to decrease the linear gain by 1 dB. Therefore mathematically (AE.9) is obtained:

$$20\ log\left(1+\frac{3A_3}{4A_1}S_1^2\right)=-1\ dB \qquad \text{(AE.9)}$$

Then, after solving for S_1 in (AE.9), we get [93] [104]:

$$P1dB=\sqrt{\frac{4}{3}\left|\frac{A_1}{A_3}\right|}\sqrt{0.11}\approx\sqrt{0.145\left|\frac{A_1}{A_3}\right|} \qquad \text{(AE.10)}$$