A Reconfigurable Root Raised Cosine Filter For a Mobile Receiver

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I dedicate this thesis to my dear son whom will enter this world in October 2003 and to my dear wife Daniela

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List of Acronyms

μs	Micro seconds
μW	Micro Watts
1G	First Generation
2G	Second Generation
3G	Third Generation
3GPP	Third Generation Partnership Project
ACI	Adjacent Channel Interference
ACLR	Adjacent Channel Leakage Ratio
ACP	Adjacent Channel Protection
ACS	Adjacent Channel Selectivity
ADC	Analog to Digital Converter
AMPS	Advanced Mobile Phone System
ASIC	Application Specific Integrated Circuit
BER	Bit Error Rate
BPSK	Binary Phase Shift Keying
BS	Base Station
CCI	Co-Channel Interference
CCTrCH	Coded Composite Transport Channel
cdfs	Cumulative distribution functions
CDMA	Code Division Multiple Access
CMOS	Complementary Metal Oxide Semiconductor
COI	Cell of Interest
COST	COperation européenne dans le domaine de la recherche Scientifique et Technique
DAC	Digital to Analog Converter
dB	Decibels
dBW	dB Watts
DEC	Digital Error Correction
DPCH	Dedicated Physical Channel
DSP	Digital Signal Processor
E	Mean

Eb/No	Bit-energy to Interference ratio
Es/No	Symbol-energy to Interference Ratio
EVM	Error Vector Magnitude
FDD	Frequency Division Duplex
FDMA	Frequency Division Multiple Access
FIR	Finite Impulse Response
FPGA	Field Programmable Gate Array
FM	Frequency Modulation
FWR	Full Wave Rectifier
GHz	Giga hertz
GSM	Global Systems for Mobile communications
HPF	High Pass Filter
Hz	Hertz
I	In-phase
I/O	Input / Output
IC	Integrated Circuit
IFFT	Inverse Fast Fourier Transform
IIR	Infinite Impulse Response
ISI	Inter-Symbol Interference
Kbps	Kilo bits per second
kHz	Kilohertz
LMS	Least Mean Square
LNA	Low Noise Amplifier
LPF	Low Pass Filter
LSB	Least Significant Bit
LUT	Look-Up Table
m	Meters
Mbps	Mega bits per second
Mcps	Mega chips per second
MER	Modulation Error Ratio
MHz	Megahertz
MS	Mobile Station
MSB	Most Significant Bit
mW	Milli Watts
NAMPS	Narrowband AMPS
NMT-900	Nordic Mobile Telephone System
ns	Nano seconds
OVSF	Orthogonal Variable Spreading Factor
PDC	Pacific Digital Cellular
pdfs	Probability density functions
PRACH	Physical Random Access Channel
PSTN	Public Switched Telephone Network
Q	Quadrature
QoS	Quality of Service
QPSK	Quadrature Phase Shift Key

RF	Radio Frequency
RPA	Reconfigurable Pipelined Architecture
RRC	Root Raised Cosine
RSN	Residue Number System
RTL	Register Transfer Language
Rx	Receiver
S/H	Sample and Hold
SIR	Signal to Interference Ratio
SNR	Signal to Noise Ratio
SoC	System-on-a-Chip
STD	Standard deviation
TACS	Total Access Cellular System
TDD	Time Division Duplex
TDMA	Time Division Multiple Access
TPC	Transmit Power Control
Tx	Transmitter
UMTS	Universal Mobile Telephone Service
USDC	United States Digital Cellular
UTRA	UMTS Terrestrial Radio Access
UTRAN	UTRA Network
V	Volts
VHDL	Very High Speed Integrated Circuit Hardware Description Language
WCDMA	Wideband CDMA

Declaration of Originality

I hereby declare that the research in this thesis and the thesis itself was entirely composed and compiled by myself in the School of Electrical Engineering, Faculty of Science, Engineering and Technology at Victoria University.

Ronny Veljanovski

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Abstract

Over the last decade, the growth of second generation (2G) digital communications has been explosive. Now wireless communications is evolving to third generation (3G), where it will offer wideband data services and multimedia wideband products and services such as video conferencing and high speed Internet over a mobile phone. Amid these high-tech feature packed mobile devices, there is a major bottleneck of cost. The major cost factor in mobile devices is battery life.

Time division duplex (TDD) is one of the duplex modes for wideband code division multiple access (WCDMA) also referred as universal mobile telephone service (UMTS) terrestrial radio access (UTRA) that offers such services. The key driver and main objective of UTRA-TDD systems are high bit rate services up to 384 Kilo bits per second (kbps) for high-mobility users and up to 2 Mega bits per second (Mbps) for low-mobility users. In TDD, adjacent channel interference (ACI) is experienced from adjacent channel base stations and adjacent channel mobile stations dependent on frame synchronisation and channel asymmetry.

This thesis analyses the UTRA-TDD downlink operation with respect to an indoor office environment. A key parameter investigated is the ACI in the system since the jamming entity and victim entity can be in close proximity in the same geographical region. The interference analysis shows that ACI is greater when neighbouring cells are not synchronised, therefore posing a greater threat. It is revealed that the strength of ACI power is dependent on various dynamics. It is never constant and varies greatly. Therefore, it is inefficient to employ a standard fixed length receiver channel filter with a high order to mitigate ACI. The high order ensured the filters' attenuation caters for the worst-case environment set by the specifications of the system. The disadvantage is that the worst case is not the only operating condition.

One significant challenge for developers of 3G wireless systems is the design of digital filters for mobile terminal receivers. Due to the ACI issue in UTRA-TDD, complex high order digital receiver channel filters are required but are a burden on battery power in the mobile. As a consequence, a new reconfigurable root raised cosine (RRC) channel filter is introduced. The reconfigurable filter automatically monitors in-band and out-of-band signal powers and intelligently chooses the required filter length (between 5 and 65) to meet the signal-to-noise ratio (SNR), thus, yielding optimum power efficiency for the filter and extended battery life in the mobile terminal. The minimum filter length was found by an inter-symbol interference (ISI) investigation as lowering the filter length in the receiver has an impact on the SNR of the system.

Moreover, a reconfigurable-pipelined architecture (RPA) based on similar reconfigurable principles as the RRC filter is developed. This architecture consists of

the channel filter as well as a pipeline analog to digital converter (ADC). The length of the filter and the word length of the ADC are variable (4 to 16 bits) and also depend on in-band and out-of-band power ratios. This architecture further reduces the power consumption in the mobile receiver, as the ADC is a key player in the receiver with high cost demands.

Index Terms: UTRA-TDD, reconfigurable root raised cosine filter, UMTS, pipeline analog-to-digital converter.

List of Publications

Peer Reviewed International Journal Publications

[1] Veljanovski, R., Singh, J., and Faulkner, M. 'Design and Implementation of a Reconfigurable Filter', IEE Electronics Letters, Vol. 39, no. 10, pp 813-814, 2003

[2] Veljanovski, R., Stojcevski, A., Singh, J., Faulkner, M., and Zayegh, A. 'A Low Cost Reconfigurable Architecture for a UMTS Receiver', Accepted for publication in IEICE Transactions, Special Issue on Software Defined Radio Technology and Applications, 2003

[3] Veljanovski, R., Singh, J., and Faulkner, M. 'Statistical analysis of adjacent channel protection factors for UTRA-TDD/FDD in a simulation environment', Accepted for publication in Best of Book Journal, AMSE Press, 2003

[4] Veljanovski, R., Stojcevski, A., Singh, J., Faulkner, M., and Zayegh, A. 'Reconfigurable Architecture for an UTRA-TDD System', IEE Electronics Letters, Vol. 38, no. 25, pp 1732-1733, 2002

International Conference Publications

[1] Veljanovski, R., Singh, J., and Faulkner, M. 'A channel filter with variable adjacent channel selectivity for UTRA-FDD/TDD', Accepted for publication in IEEE PIMRC, 2003

[2] Veljanovski, R., Stojcevski, A., Singh, J., Faulkner, M., and Zayegh, A. 'A real-time reconfigurable architecture with advanced power management for UTRA-FDD', Accepted for publication in IEEE PIMRC, 2003

[3] Veljanovski, R., Stojcevski, A., Singh, J., Faulkner, M., and Zayegh, A. 'Implementation of a Reconfigurable Architecture', Accepted for publication in IEEE ICECS 2003

[4] Veljanovski, R., Stojcevski, A., Singh, J., Faulkner, M., and Zayegh, A. 'A Highly Efficient Reconfigurable Architecture for an UTRA-TDD Mobile Station Receiver', Proceedings of IEEE ISCAS, Thailand, Bangkok, pp. 45 -48, 2003

[5] Veljanovski, R., Singh, J., and Faulkner, M. 'A Proposed Reconfigurable filter for a Mobile Station Receiver', Proceedings of IEEE GLOBECOM, Taipei City, Taiwan, pp. 524 -528, 2002

[6] Veljanovski, R., Singh, J., and Faulkner, M. 'DSP and ASIC Implementation of A Channel Filter for A 3G UTRA-TDD System', Proceedings of IEEE PIMRC, Lisbon, Portugal, pp. 1447 -1451, 2002

[7] Veljanovski, R., Singh, J., and Faulkner, M. 'Fir Pulse Shape Filter for a 3G Wireless TDD Application', Proceedings of ISIC, Marina Mandarin, Singapore, 2001

Chapter 1

Thesis Overview

1.1 Introduction

Over the past 10 years, the development of digital communications has been colossal. Global Systems for Mobile Communications (GSM) is now the '*standard*' means of cellular communications in major regions of the world. Now wireless communications is evolving to third generation (3G), where many diverse protocol standards exist for various communication applications. 3G wireless communications is the next phase that offers wideband data services and multimedia wideband products and services such as video conferencing and high speed Internet over a mobile phone. It will also allow users to access multiple services simultaneously. Among the numerous wireless communication standards there is a need for flexible and adaptive systems. With the emergence of new standards, devices that can configure themselves to the new standard while consuming minimum power are in demand. Amid these high-tech feature packed mobile devices, there is a major bottleneck of cost. The major cost factor in mobile

devices is battery life. The more complex the devices hardware, the less the battery will last till it has to be charged, resulting in lower talk and standby times.

Time division duplex (TDD) is one of the duplex modes for wideband code division multiple access (WCDMA) also referred to as universal mobile telephone service (UMTS) terrestrial radio access (UTRA) that offers such services. The key driver and main objective of UTRA-TDD systems are high bit rate services up to 384 Kilo bits per second (Kbps) for high-mobility users and up to 2 Mega bits per second (Mbps) for low-mobility users. UTRA-TDD is spectrum efficient as it uses a single frequency band for both uplink and downlink. This is achieved using synchronised time intervals. The high bit rate services together with the lack of spectrum prompt the development of more spectrum efficient radio communication technologies.

1.2 Motivation for the Thesis

Adjacent channel interference (ACI) has become one of the most critical issues in UTRA-TDD as ACI is experienced from adjacent base stations and adjacent mobile stations dependent on frame synchronisation and channel asymmetry. One significant challenge for developers of 3G wireless systems is the design of digital filters for mobile terminal receivers. In order to transmit increasing quantities of information within a finite frequency bandwidth, tighter and more complex filter specifications often arise. For example, in order to attenuate ACI below a certain tolerance level, receiver channel filters with narrow pass bands and transition bands are mandatory. These

specifications characteristically require higher order filters, increased storage for filter coefficients and higher sampling rates. In some cases, such filter specifications are difficult to design and implementation cost becomes an issue. It is also desirable to have precise phase linearity in the pass band. Finite impulse response (FIR) digital filters achieve phase linearity but require high complexity to achieve a steep cut-off. Infinite impulse response (IIR) filters generally require a lower order to achieve similar specifications as FIR filters but at the cost of comprising the pass band with a non-linear phase response.

High-order and complex digital channel filters have a major impact on power consumption in a mobile phone. It is vital to minimise power consumption to extend the life of the battery. To achieve this goal, the design and implementation of the channel filter will have to employ a power efficient design methodology.

1.3 Research Aims

The objective of this research was to design and implement a *reconfigurable* digital root raised cosine (RRC) channel filter for an UTRA-TDD mobile receiver. Specific aims are as follows:

- *Investigate the effects of interference in the UTRA-TDD system.* As the channel filter mitigates ACI, a statistical analysis of ACI assisted in the design of the reconfigurable filter, as a better understanding of ACI was achieved. Inter-symbol interference (ISI) was examined with respect to the channel filter to investigate the effect of reducing the filter length.

- *Develop novel algorithms for reconfigurable channel filtering in UTRA-TDD.* The algorithm intelligently calculates the required filter order to mitigate ACI while meeting the specified signal-to-noise ratio (SNR).

- *Design and analysis of the reconfigurable channel filter.* The design of the novel components in the architecture as well as functional simulations verified the design. A statistical analysis of the filter was used to evaluate the performance whether good or poor.

- *Implementation of the reconfigurable channel filter.* The architecture was hardware/software partitioned using digital signal processor (DSP) and application specific integrated circuit (ASIC) technologies. A DSP possesses flexibility whereas the ASIC exhibits high computational speed and lower power consumption. The control unit of the architecture was partitioned on a DSP and the filter data path as an ASIC.

- *Performance analysis of the reconfigurable filter.* The implementation was analysed at synthesis stage where a performance analysis was carried out in terms of power consumption and speed.

- *Design and analysis of a reconfigurable pipelined architecture.* The architecture consists of a reconfigurable word length analog to digital converter (ADC) and the reconfigurable channel filter.

1.4 Originality of the Thesis

This research is focused on a high speed, low power *reconfigurable* digital channel filter for an UTRA-TDD mobile terminal receiver. The UTRA-TDD receiver block diagram is presented in Figure 1.1 where the reconfigurable filter and novel (shaded) components, full wave rectifiers (FWRs), running average filters and control unit are presented. The other receiver components are described in Chapter 2.

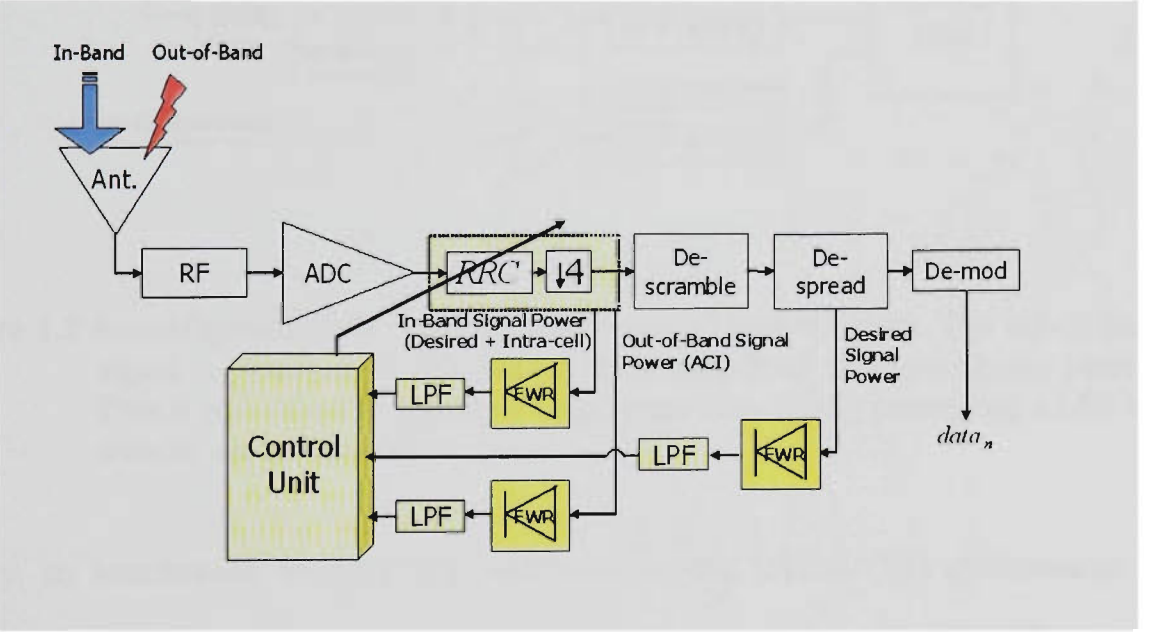


Figure 1.1 UTRA-TDD Receiver block diagram including novel reconfigurable components for the RRC channel filter

'*Reconfigurable*' can be defined as an intelligent functionality where a system can modify or scale its operating parameters to suit a change in operating conditions. The reconfigurable filter automatically monitors in-band and out-of-band signal powers and intelligently chooses the required filter order to meet the SNR, thus, yielding optimum power efficiency and extended battery life in the mobile terminal. Full wave rectifiers and running average filters obtain clearly varying amplitudes of the input signals to the

Control Unit. Full details of the reconfigurable filter architecture and operation are presented in Chapter 4. Although it is designed for UTRA-TDD, it can be modified through software for other wireless applications such as frequency division duplex (FDD) mode of UTRA. The system block diagram is presented in Figure 1.2.

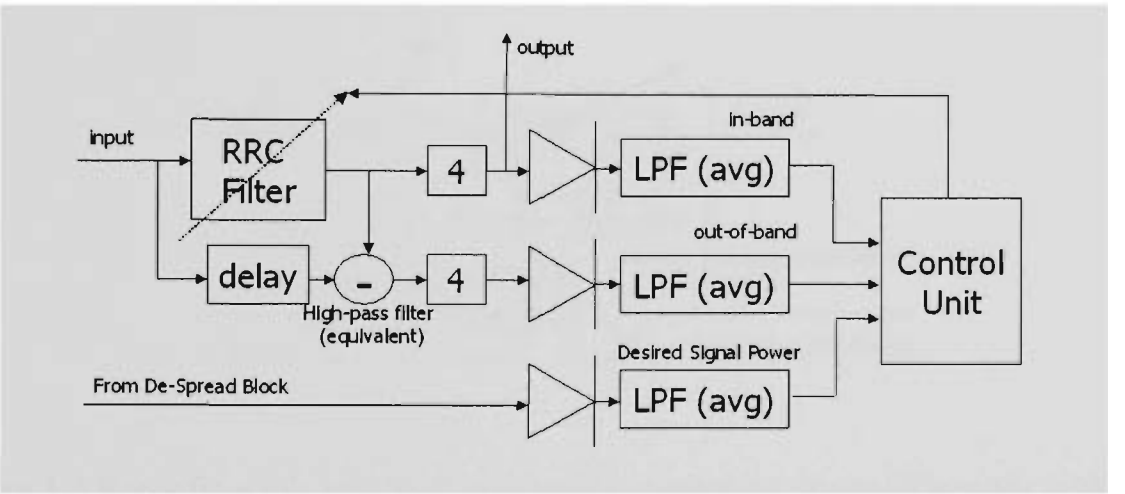


Figure 1.2 Reconfigurable RRC channel filter system block diagram. The out-of-band signal is obtained by subtracting the output from a delayed input sample. This is equivalent to a complex high-pass filter (HPF) presuming a LPF but without the complexity.

Firstly, an interference analysis was performed on the UTRA-TDD environment to evaluate and justify the necessity for such a reconfigurable filter. Based on the findings, the architectural design of the reconfigurable filter was proposed and statistical analysis in both static and dynamic UTRA-TDD simulation environments were carried out to evaluate the efficiency of the architecture. Implementation of the architecture and analysis was performed to reveal the power consumption efficiency. These findings have led to the design of a reconfigurable-pipelined architecture for an UTRA-TDD mobile terminal receiver consisting of a digital filter and a pipeline ADC. The same reconfigurable principle applies to the architecture where the length of the filter and word length of the ADC are scaled depending on in-band and out-of-band power ratios.

The idea is illustrated in Figure 1.3 where the architecture includes the same components as the reconfigurable filter with the inclusion of resolution scalability of the ADC. This architecture further reduces power consumption in the mobile, as the ADC is a key player in the receiver with high cost demands.

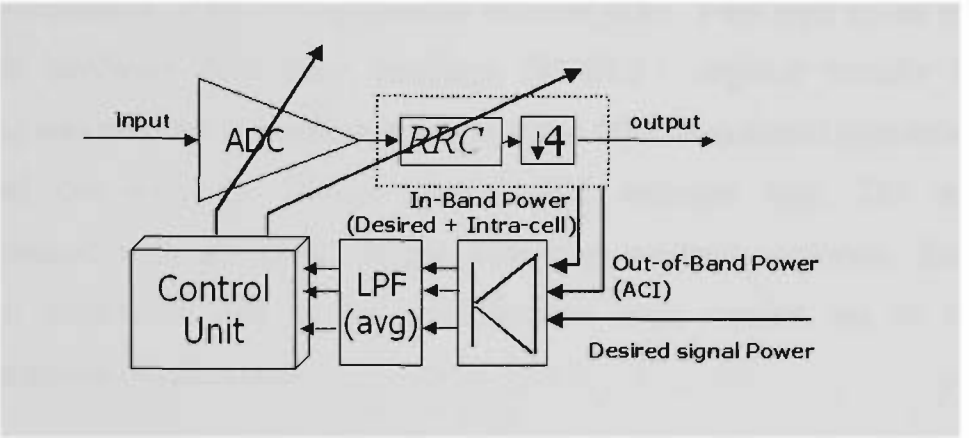


Figure 1.3 Reconfigurable pipelined architecture consisting of reconfigurable ADC and channel filter

1.5 Research Methodologies and Techniques

The research methodologies and techniques for this research are listed and detailed as follows:

- *Investigate the effects of interference the UTRA-TDD system.* The analysis was carried out using *MATLAB* simulation software. Monte Carlo simulations were used to obtain statistical analyses of ACI. An UTRA-TDD baseband transceiver was designed and simulated to investigate the effects of ISI.

- *Development of new low power algorithms for reconfigurable digital filtering.* The SNR was examined and manipulated and formed the basis of the reconfigurable algorithm for the control unit in the architecture. A control algorithm was developed to ensure outage is at a minimum by employing hysteresis protection.

- *Design and analysis of reconfigurable channel filter.* The filter architecture was designed and simulated using *MATLAB* simulation software to test for functionality. SNR analysis as well as statistical analysis was performed to evaluate its efficiency.

- *Implementation of the reconfigurable channel filter.* Very high speed integrated circuit hardware description language (VHDL) – register transfer language (RTL) was used for the implementation of the filter. Functional simulations were carried out with the *Summit Visual HDL* software tool. The code was synthesised with *Synopsys Design Compiler* synthesis software. Exhaustive circuit simulation and design modifications were carried out to meet the performance requirements.

- *Performance analysis of the reconfigurable filter.* The filter was analysed at synthesis stage where performance was measured using the features available in *Synopsys Design Compiler*. The performance analysis included timing and power dissipation.

- *Design and analysis of a reconfigurable pipelined architecture.* The reconfigurable pipelined architecture was designed and analysed in a static simulation environment using *MATLAB* simulation software. Monte Carlo simulations were used to obtain statistical analysis of ADC word lengths and filter lengths.

1.6 Organisation of the Thesis

This thesis is structured with seven chapters. Subsequent to the introduction, Chapter 2 describes the most relevant literature reviewed in order to present an understanding of the research topic with a focus on cost implications on filter design for UTRA-TDD. It concludes with a cost effective solution to the defined problem. Chapter 3 presents an

interference analysis of the UTRA-TDD system in an indoor office environment. ACI is investigated as well as ISI with respect to the channel filter. The investigation provides a solid foundation for the design of the reconfigurable channel filter.

The architectural design and specifications of the reconfigurable filter are presented in Chapter 4. Analysis of the filter in both static and dynamic simulation environments is presented in Chapter 5. This chapter also provides implementation considerations and a description of the hardware design and implementation of the reconfigurable filter. A performance analysis with respect to timing and power consumption is also presented. The design of the combined reconfigurable-pipelined architecture consisting of the filter and ADC is described in Chapter 6. A statistical analysis is presented to evaluate its efficiency. Chapter 7 concludes the thesis summarising the major findings as well as proposing extended future research options.

Chapter 2

Literature Review

2.1 Introduction

In the System-on-a-Chip (SoC) domain, digital signal processor (DSP) architectures are required as they can be reprogrammed and adapted towards system needs. As system requirements change, there is a need for flexible systems. This is the situation in the wireless communications world. DSP implementations also have a faster time to market [1, 2] compared to application specific integrated circuits (ASICs), since they are software driven. ASICs dissipate less power while exhibiting high performance, but lack adaptation [3, 4]. Therefore, if the application or standard changes, so does the hardware. DSPs can adapt to new applications or standards by reprogramming the device. The predicament with DSPs is elevated power consumption if high performance is required [5, 6].

To meet the high-speed low-cost requirement of wireless handheld devices, such a device needs to possess the flexibility and configurability of a DSP processor and

computational speed and power efficiency of an ASIC. In some cases, this can be achieved using both DSP core and ASIC architectures and incorporating advanced power management [7]. Next-generation programmable DSP cores [8, 9] form the basis for an ASIC on a single chip. The flexibility can be achieved by implementing functions with very high processing demand as an ASIC that can be run-time configured to support a wide range of structures. The DSP can maximise the number of functions performed. This combination offers lower gate count; smaller die area and lower power dissipation.

Based on the above needs, this chapter describes the most relevant literature reviewed in order to present an understanding of the research topic. Wideband code division multiple access (WCDMA) is the application for the receiver channel filter. WCDMA is firstly studied with emphasis on the time division duplex (TDD) operation mode. The advantages and disadvantages are studied and particular interest is paid to the disadvantages where cost implementation issues are discussed. Cost optimisation is analysed for the filter and a novel solution is described.

The literature review is organised into five subsections. The evolution of wireless telecommunications is described in section 2.2 and section 2.3 introduces WCDMA, with focus on the TDD mode. Cost implications of the filter are presented in section 2.4 and conclusions to this chapter are presented in section 2.5.

2.2 The Road to 3G Wireless Communications

The evolution towards third generation (3G) cellular systems is illustrated in Figure 2.1 [10]. Analog frequency modulation (FM) was the backbone of first generation (1G) cellular wireless communication systems. The advanced mobile phone system (AMPS) developed by Bell Telephone Systems, was the foremost common means of wireless communications during the 1G era. It employs FM technology for voice transmission as well as digital signalling for control information [11]. Other 1G systems include [11]:

- Narrowband AMPS (NAMPS)
- Nordic Mobile Telephone System (NMT-900), and
- Total Access Cellular System (TACS)

Frequency division multiple access (FDMA) was the scheme used in 1G, which in effect assigned each channel to a unique frequency band within a cluster of cells. The rapid growth in subscribers and the abundance of countless incompatible 1G devices yielded the evolution towards 2G cellular systems. 2G systems employ coding techniques and compression where digital modulation schemes are used, thus, 2G was the beginning of the digital era of civilian wireless communications [11].

Multiple access techniques like time division multiple access (TDMA) and code division multiple access (CDMA) are used along with FDMA in the 2G systems. 2G cellular systems include [11]:

- United States Digital Cellular (USDC) standards IS-54 and IS-136

- Global System for Mobile communications (GSM)
- Pacific Digital Cellular (PDC)
- CdmaOne

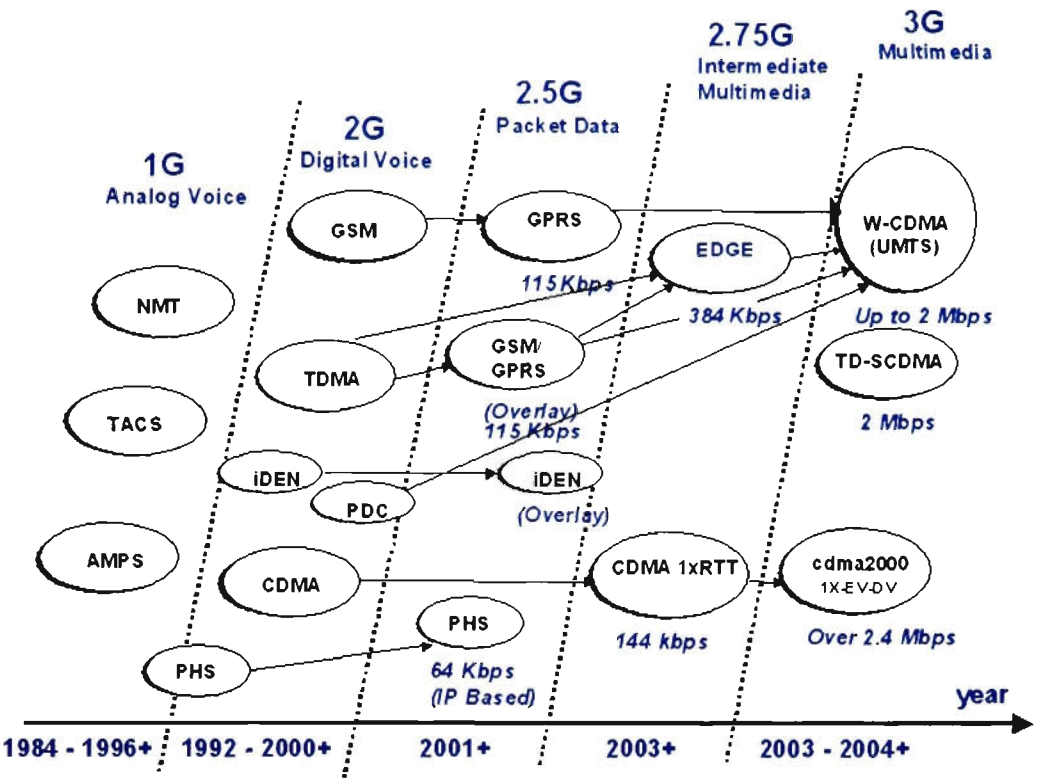


Figure 2.1 The evolution to 3G wireless communications [10]

3G wireless communications is well under way where the key objective is to support wideband services like high speed Internet, video and high quality image transmission. The primary requirements for next generation wireless systems are listed in [11, 12] and are outlined as follows:

- Voice quality comparable to Public Switched Telephone Network (PSTN).
- Support of high data rate.
- Support of both packet-switched and circuit-switched data services.
- More efficient usage of the available radio spectrum

- Support of a wide variety of mobile equipment
- Backward Compatibility with pre-existing networks and flexible introduction of new services and technology
- An adaptive radio interface suited to the highly asymmetric nature of most Internet communications: a much greater bandwidth for the downlink than the uplink.

2.3 Wideband Code Division Multiple Access

The WCDMA air interface, also referred to as universal mobile telephone service (UMTS) terrestrial radio access (UTRA) was developed by the 3rd generation partnership project (3GPP). WCDMA is characterised by two duplex modes: frequency division duplex (FDD) and TDD [13]. Figure 2.2 [14, 15] illustrates the distinction between the two duplex modes where the shaded arrows represent uplink and the non-shaded arrows represent downlink transmission to and from base and mobile station.

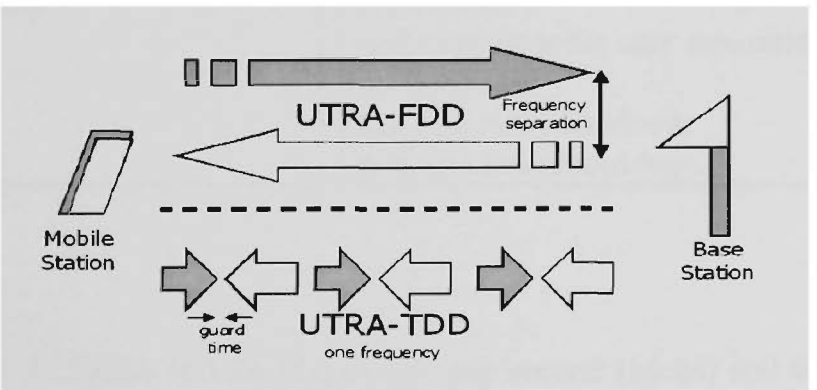


Figure 2.2 UTRA duplex modes [14, 15]

In UTRA-FDD, the uplink and downlink transmissions use paired radio frequency bands whereas in UTRA-TDD, uplink and downlink transmissions are carried over the same radio frequency using synchronised time intervals. Time slots in the physical

channel are divided into transmission and reception part [16 - 18]. Information on uplink and downlink are transmitted reciprocally [19]. Table 2.1 [20] lists the parameters of WCDMA.

Table 2.1 WCDMA parameters [20]

Parameter	*Value*
Channel Bandwidth	5 MHz
Duplex Mode	FDD / TDD
Downlink RF Channel Structure	Direct spread
Chip Rate	3.84 Mcps
Frame Length	10 ms
Spreading Modulation	Balanced QPSK (downlink) Dual-channel QPSK (uplink)
Data Modulation	QPSK (downlink) Binary Phase Shift Keying (BPSK) (uplink)
Coherent Detection	User dedicated time multiplexed pilot
Downlink Channel Multiplexing	Time multiplexed data and control channels
Uplink Channel Multiplexing	Control and pilot channel time multiplexed I&Q multiplexing for data and control channel
Channel Coding	Turbo and convolution codes
Multirate	Variable spreading and multicode
Spreading Factor Length	Uplink: 4-256, Downlink: 4-512
Downlink Spreading	OVSF for channel separation Gold sequences for cell/user separation
Uplink Spreading	OVSF codes Gold sequences for user separation
Handover	Soft handover Inter-frequency handover
Power Control	Open and fast closed loop

The chip rate of WCDMA is 3.84 Mega chips per second (Mcps) and the frame length is 10 milliseconds (ms). Each frame consists of 15 time slots (2560 chips/slot). Spreading factors range from 4 to 256 and 4 to 512 in the uplink and downlink respectively for FDD [20]. Orthogonal variable spreading factor (OVSF) channelisation codes are used for separating channels from the same source for TDD. In the uplink and

downlink, Gold codes with a 10 ms period are used to separate difference cells. Convolutional coding, turbo coding, or no channel coding is supported. Bit interleaving randomises transmission errors [20]. The carrier spacing has a raster of 200 Kilohertz (kHz) and varies from 4.2 Megahertz (MHz) – 5.4 MHz. Depending on interference, various carrier spacing can be used to obtain the most efficient adjacent channel protection [20]. This is illustrated in Figure 2.3 [20]. The figure shows an example of 20 MHz bandwidth allocated for the operator with 4 cell layers (or simply cells) which illustrates the carrier spacing and raster.

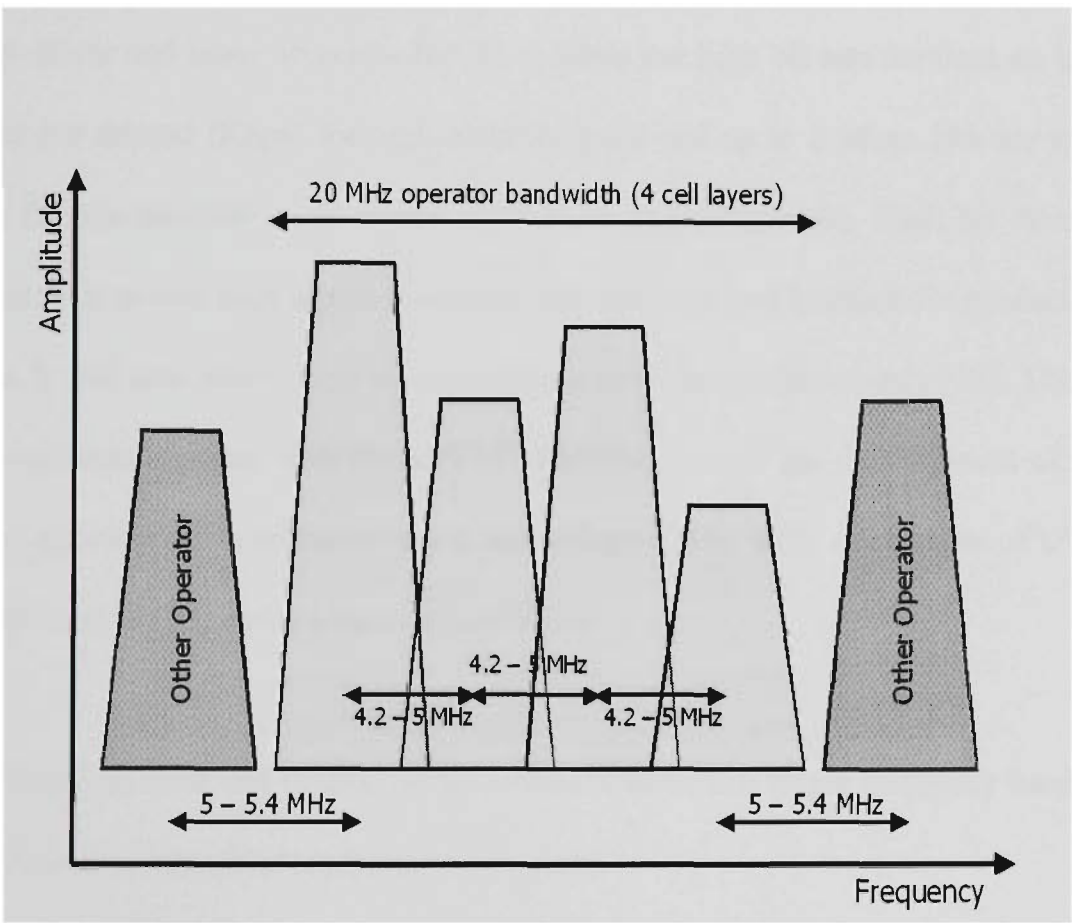


Figure 2.3 Operator bandwidth allocation in WCDMA [20]

From this point forward, the thesis focuses on TDD as these systems will be of major importance in the future. Nevertheless, FDD is relevant to the 'big picture' as TDD is its complement by providing high density local area access. This is a consequence of the

requirement for co-ordination of FDD and TDD network planning due to the particular UMTS frequency allocations. As a consequence of poor network planning, both FDD and TDD are susceptible from interference from one another and this issue could be investigated further in future with relation to the reconfigurable filter documented in this thesis.

2.3.1 UTRA-TDD

The key driver and main objective for 3G systems are high bit rate services up to 384 Kilo bits per second (Kbps) for high-mobility users and up to 2 Mega bits per second (Mbps) for low-mobility users (mainly for indoor environments). High bit rates will allow users to access high-speed wideband data services and multimedia products and services. It will also allow users to use multiple services simultaneously [21]. The high bit rate services together with the lack of spectrum prompt the development of more spectrum efficient radio communication technologies. The main advantages of UTRA-TDD are listed in [20] and are summarised below:

- Unpaired band and bi-directional communication in a single frequency band.
- Adaptive support of asymmetric data rates.
- High speed data services for indoor or low-mobility operating environments.
- Large channel capacity (equivalent to FDD mode).
- Small sized mobile terminal.
- Precise and efficient open loop power control.
- Low complexity transceivers.

TDMA is the key feature in UTRA-TDD, which these advantages result from. The key advantage of UTRA-TDD is the ability to use unpaired frequency bands, which in effect, solves some frequency band allocation issues resulting in effective and efficient use of the spectrum [20, 21]. Services such as mobile Internet, multimedia applications and file transfers may have different capacity requirements for uplink and downlink transmission. UTRA-TDD offers the advantages of flexibility in resource allocation, as the frequency band is not fixed between uplink and downlink (unlike FDD) [20, 21].

2.3.1.1 Physical Channel Structure

An UTRA-TDD physical channel is defined by frequency, timeslot, channelisation code, burst type and radio frame allocation. Figure 2.4 [22] illustrates the physical channel signal format.

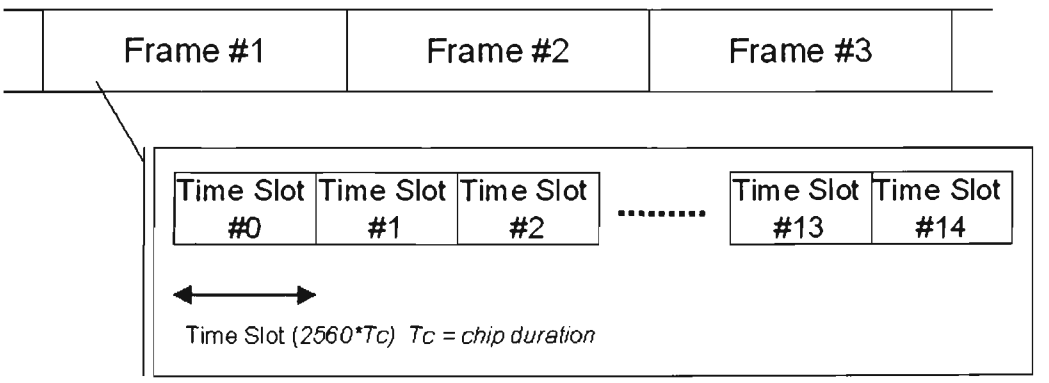


Figure 2.4 UTRA-TDD signal structure [22]

Each frame has a duration of 10 ms, which contains fifteen time slots. A time slot corresponds to 2560 chips. Time slots can be allocated to either uplink or downlink, which therefore can support asymmetric services. Depending on resource allocation, the configuration of radio frames and/or time slots could differ. Guard symbols are used to

separate different user signals in the time and code domain. The physical contents of the time slots are bursts of data with a length corresponding to the data rate. Figure 2.5 [22] illustrates a TDD burst where GP is the guard prefix.

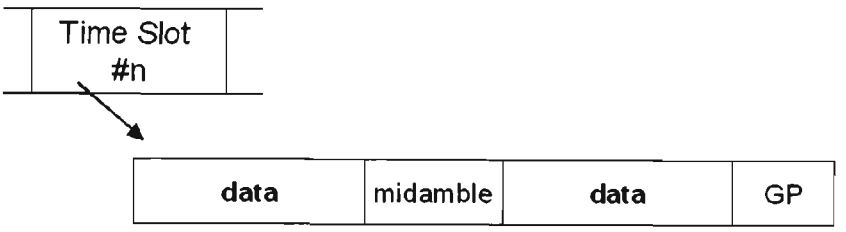


Figure 2.5 Example of an UTRA-TDD burst structure [22]

As each 10 ms frame consists of 15 time slots, each allocated to either the uplink or the downlink, the TDD mode can be adapted to different environments and deployment scenarios [22]. Examples for multiple and single switching point configurations as well as for symmetric and asymmetric uplink and downlink allocations are presented in Figure 2.6 [22] where the arrows pointing upwards indicate uplink allocation and arrows pointing downwards indicate downlink allocation.

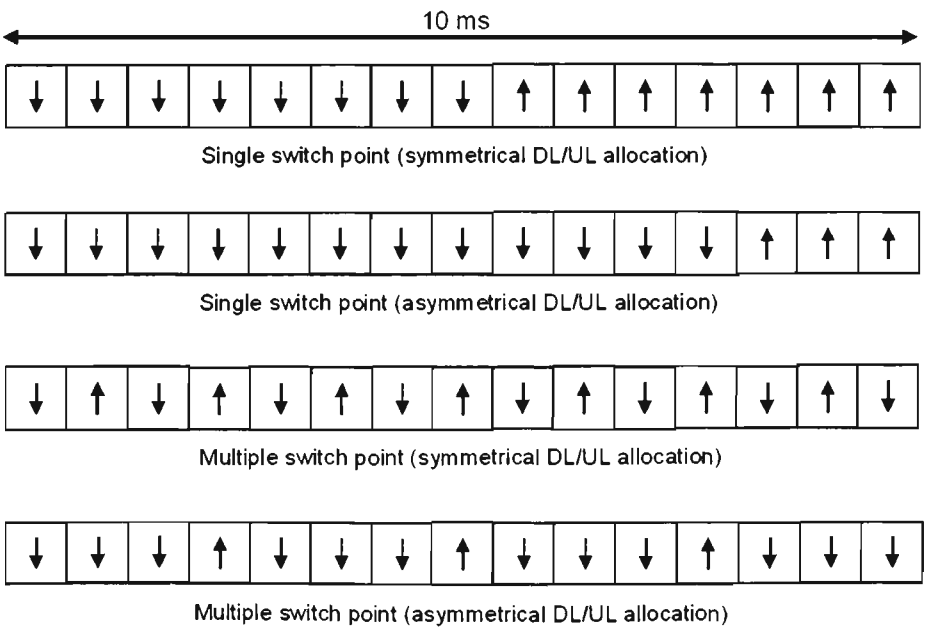


Figure 2.6 TDD frame structure examples (UL = uplink, DL = downlink) [22]

2.3.1.2 Transmitter Architecture

A specification for an UTRA-TDD transmitter has been released by 3GPP and is presented in Figure 2.7 [23]. The diagram presents the modulation for sixteen users of one of the fifteen time slots per TDD frame [24, 25]. The first block in the transmission chain is data mapping. The data mapping of raw bits is performed using Quadrature Phase Shift Key (QPSK), where two consecutive binary bits are combined and converted to a complex valued data symbol.

As an example, consider the data source [00 10 11 01], the corresponding complex data symbols after QPSK mapping are [+j −1 −j +1]. See Annex A for full details on spreading and modulation by 3GPP.

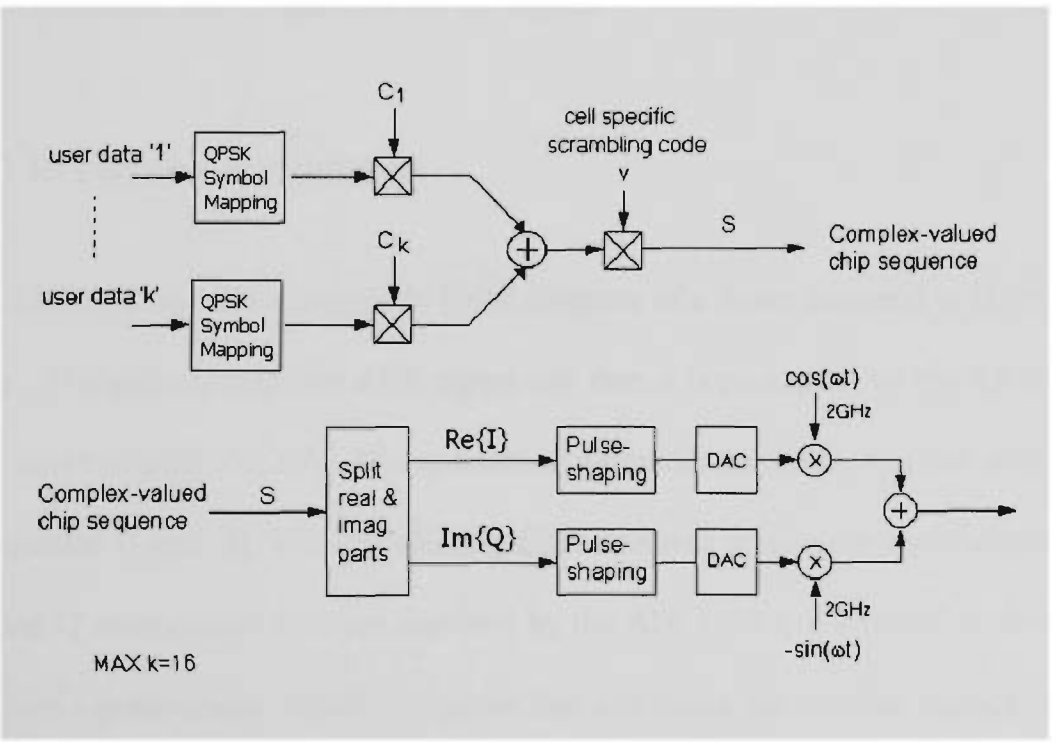


Figure 2.7 UTRA-TDD Baseband Transmitter (one time slot) [23]

The complex valued data symbols are spread by two operations. Firstly, the symbols are spread with real valued channelisation codes *Ck*. The channelisation codes are OVSF codes, allowing mixing for the same time slot with different spreading factors while preserving orthogonality. The resulting sequence is scrambled by a complex cell specific scrambling code *v*. The complex-valued chip sequence is split into in-phase (I) and quadrature (Q) components. The signals are next pulse-shaped by two low pass pulse-shaping filters. Details and specifications of the pulse-shaping filters are presented in Chapters 3 and 4 subsections 3.3 and 4.2 respectively.

Two digital-to-analog converters (DACs) convert the digital signals to analog. The signals are then quadrature modulated to represent the signal in radio frequency (RF) format at a 2 Gigahertz (GHz) carrier frequency. All information is contained in the complex envelope and the phase of the RF signal.

2.3.1.3 Receiver Architecture

Figure 2.8 [23] illustrates the generic block diagram of a direct conversion UTRA-TDD receiver. The antenna receives a RF signal and then it is processed by the RF filter and the low noise amplifier (LNA). The quadrature demodulator produces a complex valued chip sequence (I and Q). The anti-aliasing filter removes aliasing in the spectrum from both I and Q components then are digitised by the ADCs. The root raised cosine (RRC) filters have a pulse-shape impulse response that attenuates out-of-band signals from the I and Q components before the in-band signal is brought to other baseband signal processing blocks. If the out-of-band signals were not filtered, the end user of the mobile phone will experience interference noise.

These filters dissipate major power in the transmission chain [26]; therefore reducing the complexity is vital. Once filtering is completed, the signals are de-scrambled with a cell specific scrambling code *Vn*, de-spread with channelisation code *Ck* and finally de-modulated (de-mapped) to obtain the users' raw data bits.

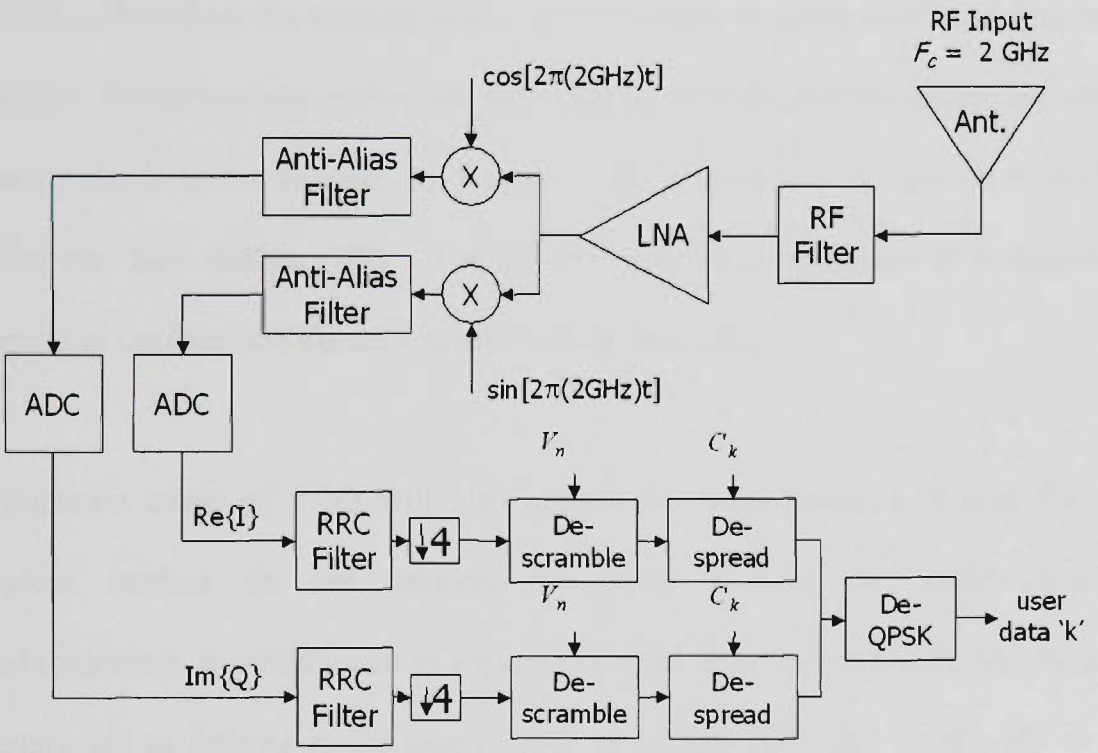


Figure 2.8 UTRA-TDD Receiver architecture for one time slot [23]

2.3.1.4 Interference Issues

Interference has become one of the most critical issues in WCDMA [27, 28]. The signal to interference ratio (SIR) can be low at carrier bandwidth as the processing gain improves the SIR after despreading. In UTRA-TDD, a transmitter located near a receiver may jam the front end of the receiver as no RF filter can be used to separate

uplink and downlink. This can occur if the transmitter and receiver are operating in the same band allocation but on different frequency channels [20].

To avoid interference between uplink and downlink, all users must be synchronised and have the same time division between uplink and downlink within one cell. This time division is based on the average uplink and downlink capacity needed in that cell [20]. Multirate techniques are applied for each user so they adapt to its uplink and downlink capacity needs to the average need in that cell. It must also be applied to all carriers within one base station (BS). The BS can jam its own signals if it transmits and receives at the identical instance as adjacent carriers [20].

Asymmetric usage of TDD will also impact the radio resource in near by cells. If adjacent carriers do not employ the same channel asymmetry and frame synchronisation, it would result in adjacent channel interference (ACI). The interference overlaps are as follows in the case of ACI in UTRA-TDD: BS → BS, BS → mobile station (MS), MS → MS and MS → BS [29]. This is the case if there are several operators providing service in the same geographical locality. Asymmetrical services are consequently not suitable if several operators share the same spectrum [20].

2.4 Cost Implications

WCDMA will eventually lead to further enhanced communications and feature packed mobile devices where the main focus will be video streaming and Internet, not voice communication alone. Amid these high-tech feature packed mobile devices, a major

bottleneck of cost will exist. The major cost factor in mobile devices is battery life. The more complex the devices hardware, the less time the battery will last till it has to be charged, resulting in lower talk and standby times.

2.4.1 Filter Implications

Mobile terminals have limited dynamic range and limited adjacent channel filtering capability; therefore ACI could be quite severe and is recognised as one of the major issues. This leads to really complex filter designs and implementations to eliminate ACI, but is costly on the battery life of the terminal. To attenuate the ACI at the worst case, i.e., a mobile terminal of particular interest is receiving and is situated near by adjacent carriers that are being transmitted; the filter will need to be complex to achieve the target signal-to-noise ratio (SNR). If the ACI is minor and only a fraction of full filtering power is needed, the filter will still operate at full power as it has a fixed length or complexity. This will dissipate unnecessary power resulting in shorter battery life, which is one of the biggest dilemmas for the mobile terminal [30].

An optimal receiver filter is matched to the transmitter pulse-shaping filter. This will provide maximum SNR. The receiver filter poses many problems in terms of complexity, as it requires a higher input dynamic range compared to the transmitter filter and it also desirable to have precise phase linearity in the pass band. Finite impulse response (FIR) digital filters achieve phase linearity, as the coefficients are symmetrical but it is also possible to employ an infinite impulse response (IIR) wave digital filter with almost linear phase characteristics. The only disadvantage is to achieve high roll-off sharpness; the filters` requirements will need to be of higher order. The multipliers

dominate the power consumption of digital FIR filters. For every coefficient, a multiplication operation is required are used and is costly on hardware [31]. This is subject to multiple-constant techniques that cause the cost of a multiplier to asymptotically approach one addition for large numbers of multiplications. The total power consumption of an FIR filter (based on a direct form structure), P_{FIR}, can be estimated as follows:

$$P_{FIR} = \left(P_{mac} + P_{reg}\right)n \tag{2.1}$$

where P_{mac} is the power consumption of a multiplication and addition (multiply-accumulate) unit, n is the filter length and P_{reg} is the power consumption of registers for coefficient and input sample storage. Power consumption is also proportional to the sampling frequency of the filter in complementary metal oxide semiconductor (CMOS) implementation. Lowering the supply voltage, V_{dd}, will also reduce the power consumption, as it also is the key factor in dynamic power consumption. This will also degrade system performance but can be compensated by parallelism and pipelining. A suitable supply voltage should be chosen to ensure that performance requirements are satisfied. Power consumption in a CMOS integrated circuit is dominated by the switching or dynamic power where the model, P_{cmos}, is a summation of static and dynamic power consumption given by [32, 33]:

$$P_{cmos} = \overbrace{\left(\sum I_{dd} \bullet V_{dd}\right)}^{StaticPower} + \overbrace{\left(\underbrace{\left[C_p f_i b_s\right]}_{TransientPower} + \underbrace{\left[C_l f_o O_s\right]}_{\substack{Capacitive-load \\ Power}}\right) V_{dd} V_{swing}}^{DynamicPower} \tag{2.2}$$

where V_{dd} is the supply voltage, V_{swing} is the voltage swing, I_{dd} is leakage current, C_p is dynamic power-dissipation capacitance, f_i is the input signal frequency, b_s is the number

of bits switching, C_l is external load capacitance, f_o is the output signal frequency, and O_s is the total number of outputs switching.

2.4.2 FIR Filter Optimisation Techniques

Digital FIR filters can be implemented using various architectures. The direct form or otherwise known as the transversal structure is the most common implementation architecture and is depicted in Figure 2.9 [34]. The input, *x(n)* and the output *y(n)* of the filter structure are related by:

$$y(n) = \sum_{m=0}^{M} b_m x(n-m) \tag{2.3}$$

z^{-1} represents a delay unit of one sample or unit of time, thus, *x(n-1)* is *x(n)* delayed by one sample. The output sample is a weighted sum of the present input and *M* previous samples of the input.

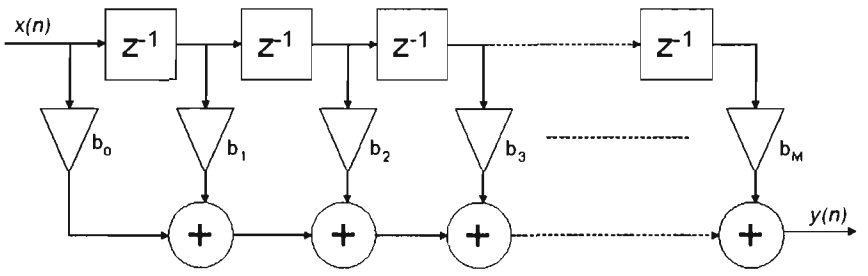


Figure 2.9 Transversal FIR filter structure [34]

The computation of each output sample requires the following hardware [34]:

- *M* memory locations to store the input samples
- *M+1* memory locations to store the coefficients

- M multiplication operations
- M addition operations

A linear phase structure is a variation of the transversal structure, which takes advantage of symmetrical coefficients and in effect, uses half the required multiplications and additions [34]. For odd and even phase filters, the transfer function, *H(z)*, can be written as [34]:

$$H(z) = \sum_{m=0}^{M/2-1} b_m \left[z^{-m} + z^{-(M-m)} \right] + b\left(\frac{M}{2}\right) z^{-(m/2)} \qquad M \text{ odd} \quad (2.3)$$

$$H(z) = \sum_{m=0}^{(M+1)/2-1} b_m \left[z^{-m} + z^{-(M-m)} \right] \qquad M \text{ even} \quad (2.4)$$

The corresponding difference equations, *y(n),* are as follows [34]:

$$y(n) = \sum_{k=0}^{M/2-1} b_m \{x(m-k) + x[m-(M-k)]\} + b[(M)/2]x[m-(M/2)] \quad M \text{ odd} \quad (2.5)$$

$$y(n) = \sum_{k=0}^{M/2-1} b_m \{x(m-k) + x[m-(M-k)]\} \qquad M \text{ even} \quad (2.6)$$

Figure 2.10 [34] illustrates the linear phase structure where seven coefficients are used. Numerous optimisation techniques exist for reducing power dissipation in complex digital FIR filter implementations for telecommunications equipment [35 - 43]. Implementation architectures can take advantage of the residue number system (RSN), which allows the decomposition of a given dynamic range in slices of smaller range on which the computation can be efficiently implemented in parallel [44 - 46]. This scheme

provides lower power consumption compared to traditional standard FIR filter structures for high order complex filters.

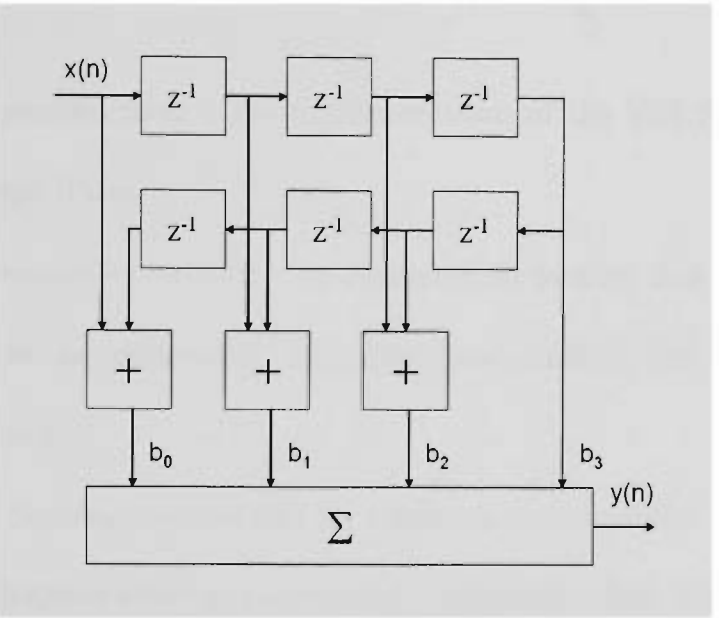


Figure 2.10 Linear Phase FIR filter structure [34]

Other filter architectures are adaptive which use the least mean square method (LMS) [47, 48] to adjust the filter coefficients to obtain better performance. Pipeline architectures for digital FIR filters achieve speed enhancements and lower power consumption combined with supply voltage downscaling [49]. An efficient filter design method for the design of a relatively complex low pass receiver filter for the CDMA standard as in [50, 51] employs the canonical digit representation of signed numbers to reduce the complexity of multiplication operations by reducing the number of 1's in the multiplicands. This in effect reduces the number of additions required for one multiplication.

A coefficient segmentation algorithm [52] can be applied to each filter coefficient. This algorithm splits each coefficient into two sections, *s1* and *s2*. When the filter is realised,

s1 is just a shift operation while *s2* is a reduced word-length low power multiplication. Other techniques to reduce power consumption in filters are summarised below [53]:

- *Multi-rate architectures* - the implementation of the FIR filter is in terms of decimated sub filters.
- *Multiple-constant techniques* – an optimisation method that cause the cost of a multiplier to asymptotically approach one addition for large numbers of multiplications.
- *Coefficient Scaling* - introduces an optimum scaling factor such that the total Hamming distance between consecutive coefficient values is minimised.
- *Coefficient Optimisation* - is an iteration algorithm where one or a pair of coefficients is optimised to reduce the Hamming distance between successive coefficients while preserving filter characteristics.
- *Selective Coefficient Negation* - reduces the number of "1s" (1s or 2s complement representation) in the coefficient input to the multiplier. This technique also reduces the Hamming distance between consecutive coefficients.
- *Coefficient Reordering* – looks at the order of coefficients stored, as the output is independent of the order.
- *Adder Bit Swapping* - uses the bit-wise commutativity property to reduce the number of toggles in the buses that feed the inputs to the adder.
- *Bus Bit Reordering* - looks at reducing the power dissipated in the coefficient memory data bus. As embedded SoC products typically are built with a DSP core with an ASIC back plane, the designer has control over the placement of various memories.

These filter optimisation techniques reduce power consumption but do not reduce it to the maximum possible limit for an UTRA-TDD MS receiver as the complexity of the filter is fixed. Therefore, full power is always used even when it is not required.

2.5 Conclusions

There are distinct advantages of using UTRA-TDD. Primarily, it offers a high degree of flexibility due to the reciprocity of the channel and channel asymmetry. The main disadvantage of UTRA-TDD is that additional interference sources exist compared to UTRA-FDD. Namely, MS→MS ACI exists if the network is not synchronised nor have non-identical channel asymmetries (variations of the channel) with neighbouring cells. This leads to a more complex receiver filter design and implementation, which will have a significant impact on battery life in the mobile terminal.

Filter optimisation techniques could lower power consumption but will not reduce it to its most efficient level. A solution in theory could be to use the minimum amount of filtering complexity required and still satisfy the performance requirements of the UTRA-TDD receiver specified by the 3GPP. To achieve this, in-band and out-of-band signal powers need to be measured. Then the filter intelligently calculates the amount of complexity (filter taps) required to ensure the out-of-band signal is below a certain tolerance level and the SNR is met. This scheme will reduce power consumption, as it only utilises the required filter complexity as compared to traditional fixed complexity architectures.

To convert theory into reality, the solution has to take advantage of the software defined radio concept and technologies [54]. An exact definition for a software radio does not yet exist, but there are many definitions to help gain an understanding. Some are as follows [55, 56]:

- Flexible transceiver architecture, controlled and programmed by software
- Signal processing able to replace, as much as possible, radio functionalities
- Radio equipment dynamically reconfigurable by downloadable software at every level of the protocol stack
- Software realisation of terminals to exhibit multiple modes and standards

The presence of the software defining the radio interface implies the use of DSPs to replace some or all dedicated hardware, to execute, in real time, the necessary software. Software radio is an emerging technology, which can build flexible radio system, multi-user, multi-standard that is reconfigurable and re-programmable by software. Another advantage of software radio is that it increases hardware lifetime reducing obsolescence risks. System re-programmability allows hardware reuse until a new generation of hardware platforms is available [57, 58].

Taking advantage of the software radio theory, a solution can be achieved using DSP and ASIC technologies that can meet the performance and system needs of high speed and low cost devices. A DSP can interface with an ASIC and control the filter complexity dependent on in-band and out-of-band power ratios. This could be embedded on a single chip to provide a SoC solution [59, 60].

Chapter 3

Adjacent Channel and Inter Symbol Interference Investigation

3.1 Introduction

The general aim of this work was to develop a reconfigurable digital receiver channel filter, which is power consumption efficient for the mobile terminal, and will enable system operators to use the universal mobile telephone service (UMTS) terrestrial radio access (UTRA) – time division duplex (TDD) cellular system efficiently. Interference is a major concern in any cellular system in terms of adjacent channel interference (ACI) and inter-symbol interference (ISI). ACI is a greater concern in TDD due to the additional interference sources. It is necessary to investigate interference in the downlink mode of TDD to gain an understanding of how it affects the system before the reconfigurable filter is designed.

The interference strength is dependent on transmission powers of the sources of interference, frame synchronisation and asymmetry, as well as location of the base

stations (BS's) or mobile stations (MS's), therefore, creating complicated interference situations. Many remedies exist to minimise interference issues and have been studied in [61 - 65]. Related work in [61] has proposed various solutions to minimise interference and are summarised as follows:

- Dynamic channel allocation techniques [66 - 69]
- Frame level synchronisation of TDD base stations within an operator's network and with different TDD operators if the base stations are located in the same geographical region
- TDD and frequency division duplex (FDD) co-placement should be minimised as well as the network should be planned carefully
- Handover techniques can minimise the severity of interference signal powers

The focus of this chapter is on downlink ACI in the UTRA-TDD system. An investigation into co-channel interference (CCI) is not provided as works related in [61-72] have addressed the issues. An investigation of ISI is also presented, as it is an important issue relating to the receiver channel filter. Scaling the filter length can cause great concern if the length is scaled down, as the required quality of service (QoS) may not be met.

Section 3.2 studies ACI for an UTRA-TDD environment. Interference models, synchronisation and frame asymmetry is discussed. Statistical analysis of ACI is performed for a single cell and multiple cells environment to justify the necessity for a reconfigurable channel filter. ISI is studied in section 3.3 where it is first defined then

an analysis is given with respect to the channel filter. Conclusions are presented in section 3.4.

3.2 Adjacent Channel Interference

ACI is investigated in this section and how certain dynamics affect the strength of the interference power. Section 3.2.1 defines ACI in an UTRA-TDD system. The investigation in section 3.2.2 first considers a single interfering cell scenario then it is expanded to a multiple interfering cell scenario consisting of a cluster of seven interfering cells. This platform is considered the *'worst case'* interference scenario for TDD assuming an indoor operating environment.

A statistical analysis in a simulation environment of both single cell and multiple cells interference scenarios are presented in section 3.2.2 where particular interest is paid to the effect of various frame synchronisation and channel asymmetry.

3.2.1 Classification of ACI in UTRA-TDD

In a fully flexible system, cellular operators may independently plan their network structure without the consideration of other cellular operators. Therefore, there is a good probability that cells between independent operators can overlap and create complicated ACI scenarios as transmitting and receiving users can be in close proximity. Adjacent channel protection (ACP) factors combat the interference a user experiences but is a great concern as ACI can be quite severe in UTRA-TDD. Figure 3.1 [64] depicts such a

scenario where two operators have their cells overlapped creating uplink and downlink ACI situations.

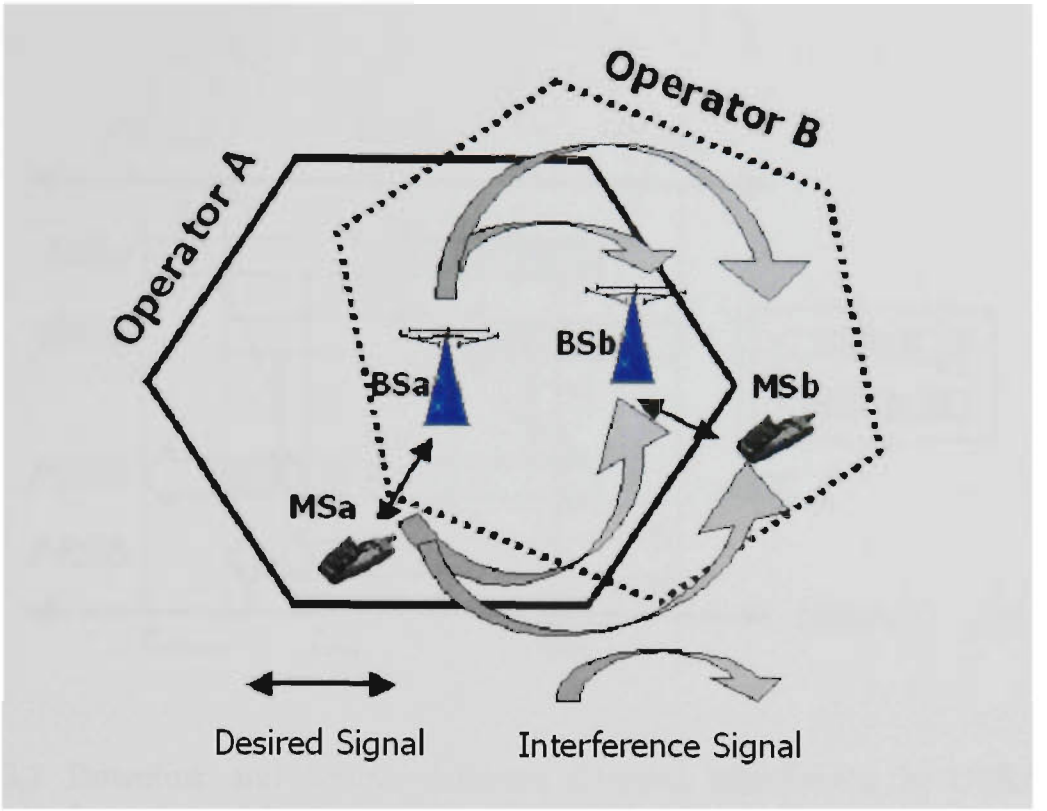


Figure 3.1 Two independent operators on adjacent carriers creating complicated ACI issues in the uplink and downlink of UTRA-TDD as their cells overlap [64]

As TDD divides time on one frequency, the possible interference links for uplink operation are: MS → MS and MS → BS, and for downlink operation are: BS → BS and BS → MS. If independent operators employ identical channel asymmetry and frame synchronisation, it would eliminate the cases of MS → MS and BS → BS interference leaving the equivalent interference overlaps as FDD mode. Frame synchronisation and identical channel asymmetry cannot be assumed in practical and a fully flexible UTRA-TDD system; therefore, there are greater interference issues as compared to FDD. This is illustrated in Figure 3.2 [71]. This figure illustrates a timing analysis of two independent operators where the vertical arrows represent interference links and the horizontal blocked arrows represent uplink and downlink. The shaded segments of the

blocked uplink/downlink arrows indicate that the segment is susceptible to interference from the source indicated by the vertical arrows.

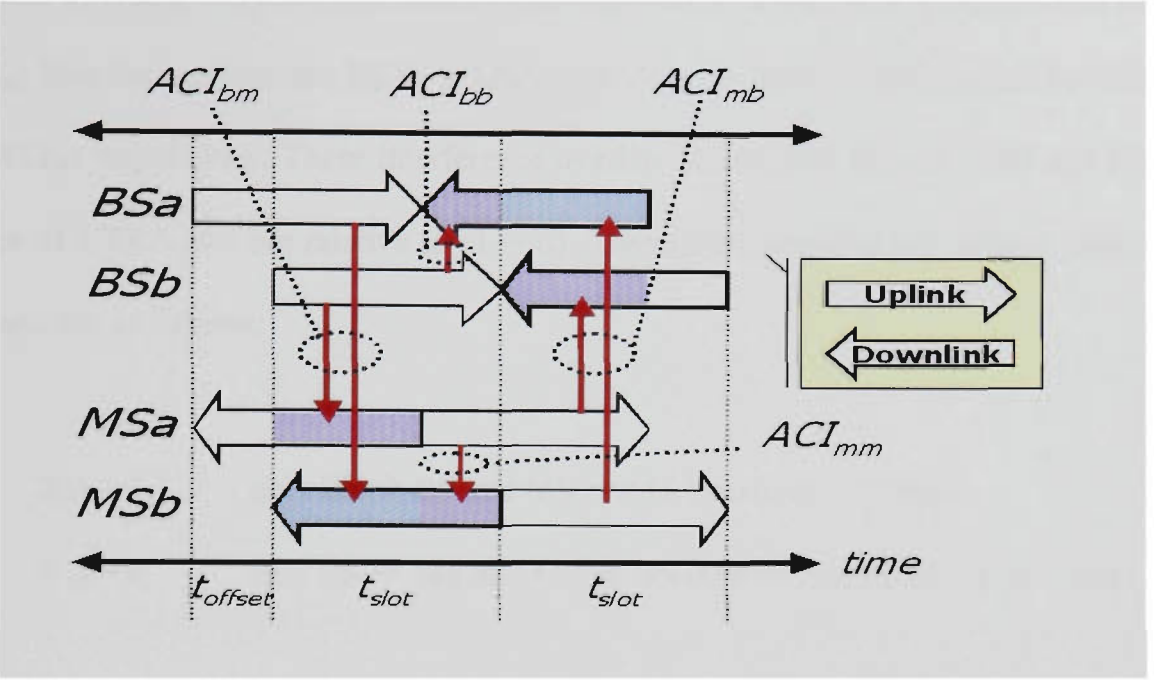


Figure 3.2 Downlink and Uplink Adjacent Channel Interference in UTRA-TDD dependent of frame synchronisation [71]

Operator *a* consists of one BS and one MS in session and is the same for operator *b*. Therefore, when operator *BSa* transmits data, *MSa* will receive the transmitted data. It also shows that there is time duration of frame misalignment between the two operators denoted as t_{offset}, as in reality it may be impossible to align frames of independent operators. To model the synchronisation between independent operators, α, the time offset is normalised by the frame duration which is denoted as t_{slot}, which yields [71]:

$$\alpha = \frac{t_{offset}}{t_{slot}} \tag{3.1}$$

Frame misalignment in UTRA-TDD creates two unique interference scenarios, which are relative to α. Firstly, interference between the two adjacent BS's, *a* and *b*, is depicted by ACI_{bb} and secondly, interference between *MSa* and *MSb* is represented with ACI_{mm}. Interference between BS's → MS's and MS's → BS's are represented by ACI_{bm} and ACI_{mb} respectively. These interference overlaps are mutual in both TDD and FDD modes of UTRA and are relative to $(1 - \alpha)$. Therefore, α depicts two unique cases of ACI and are as follows:

- If $\alpha = 1$, only BS → BS and MS → MS interference exists
- If $\alpha = 0$, only BS → MS and MS → BS interference exists (as in FDD)

The above two cases clearly outline that there still is an issue of interference whether independent operators are in synchronisation or not. As the interference can be considered independent due to various interference sources, the extent or magnitude of each category of interference (BS → BS, MS → MS, BS → MS or MS → MS) can contrast significantly. Various synchronisation factors also play a major role in the magnitude of interference. The subsequent sections only focus on downlink mode of TDD as this thesis concentrates on the receiver channel filter. Uplink interference analysis is not presented.

3.2.1.1 Downlink Power Control

The downlink power control model used in this chapter is based on the principle of the model related in [62]. The principle of the power control model is as follows: Firstly,

the code power, P_{rec}^{i} of the MS i that faces the greatest path loss within one time slot in the cell of interest (COI) is determined. Secondly, the same code power is applied for all users within that same time slot. This principle assures that the required or target bit energy to interference ratio (Eb/No) is satisfied for all users within that time slot. The *Eb/No* at a particular MS corresponds to [62]:

$$Eb/No = \frac{P_{rec}^{\ i} pg}{\tau(M-1)P_{rec}^{\ i} + \kappa^{i}\left(\frac{I_{adj}^{\ i}}{ACP} + \eta\right)} \tag{3.2}$$

where pg is the processing gain, M corresponds to the number of users served by the BS, $(M-1)P_{rec}^{i}$ is intra-cell interference depending on an orthogonality factor depicted as τ, ACP is the adjacent channel protection factor, η is thermal noise, I_{adj}^{i} is ACI, and κ^{i} is the maximum path loss for a MS in the time slot.

3.2.1.2 Indoor Propagation

The primary use of TDD is for high-speed data oriented services and its foremost use will be in indoor alike office environments. Therefore, the propagation model employed for the simulations in the chapter are based on the COST (COperation européenne dans le domaine de la recherche Scientifique et Technique) 231 indoor office environment excluding floor and wall losses as sited in [73]. This model represents the path loss model, κ and is defined in decibels (dB) as [73]:

$$\kappa = 37 + \gamma 10\log(d) + \xi \ \text{[dB]} \tag{3.3}$$

where γ is the path loss exponent and d is the separation between transmitter and receiver. Lognormal shadowing is modeled by ξ with a mean of zero and a standard deviation of σ dB. The receiver sensitivity is modeled as [65]:

$$Rs = (Eb/No) + \eta - pg + I_{addition} \text{ [dB]} \tag{3.4}$$

where $I_{addition}$ is an additional interference margin from the presence of other users in the same cell. $I_{addition}$ is modeled as [29]:

$$I_{addition} = \frac{1}{1 - \frac{(Eb/No)M - 1}{pg}} \tag{3.5}$$

where M is the number of users within the COI. Transmission power, Ptx, is derived from the receiver sensitivity, Rs, and the path loss model, κ, is as follows [29]:

$$Ptx = Rs + \kappa \text{ [dB]} \tag{3.6}$$

3.2.1.3 Downlink Interference Model

The extent of this work was restricted to downlink analysis. As noted earlier, MS's experience ACI from two sources, adjacent BS's and adjacent MS's depending on the synchronisation factorα. To gain an understanding of how this affects the amount of ACI experienced from BS's and MS's, we need to examine t_{offset}. A small t_{offset} results in a high BS→MS interference and a low MS→MS interference. It is vice versa for a large t_{offset}. We cannot assume synchronised frames in a fully flexible system; therefore the

computer simulations take into consideration misaligned frames and different asymmetry.

Evaluating ACI in the downlink with no ACP factor would give non-filtered ACI power, which means there is no presence of a receiver channel filter in the MS. It is required to obtain raw ACI to perform statistical analysis and to justify the requirement of a reconfigurable channel filter.

To determine the interference power from a single adjacent channel BS at a MS within the COI, we need to first determine the adjacent channel BS transmission power and the path loss between this BS and the MS within the COI. The ACI is then the BS transmission power multiplied by the number of users being served in the time slot of this adjacent channel cell, over the path loss and is given by I_{BS}:

$$I_{BS} = \frac{Ptx_{bs} M}{\kappa_{bs}} \tag{3.7}$$

where Ptx_{bs} is the adjacent channel BS transmission power, M is the number of users served by this BS, and κ_{bs} is the path loss between the adjacent channel BS and the MS within the COI. Based on this model, the total raw BS→MS ACI can be calculated with several adjacent channel interferers. Hence, raw BS→MS adjacent channel interference including a synchronisation factor is modeled by I_B [29]:

$$I_B = \sum_{j=1}^{H} (1-\alpha) \frac{Ptx^j M^j}{\kappa^j{}_{B_m}} \tag{3.8}$$

where $\kappa^j{}_{B_m}$ is the path loss between the j^{th} adjacent channel BS causing interference and the mobile located at m within the COI. H is the total number of BS's and M^j is the number of users served by the j^{th} BS. Ptx^j is the j^{th} adjacent BS transmission power. The user facing the greatest attenuation in an adjacent channel cell determines the transmission power of that adjacent channel BS. This results in high or low BS transmission powers.

To investigate the interference power from a single MS in one adjacent channel cell at a MS within the COI, the transmission power of the MS in the adjacent channel cell needs to be calculated. The path loss from the adjacent channel MS to the MS within the COI also need to be determined. The ACI, I_{MS}, results in:

$$I_{MS} = \frac{Ptx_{ms}}{\kappa_{ms}} \tag{3.9}$$

where Ptx_{ms} is the adjacent channel MS transmission power and κ_{ms} is the path loss between the adjacent channel MS and the MS within the COI. To investigate the raw MS→MS ACI caused by many MS's in many adjacent channel cells incorporating a synchronisation factor, the interference, I_M, results as [29]:

$$I_M = \sum_{j=1}^{H} \sum_{i=1}^{M} \alpha \frac{P^j tx_i}{\kappa^j{}_{M_{mi}}} \tag{3.10}$$

where $\kappa^{j}{}_{M_{mi}}$ is the path loss between the i^{th} MS in the j^{th} adjacent channel cell causing interference and the mobile m within the COI. $P^{j}tx_{i}$ is the MS transmission power. It can clearly be seen that when $\alpha = 0$, all ACI is sourced from the adjacent BS's. If $\alpha = 0.01$, this would mean that ninety nine percent of ACI is from adjacent channel BS's and one percent from adjacent channel MS's. The total ACI is a linear sum of both sources of interference. Therefore, the total downlink raw ACI power, $I_{adj(x,y)}$ at a MS at point m within the COI specified by the coordinates (x, y) is expressed as follows:

$$I_{adj}(x,y) = \overbrace{\sum_{j=1}^{H}\sum_{i=1}^{M}\alpha\frac{P^{j}tx_{i}}{\kappa^{j}{}_{Mmi(x,y)}}}^{I_{M}} + \overbrace{\sum_{j=1}^{H}(1-\alpha)\frac{Ptx^{j}M^{j}}{\kappa^{j}{}_{Bm(x,y)}}}^{I_{B}} \qquad (3.11)$$

3.2.2 Analysis of Adjacent Channel Interference

In this section, ACI is investigated with respect to the UTRA-TDD system. The analysis is achieved statistically with two scenarios; single interfering cell in section 3.2.2.1 and multiple interfering cells in section 3.2.2.2. The analysis is valid for a static simulated environment. The simulation parameters are listed in Table 3.1 and are identical for both scenarios. All MS users have a fixed bit rate of 32 Kbps where there are 8 interfering MS's in each interfering cell. The required *Eb/No* is 3.5 dB due to the assumption of a powerful coding mechanism, such as turbo coding. The inherent assumption was that UTRA-TDD is primarily used for data-oriented services. Three values of the local mean variability σ and various synchronisation factors have been considered to evaluate ACI.

Table 3.1 Simulation Parameters for ACI in UTRA-TDD

Parameter	*Value*
Bit Rate	32 Kbps
# of Monte Carlo Runs	10,000
# of Input Samples	1000
# of users in COI	8
Max TX Power (dB milli watts (dBm))	Downlink: 10, Uplink: 4
Thermal Noise (dBm)	−102.85
Required Eb/No (dB)	3.5
Receiver Sensitivity (dBm)	−115.09
Standard deviation σ (dB)	4, 8, 16
Cell Radius, R (meters (m))	100
# of Interfering Adjacent Cells	7 for Multiple Scenario 1 for Single Scenario
# of users in each Interfering Adjacent Cell	8
Synchronisation factor α	Uniform random 0 to 1
Path loss exponent γ	3.0
Orthogonality Factor τ	1
ACP	Not present

For an indoor propagation environment, a path loss exponent of 3 is suitable [29]. One parameter to note is that there is no ACP factor present in the simulations. The aim is to purely obtain raw ACI powers. Other simulation parameters, which include the maximum transmission power, thermal noise and the receiver sensitivity as well as the cell radius, are similar to the simulation parameters found in [29]. A few assumptions have also been taken into consideration that may affect the interference analysis and will be detailed at in the conclusion chapter of this thesis.

3.2.2.1 Single Adjacent Channel Interfering Cell

The cell topology for the case of a single interfering cell for downlink operation is depicted in Figure 3.3. The figure only illustrates BS→MS ACI, not MS→MS ACI for simplicity reasons but nevertheless, a similar principle applies in a graphical

representation. The cells are approximated with hexagons. The distance between adjacent BS's, denoted by d_b is set to 50 m. The distance between the BS within the COI (shaded cell) and the MS of interest is depicted by d_0 and d_1 depicts the distance between the adjacent BS and the MS within the COI.

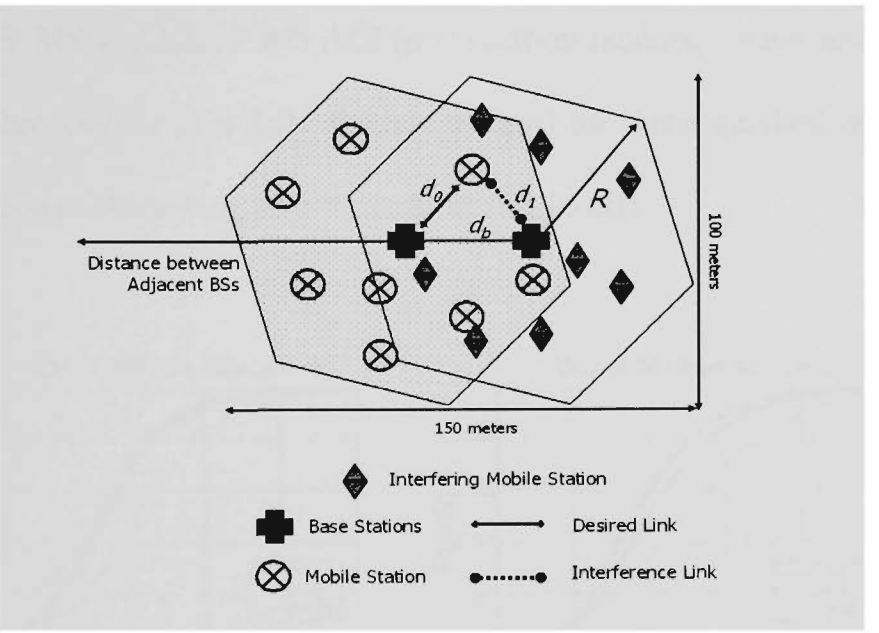


Figure 3.3 Single cell interference scenario where an adjacent cell is causing ACI to a MS in the cell of interest

All MS's within the COI and adjacent cell are distributed uniformly. ACI is calculated at the MS within the COI from adjacent BS's and MS's using equation (3.11). Monte Carlo simulations of 10,000 iterations are used to calculate the probability density functions (pdfs) and cumulative distribution functions (cdfs) of ACI powers. The number of Monte Carlo iterations used provided a solid foundation for the analysis where lower iterations did not. Figures 3.4 and 3.5 present cdfs and pdfs of ACI powers respectively. Four cases are presented and are as follows:

a) MS → MS ACI (α = 1) for three standard deviations of lognormal shadowing (σ= 4 dB, 8 dB and 16 dB)

b) BS → MS ACI (α = 0) for three standard deviations of lognormal shadowing (σ= 4 dB, 8 dB and 16 dB)

c) BS → MS and MS → MS ACI (α = 0.5, equal from MS and BS) for three standard deviations of lognormal shadowing (σ= 4 dB, 8 dB and 16 dB)

d) BS → MS and MS → MS ACI (α = uniform random, cannot assume a fixed synchronisation in a fully flexible system) for three standard deviations of lognormal shadowing (σ= 4 dB, 8 dB and 16 dB)

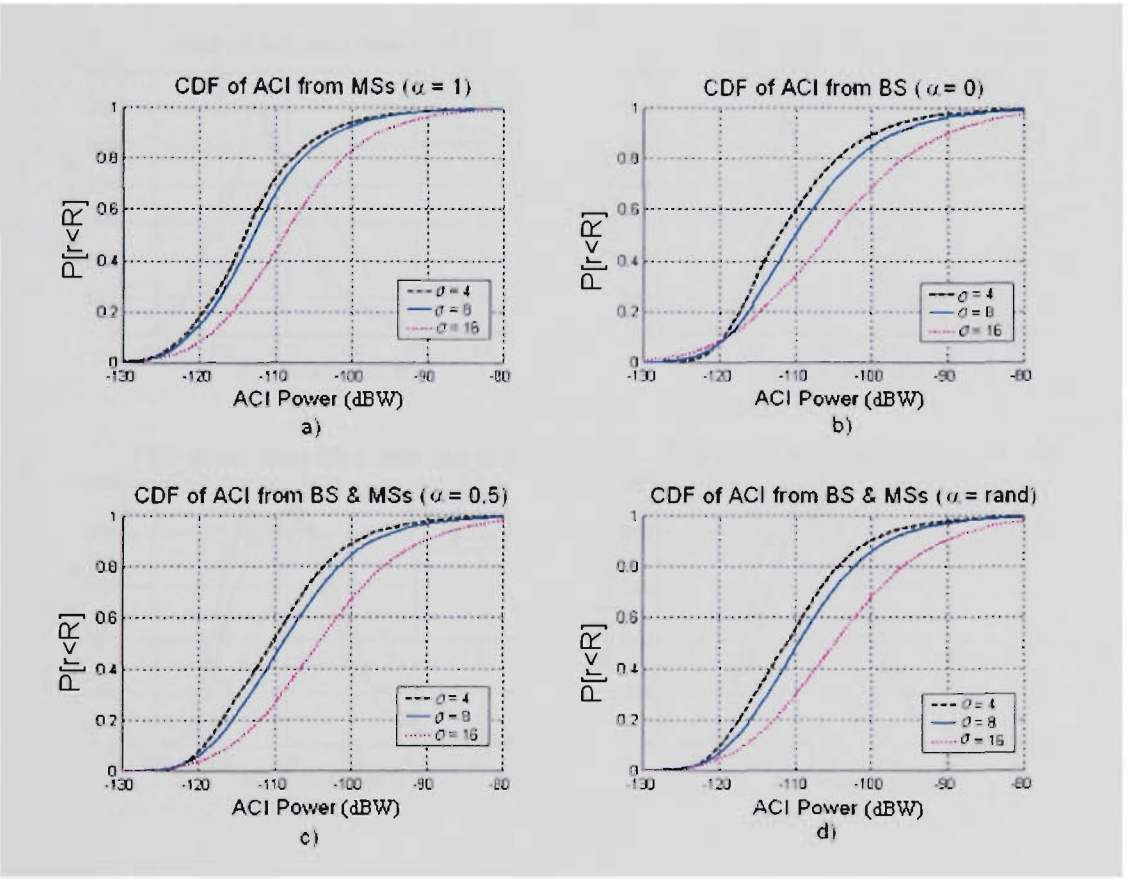


Figure 3.4 cdfs of ACI powers with variable synchronisation factors α and standard deviations σ for lognormal shadowing in a single interfering cell scenario

Results are presented in Tables 3.2, 3.3, 3.4 and 3.5 corresponding to Figures 3.4 a), b) c) and d) respectively. Analysing the first case where α = 1 (MS→MS ACI), the mean (E) ACI power tends to increase by 5.11 dB as the standard deviation σ of lognormal

shadowing increases from 4 dB to 16 dB. The standard deviation (STD) of ACI powers increase by 1.46 dB when σ increases from 4 dB to 16 dB. It is clear that varying the standard deviation of lognormal shadowing has a vital impact on ACI. Even though the lognormal shadowing variable has a mean of zero, the mean ACI powers increase as σ increases. There is only a 1.1 dB difference in the standard deviation of ACI powers for $\sigma = 4$ dB and $\sigma = 8$ dB. In this case, ACI is principally subject to cell geometry and random user distribution.

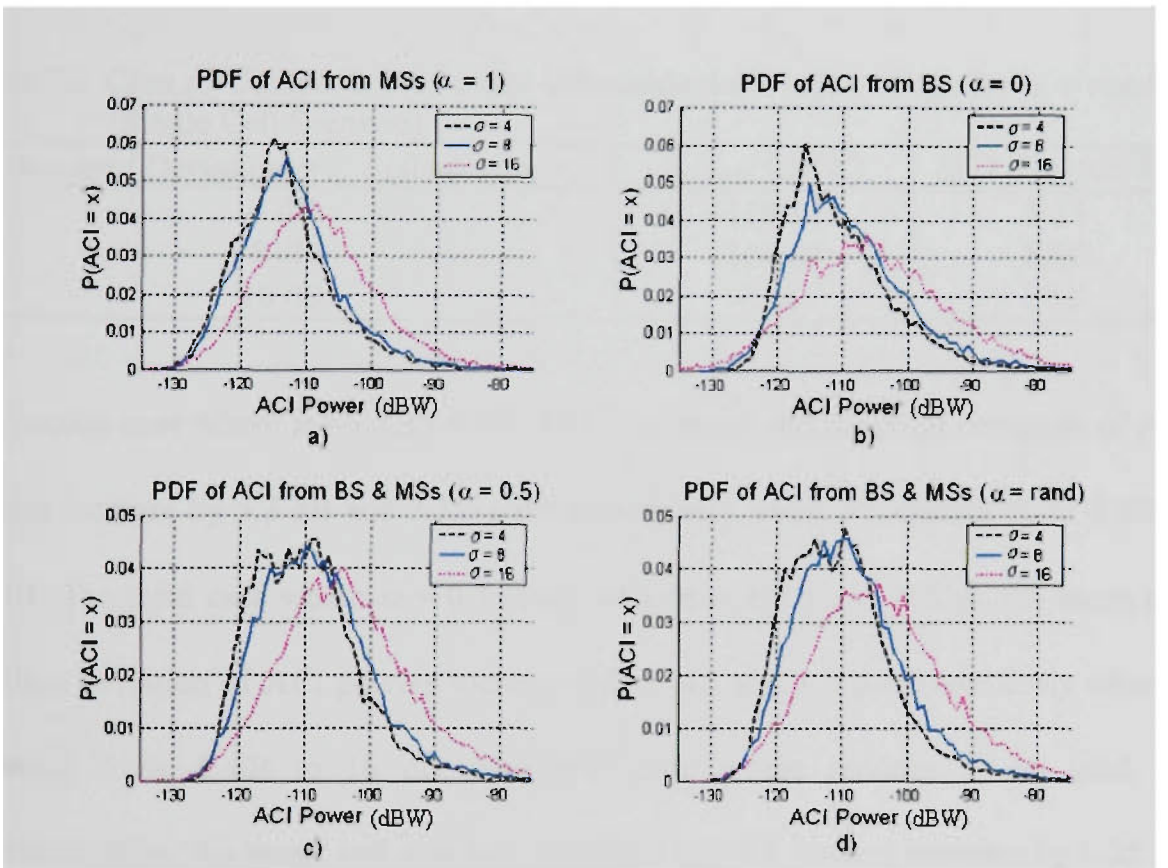


Figure 3.5 pdfs of ACI powers with variable synchronisation factors α and standard deviations σ for lognormal shadowing in a single interfering cell scenario

Table 3.2 *Case a)* Comparison of mean and standard deviation of I_{adj} for $\alpha = 1$ (Single Cell Scenario)

Standard Deviation σ *of* ξ (shadowing)	$E(I_{adj})$ (dB watts (dBW))	$STD(I_{adj})$ (dBW)
4 dB	−113.18	7.87
8 dB	−112.11	8.10
16 dB	−108.07	9.34

Table 3.3 *Case b)* Comparison of mean and standard deviation of I_{adj} for $\alpha = 0$ (Single Cell Scenario)

Standard Deviation σ of ξ (shadowing)	*E (I_{adj})* (dBW)	*STD (I_{adj})* (dBW)
4 dB	−110.57	8.34
8 dB	−108.75	9.18
16 dB	−104.91	11.6499

Table 3.4 *Case c)* Comparison of mean and standard deviation of I_{adj} for $\alpha = 0.5$ (Single Cell Scenario)

Standard Deviation σ of ξ (shadowing)	*E (I_{adj})* (dBW)	*STD (I_{adj})* (dBW)
4 dB	−109.71	8.27
8 dB	−108.11	8.82
16 dB	−103.48	10.26

Table 3.5 *Case d)* Comparison of mean and standard deviation of I_{adj} for α = *random* (Single Cell Scenario)

Standard Deviation σ of ξ (shadowing)	*E (I_{adj})* (dBW)	*STD (I_{adj})* (dBW)
4 dB	−110.36	8.23
8 dB	−108.69	8.60
16 dB	−104	10.5

The second case where $\alpha = 0$ (BS→MS ACI), the mean and standard deviation of ACI powers increase by 5.7 dB and 3.3111 dB respectively when σ increases from 4 dB to 16 dB. The third case where $\alpha = 0.5$ (even ACI from BS's and MS's), the mean and standard deviation of ACI powers increase by 6.2 dB and 1.9 dB respectively when σ increases from 4 dB to 16 dB. The final case where random α are used for synchronisation, the mean and standard deviation of ACI powers increase by 6.35 dB and 2.25 dB respectively when σ increases from 4 dB to 16 dB. Between the four cases, it is clear that the mean of ACI powers for the σ between 4 dB and 8 dB only varies the mean and standard deviation of ACI powers by (1.07 dB to 1.8 dB) and (0.23 dB to 0.85 dB) respectively. Increasing σ from 8 dB to 16 dB dramatically varies the mean and standard deviation of ACI powers by (3.8 dB to 4.7 dB) and (1.2 dB to 2.5 dB) respectively. It can be concluded that higher σ impacts the mean and standard deviation

of ACI powers whereas with lower σ, ACI powers are subject to cell geometry and random user distribution in the Monte Carlo simulations.

The four cases also reveal some interesting results, which are vital in this investigation. Thus far, the mean and standard deviation of each of the four cases has been examined. It is also clear that synchronisation factors α are the main drivers in the amount of ACI experienced. *Case a)* presents the 'best case' (lower ACI) of ACI where only MS→MS interference exists and the mean ACI for σ = 16 dB is −108.07 dBW. *Case b)* presents a worse case of ACI as the mean is −104.91 dBW for the same σ. Therefore, it can be stated that BS→MS ACI is more severe than MS→MS ACI based on eight users in each cell. A difference of 3.2 dB in the means concludes that *case b)* is 2.1 times more severe than *case a)* in terms of ACI power. The mean of ACI is further increased to −103.48 dBW for the same σ in *case c)*. The introduction of BS→MS ACI along with MS→MS ACI where α = 0.5 is 1.36 times more severe than BS→MS ACI alone and is nearly 2.9 times more severe than MS→MS ACI alone. This can be depicted as the 'worst case' (higher ACI) for this scenario. As synchronisation cannot be assumed in a fully flexible system, random α values are used in *case d)*. The mean ACI is slightly less severe than *case c)* but poses a great threat compared to the first two cases. It is also interesting to note that for low σ, synchronisation only varies the mean by (0.21 dB to 0.87 dB) except for *case a)* as BS→MS is dominating.

3.2.2.2 Multiple Adjacent Channel Interfering Cells

Code division multiple access (CDMA) systems have the potential to attain better flexibility than time division multiple access (TDMA) or frequency division multiple

access (FDMA) systems due to frequency or time slot reuse. Regardless of increased interference and accompanying effects on capacity, the system can be operated to allow high capacity and achieve greater flexibility [72]. The cell topology for the case of a multiple interfering cells for downlink operation is depicted in Figure 3.6.

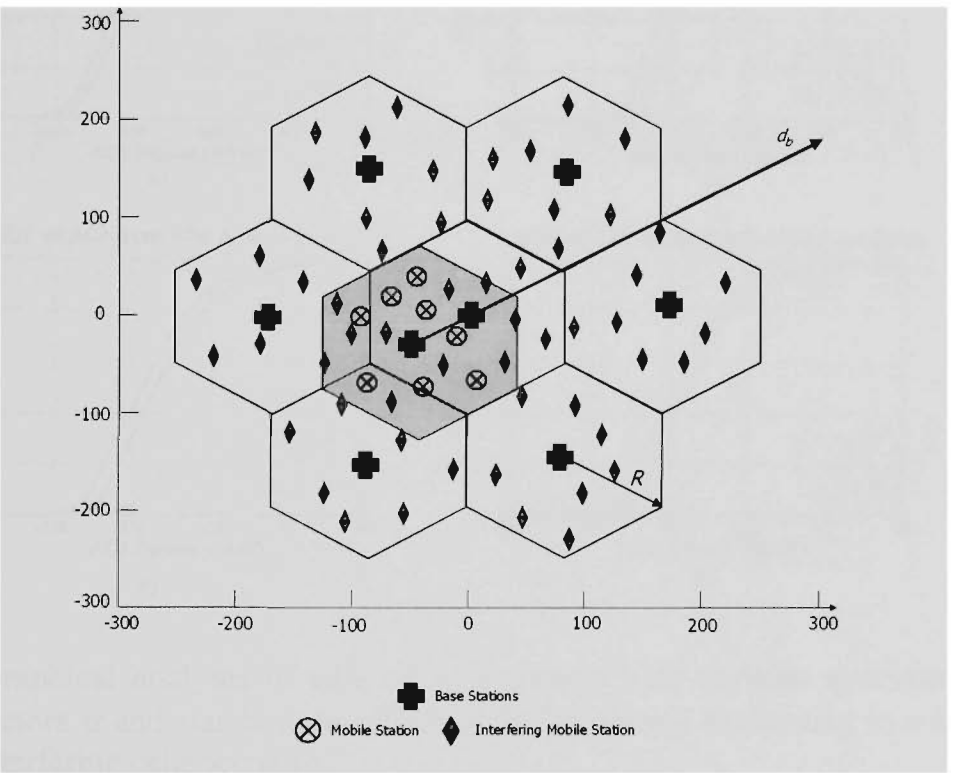


Figure 3.6 Multiple cells interference scenario where adjacent cells are causing ACI to a MS in the cell of interest. The units on the x and y axis are in meters.

The interference links are BS→MS and MS→MS. The cells are approximated with hexagons. The distance between the first adjacent BS and the BS within the COI, denoted by d_b is set to 50 m. All MS's within the COI and adjacent cells are distributed uniformly. ACI is calculated at the specified MS within the COI from adjacent BS's and MS's using equation (3.11). Monte Carlo simulations (corresponding to the number of iterations are per the single interfering cell scenario) are used to calculate the pdfs and cdfs of ACI powers. The layer of interfering cells was approximated with seven cells ACI was found to be inconsequential beyond this. Figures 3.7 and 3.8 present cdfs and

pdfs of ACI powers respectively. The four analysis cases described in the single interfering cell scenario are also valid for this investigation.

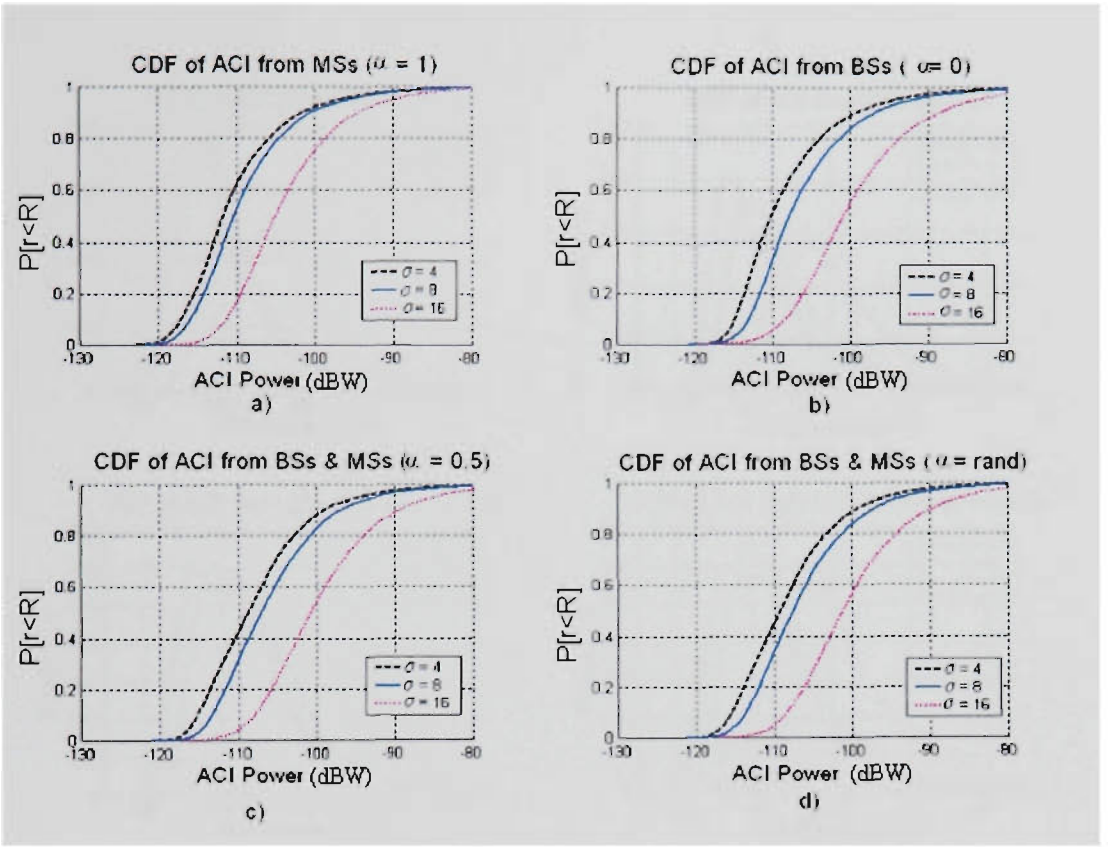


Figure 3.7 Graphical analyses of cdfs of ACI powers with variable synchronisation factors α and standard deviations σ for lognormal shadowing in a multiple interfering cells scenario

The results presented in Tables 3.6, 3.7, 3.8 and 3.9 that correspond to Figures 3.7 a), b), c) and d) respectively follow the same trend as the single interfering cell scenario investigated in section (3.2.2.1). As σ increases from 4 dB to 16 dB, the mean of ACI powers increases for each case by (6.57 dB to 8.84 dB), and the standard deviation of ACI powers increases by (0.42 dB to 1.23 dB). In the multiple interfering cells scenario, it seems that there is greater variance between the mean of ACI powers of the four cases and less variance between the standard deviation of ACI powers with various σ values, as compared with the single interfering cell scenario. This is due to the addition of six

interfering cells cluster along with the single interfering cell totalling a seven interfering cells cluster.

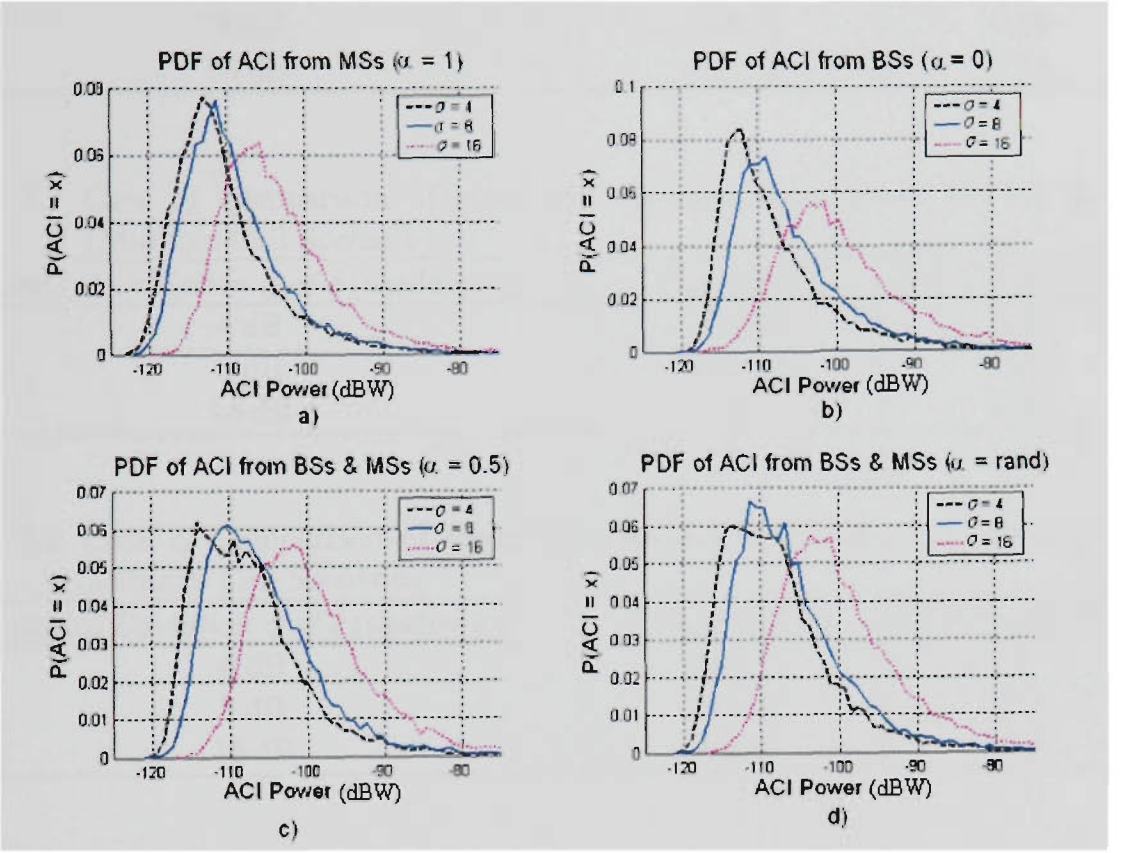


Figure 3.8 Graphical analyses of pdfs of ACI powers with variable synchronisation factors α and standard deviations σ for lognormal shadowing in a multiple interfering cells scenario

The synchronisation factors α also play a vital role in the severity of ACI. *Case a)* again, presents the 'best case' of ACI where only MS→MS interference exists and the mean ACI for $\sigma = 16$ dB is −103.7 dBW. *Case b)* in this scenario follows the same tendency as the single interfering cell scenario as BS→MS ACI is more severe than MS→MS ACI. The mean was recorded at −99.5 dBW. The 4.2 dB difference concludes that *case b)* provides 2.63 times the amount of ACI of *case a)*.

Table 3.6 *Case a)* Comparison of mean and standard deviation of I_{adj} for $\alpha = 1$ (Multiple Cell Scenario)

Standard Deviation σ of ξ (shadowing)	*E (I_{adj})* (dBW)	*STD (I_{adj})* (dBW)
4 dB	−110.27	6.84
8 dB	−108.92	6.86
16 dB	−103.7	7.25

Table 3.7 *Case b)* Comparison of mean and standard deviation of I_{adj} for $\alpha = 0$ (Multiple Cell Scenario)

Standard Deviation σ of ξ (shadowing)	*E (I_{adj})* (dBW)	*STD (I_{adj})* (dBW)
4 dB	−108.34	6.98
8 dB	−106.08	7.20
16 dB	−99.5	8.22

Table 3.8 *Case c)* Comparison of mean and standard deviation of I_{adj} for $\alpha = 0.5$ (Multiple Cell Scenario)

Standard Deviation σ of ξ (shadowing)	*E (I_{adj})* (dBW)	*STD (I_{adj})* (dBW)
4 dB	−107.75	7
8 dB	−105.79	7.2
16 dB	−99.46	7.9

Table 3.9 *Case d)* Comparison of mean and standard deviation of I_{adj} for α = *random* (Multiple Cell Scenario)

Standard Deviation σ of ξ (shadowing)	*E (I_{adj})* (dBW)	*STD (I_{adj})* (dBW)
4 dB	-108.1	7.01
8 dB	-106.18	7.19
16 dB	-99.84	7.93

Case c) further increases the mean of the ACI power to −99.46 dBW for the equivalent σ providing 1 and 3.65 times the ACI strength than *case b)* and *case a)* respectively. This case can also be represented as the 'worst case' for this scenario. The mean ACI power for *case d)* is slightly less severe (0.38 dB) than *case c)* when random synchronisation factors are used. The interesting and anticipated result in this scenario is that the ACI power severity is 2.52 to 3.24 times greater than that of the single interfering cell scenario even though there are seven interfering cells in this scenario.

This is due to the COI placement and user distribution within that cell and others where the major factor concerning the strength of ACI powers is the path loss and its logarithmic properties. Figure 3.9 illustrates the path loss with parameters specified in Table 3.1.

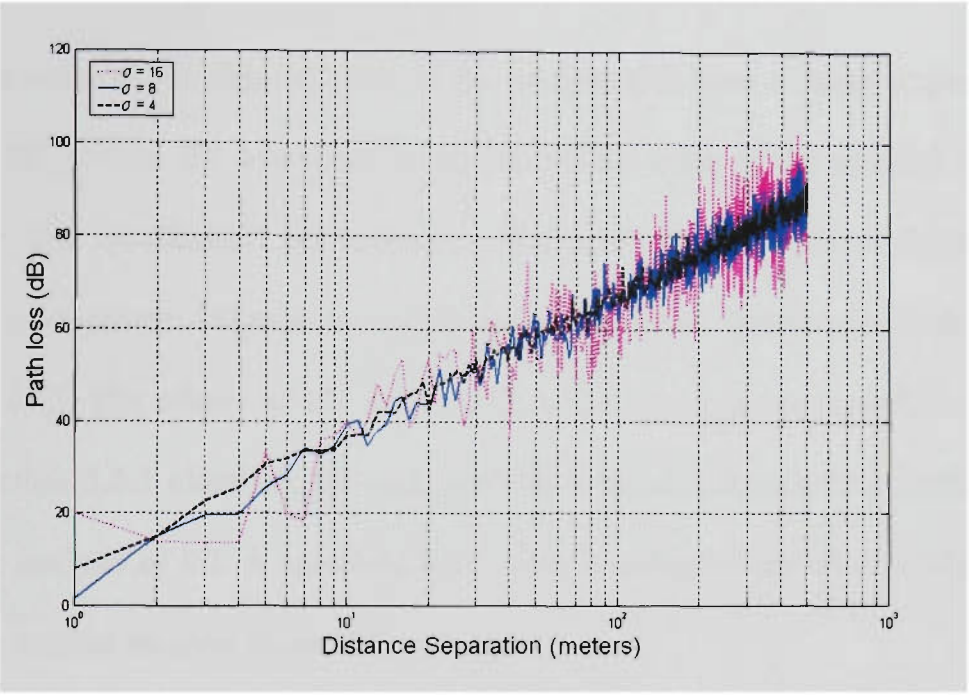


Figure 3.9 COST 231 indoor propagation path loss without floor or wall losses [73]

A separation of 50 m between interfering source and receiving source yields a path loss of (60 +ξ) dB and at 500 m separation, there is a loss of (90 +ξ) dB. Therefore, the ACI power of MS's and BS's varies depending on their separation distance with the MS within the COI. It is relatively apparent that the strength of ACI power is dependent on various dynamics. It is never constant and varies greatly.

Summarising the analysis on ACI, it can be said that ACI is greatly dependent on time synchronisation and channel asymmetry between adjacent cells. Lognormal shadowing also affected the severity of ACI powers. It was found that varying the standard deviation of the lognormal shadowing variable increased or decreased the mean and standard deviation of ACI powers. The key impact of these findings justifies the

necessity of a reconfigurable filter as ACI is never constant; therefore, the filters' efficiency can be increased.

3.3 Inter-Symbol Interference

Altering the order of the channel filter in the receiver can have a major impact on the severity of ISI powers. ISI would not be an issue if the order of the transmit filter and the receiver filter are identical, but in the case of a reconfigurable receiver channel filter, ISI may be quite severe. ISI must be considered as additional interference to the system apart from ACI. The effects of ISI in the UTRA-TDD system are investigated in this section. Section 3.3.1 classifies ISI and provides a general description. Section 3.3.2 provides an analysis of ISI. A baseband transceiver is designed and simulated to obtain results with various receiver channel filter lengths.

3.3.1 Classification of Inter-Symbol Interference

ISI is an inevitable consequence of both wired and wireless communication systems. Throughout early attempts of transmission, it was noticed that received signals had a propensity to get elongated into one another [74]. Figure 3.10 [74] illustrates an example of transmitted and received signals with ISI. The problem at first thought to be related to the properties of the medium used and the distance of signal travel. To combat this undesired effect, intermediate repeating stations were established and ways had to be devised to reduce this smearing [74].

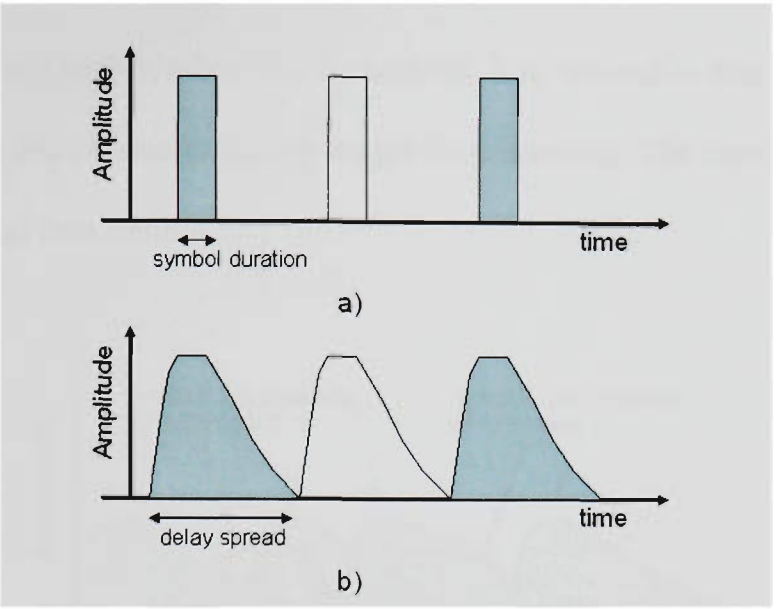


Figure 3.10 The effect of ISI on a transmitted data sequence. The received sequence illustrates a delay spread of the transmitted data symbol. [74] *(a) Transmitted data sequence (b) Received data sequence*

ISI still exists in digital communications affecting the symbols transmitted. Figure 3.11 [74] illustrates a data sequence, 101101 that are transmitted. This sequence is in form of square pulses. Square pulses are ideal as a concept but in practice they are complex to generate and require more than ample bandwidth. Therefore, the square pulses are shaped and are represented by the dotted line. This will in effect reduce the bandwidth requirements [74].

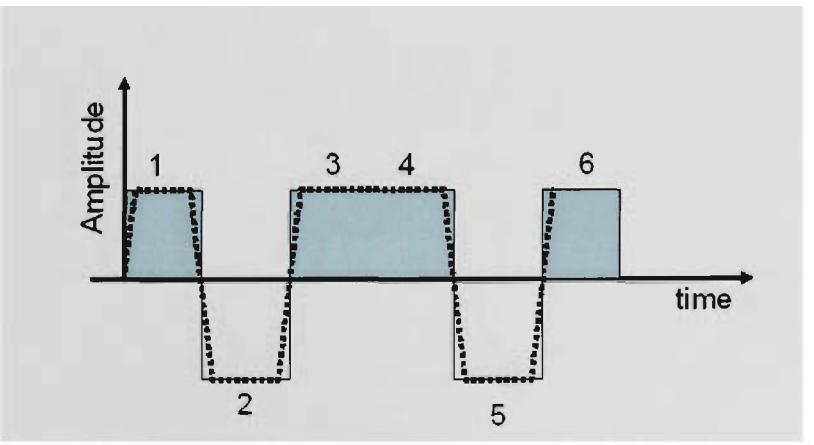


Figure 3.11 Sequence of transmit symbols (101101) [74]

Fig 3.12 [74] depicts each symbol as it is received. It is noticeable that the transmission medium creates a tail of energy lasting longer than intended. The energy from the first two symbols spread into symbol 3.

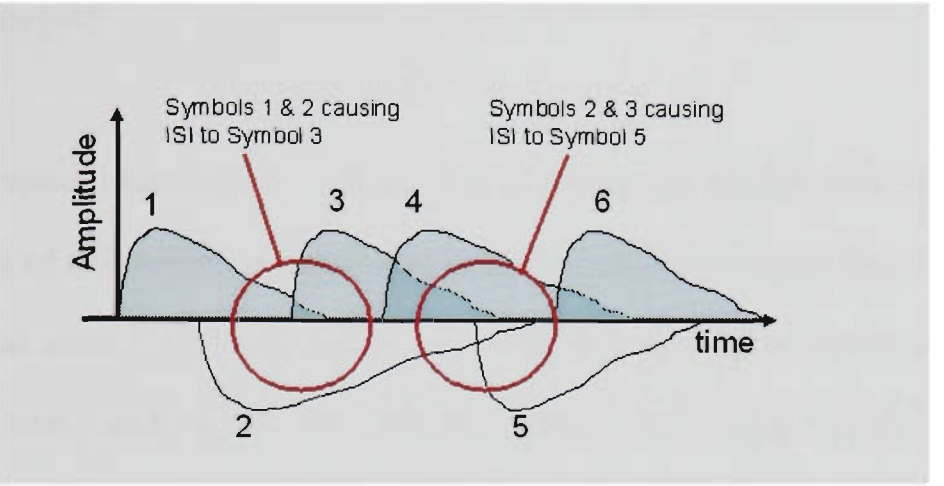


Figure 3.12 Received symbols illustrating smearing caused by the medium [**74**]

Figure 3.13 [74] illustrates the actual signal received as the sum of all the distorted symbols. In contrast to the transmitted signal (dashed), the received signal is quite distorted. The dots show the value of the amplitude at the timing instant. For symbol 3, this value is approximately half of the transmitted value, which makes this particular symbol more vulnerable to noise and inaccurate interpretation [74].

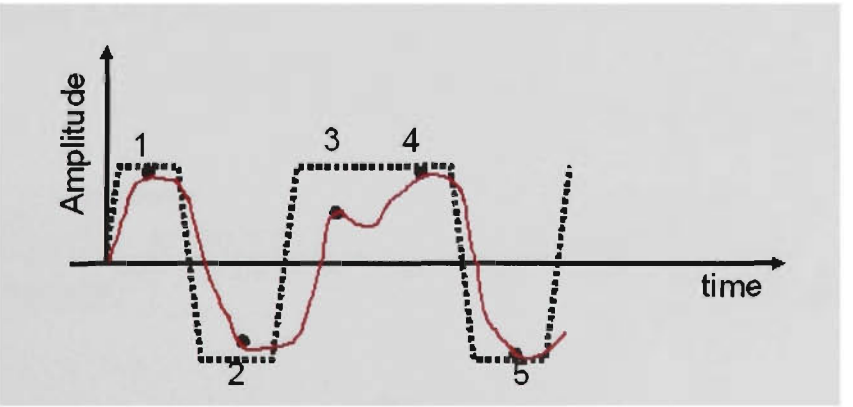


Figure 3.13 Received signal vs. the transmitted signal [**74**]

ISI can be caused by various phenomena. It can be caused by filtering effects from hardware or frequency selective fading, from non-linearities and from charging effects. Only a minority of systems are resistant to ISI and it is nearly always present in wireless communications [74].

One of the simplest techniques to reduce ISI is to reduce the symbol rate. Therefore, when a symbol of information is transmitted only after allowing the previous symbols' delay spread has eased [74]. This solution is not desirable, as many applications require high symbol rates, such as wireless communications. Nowadays, highly efficient processors, in terms of speed and power can control ISI through filtering the symbols in the transmitter and receiver. This is defined as pulse shaping where the secret lies in the digital demodulation process. Raised cosine filters in both transmitter and receiver are used. To implement the raised cosine response, the filtering is split into two components (root raised cosine) to create a matched set (raised cosine). The entire raised cosine can be applied once in the transmitter but in practice it has been established that concatenating two filters each with a root raised cosine response is more efficient as illustrated in Figure 3.14 [74].

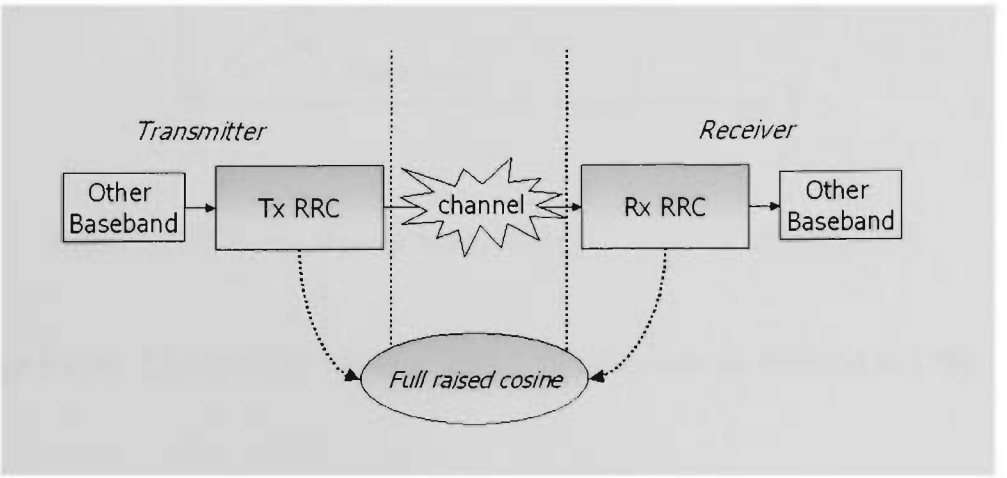


Figure 3.14 Pulse Shaping used to reduce ISI split into two separate root raised cosine (RRC) filters in transmitter and receiver [74]

3.3.1.1 Error Vector Magnitude

The error vector magnitude (EVM) can be used as a figure of merit for modulation systems and is used to measure ISI. The error vector represents the distance between a measured symbol at the receiver and the transmitted reference symbol. This is illustrated in Figure 3.15 [75].

EVM is used instead of the typical figure of merit, bit-error-rate (BER), as the BER experiences some limiting factors such as the requirement for dedicated equipment, long measurement intervals and a limited diagnostic value [76]. Other errors such as magnitude error and phase error are the differences between the measured and the reference symbols.

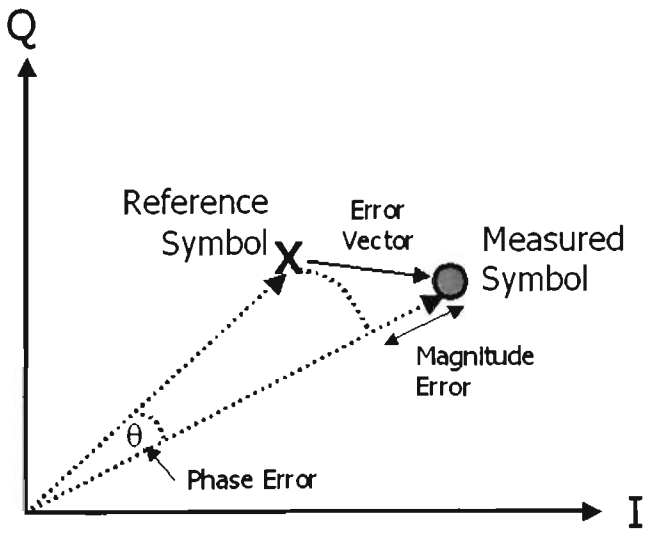


Figure 3.15 Error Vector Magnitude of complex symbol [75]

The average EVM, *EVM(dB)*, for *M*-modulated symbols can be defined as [76]:

$$EVM(dB) = 10\log_{10}\left(\sqrt{\frac{1}{M}\left(\sum_{m=1}^{M}\left(\Delta I_m{}^2 + \Delta Q_m{}^2\right)\right)^2}\right) \tag{3.12}$$

where ΔI and ΔQ are the differences between the references and measured I and Q values respectively. The accuracy of the modulation is affected by the root raised cosine filter length and coefficients. The average magnitude error, *MagnitudeError*, for *M*-modulated symbols can be defined as [76]:

$$MagnitudeError = \frac{1}{M}\sum_{m=1}^{M}\left(\sqrt{I_{measured\,m}{}^2 + Q_{measured\,m}{}^2} - \sqrt{I_{ideal\,m}{}^2 + Q_{ideal\,m}{}^2}\right) \tag{3.13}$$

where $I_{measured}$ and I_{ideal} are the measured and reference I values respectively and $Q_{meansured}$ and Q_{ideal} are the measured and reference Q values respectively. The corresponding phase error, *PhaseError*, for *M* modulated symbols is defined as follows [76]:

$$PhaseError = \frac{1}{M}\sum_{m=1}^{M}\left\{\left(\arctan\frac{Q_{measured\,m}}{I_{measured\,m}}\right) - \left(\arctan\frac{Q_{ideal\,m}}{I_{ideal\,m}}\right)\right\} \tag{3.14}$$

3.3.1.2 Modulation Error Ratio

Modulation Error Ratio (MER) is a measure of the constellation cluster variance due to any mutilation or transmitter deficiencies measured relative to the ideal constellation point locations. The EVM and MER are closely related and express the same information [77]. There is also a one to one relationship between the two. MER in some

cases may be uncomplicated to understand as it directly relates to the signal-to-noise ratio (SNR). The MER, *MER(dB)*, is defined in [77] and is:

$$MER(dB) = -10\log_{10}\left(\frac{\sum_{m=1}^{M}\left(\Delta I_m{}^2 + \Delta Q_m{}^2\right)}{\sum_{m=1}^{M}\left(I_{idealm}{}^2 + Q_{idealm}{}^2\right)}\right) \tag{3.15}$$

M is not directly related to the number of points in the constellation, but should be much greater than the number of points in the constellation in order to capture a representative sample. Typically M should be at least 10 times the number of points in the constellation [77].

In the presence of multiple CDMA codes, an individual code must be de-spread before measuring the MER with equation (3.15) [77]. On the other hand, if all codes are on, all codes can be de-spread at the signaling rate. Therefore, index m, would be split into two indices where m is an index across time, a second index, l, would be added that spans codes and the MER, *MER(dB)*, would result in [77]:

$$MER(dB) = -10\log_{10}\left(\frac{\sum_{m=1}^{M}\sum_{l=1}^{L}\left(\Delta I_{m,l}{}^2 + \Delta Q_{m,l}{}^2\right)}{\sum_{m=1}^{M}\sum_{l=1}^{L}\left(I_{idealm,l}{}^2 + Q_{idealm,l}{}^2\right)}\right) \tag{3.16}$$

where l runs over all codes and L is the number of active codes.

3.3.2 Receiver Channel Filter ISI Analysis

In this section, ISI is investigated with respect to the UTRA-TDD system. The purpose of this investigation was to determine what the minimum filter length could be for the reconfigurable filter without jeopardising the QoS of UTRA-TDD.

ISI is measured in terms of EVM and MER. Variable length receiver RRC filters are used to examine the effect of ISI on system performance. The analysis is only valid in a simulation environment. Figure 3.16 presents the baseband transceiver system for the simulation purpose of this investigation. Simulation parameters are presented in Table 3.10.

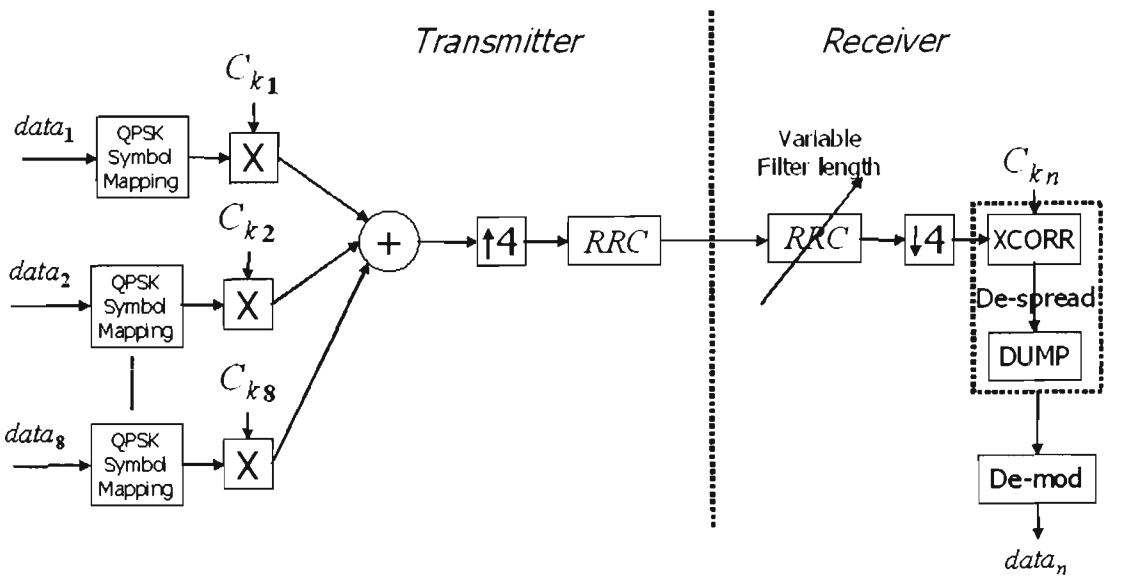


Figure 3.16 UTRA-TDD Baseband Transceiver used for ISI investigation

The simulation platform consists of 8 users of QPSK symbol mapped data each spread with an OVSF code of length 16. The transmit (Tx) RRC filter has a length of 57. The

receiver (Rx) RRC filter length is variable from 3 to 57. The signal is de-spread with a specific code for user *k*. The received QPSK symbols are weighed against the transmitted QPSK symbols of user *k* and the EVM as well as the MER are calculated. The *Eb/No* is set to 3.5 dB and the work is restricted to one time slot.

Table 3.10 Simulation parameters for ISI investigation

Parameter	*Value*
Number of users in time slot	8
Bit Rate	32 Kbps
Number of transmitted bits per user	5000
OVSF code length	16
Eb/No	3.5 dB
Tx RRC Filter length	57
Rx RRC Filter length	Variable (3 to 57)
C_{k1}	1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1
C_{k2}	1,1,1,1,1,1,1,1,-1,-1,-1,-1,-1,-1,-1,-1
C_{k3}	1,1,1,1,-1,-1,-1,-1,1,1,1,1,-1,-1,-1,-1
C_{k4}	1,1,1,1,-1,-1,-1,-1,-1,-1,-1,-1,1,1,1,1
C_{k5}	1,1,-1,-1,1,1,-1,-1,1,1,-1,-1,1,1,-1,-1
C_{k6}	1,1,-1,-1,1,1,-1,-1,-1,-1,1,1,-1,-1,1,1
C_{k7}	1,1,-1,-1,-1,-1,1,1,1,1,-1,-1,-1,-1,1,1
C_{k8}	1,1,-1,-1,-1,-1,1,1,-1,-1,1,1,1,1,-1,-1

Figure 3.17 illustrates the effect of reducing the receiver filters' length with a graphical representation of the received symbols constellation map. The figure depicts four cases as follows:

a) Both transmitter and receiver RRC filters employ the same length (matched)

b) The receiver RRC filters' length has been reduced to 31

c) The receiver RRC filters' length has been reduced to 17

d) The receiver RRC filters' length has been reduced to 9

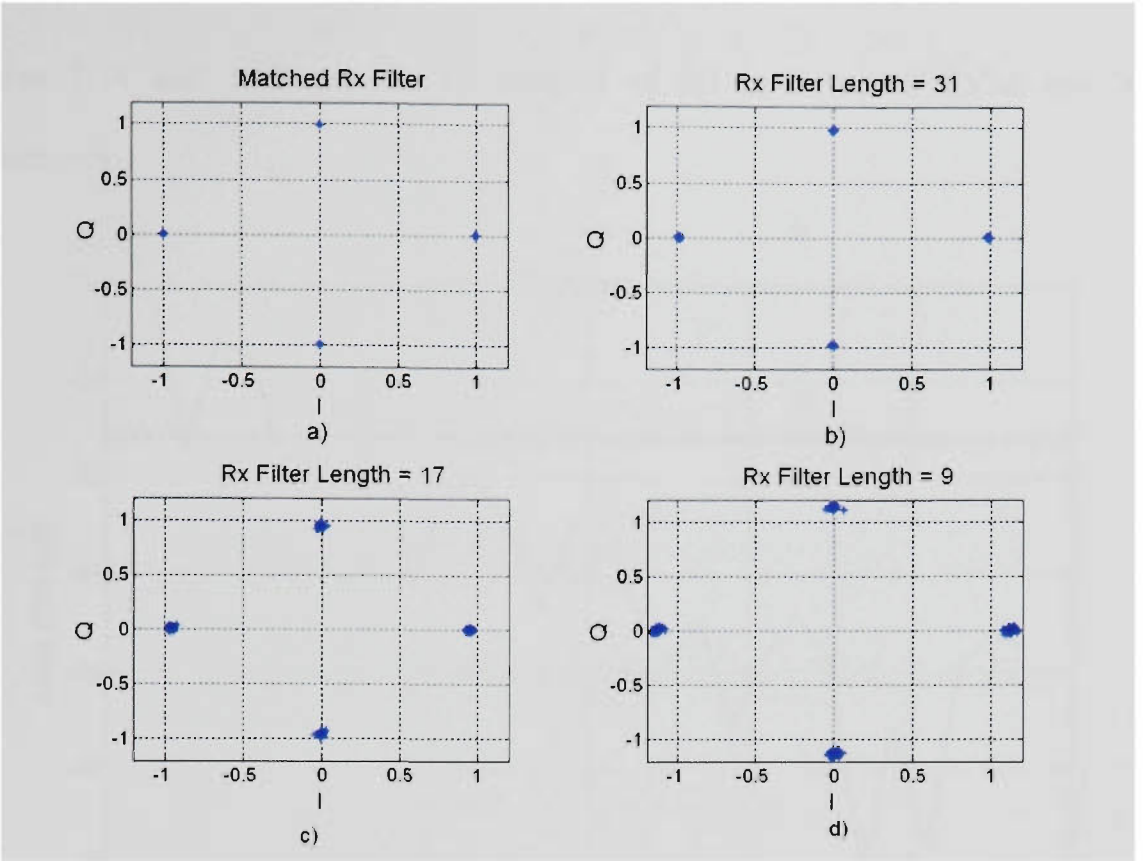


Figure 3.17 The effect of reducing the Rx RRC filters' length results in increased ISI

Figure 3.17 a) demonstrates that ISI is at a minimum and does not provide any problem as the transmitter RRC filter and receiver RRC filter are matched in terms of length and coefficient values. As the receiver filter length is reduced to 31 as shown in Figure 3.17 b), ISI begins to increase. The received symbols in the constellation map now have a spread variance in contrast to the transmitted symbols. Reducing the filter length further in the receiver results in greater ISI as presented in Figure 3.17 c) and d). Here the received symbols have a greater variance causing much concern. *Case d)* which employs a filter length of only 9 illustrates that the received symbols have essentially shifted from the desired constellation point, as well as having a greater spread variance. The shift is due to the distortion in the pass band of the receiver filter caused by a low filter length and it essentially adds to the amount of ISI as the error between transmitted and received symbols is greater.

Figures 3.18 and 3.19 provide an analysis of ISI in terms of EVM and MER respectively.

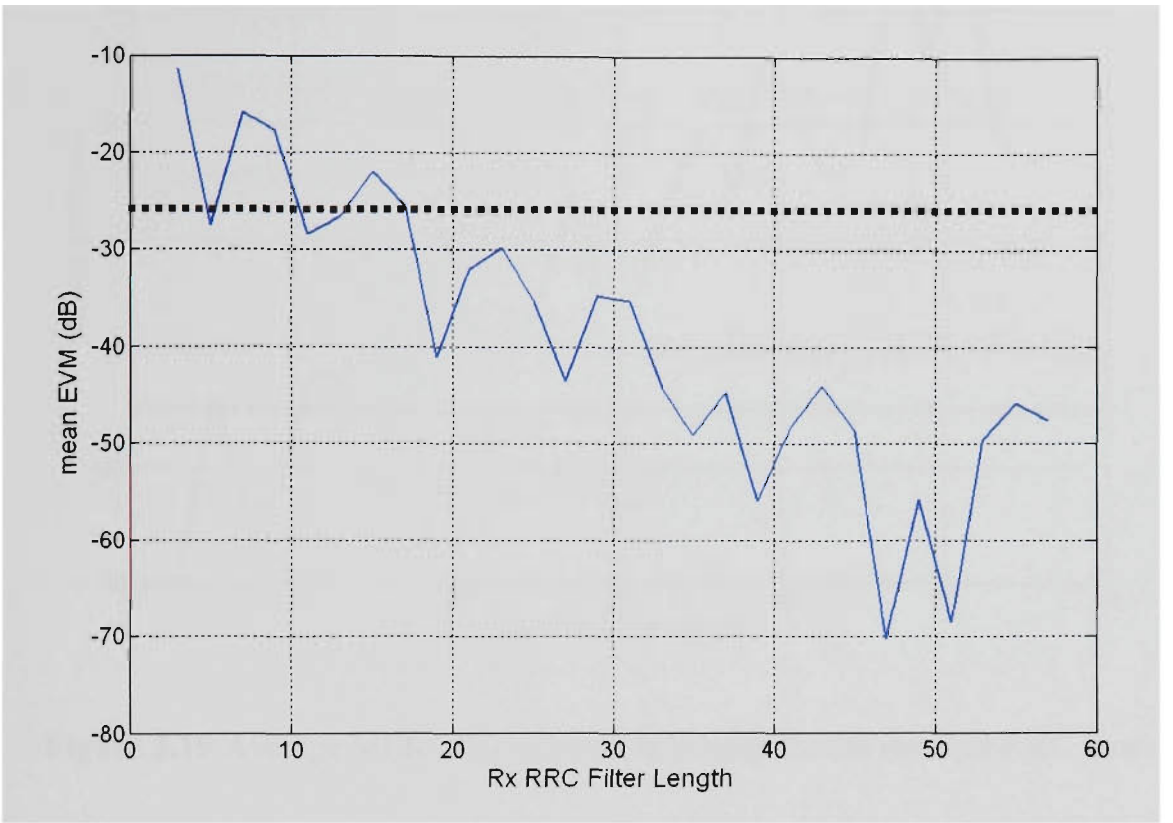


Figure 3.18 Average EVM (dB) of variable lengths for the receiver RRC filer

The required SNR for adequate performance is 6.51 dB (2 * Eb/No) for a QPSK modulator. An additional safety margin of 20 dB is acceptable to ensure the noise performance of the receiver is not affected. In terms of EVM, this leads to –26.51 dB and the filter length is required to be less to ensure the QoS is met.

Figure 3.18 clearly demonstrates that a filter length below the dotted margin line is adequate and will not affect the noise performance of the receiver. Therefore acceptable filter lengths are 5, 11, 13 and $\geq$ 19 where the minimum filter length is 5.

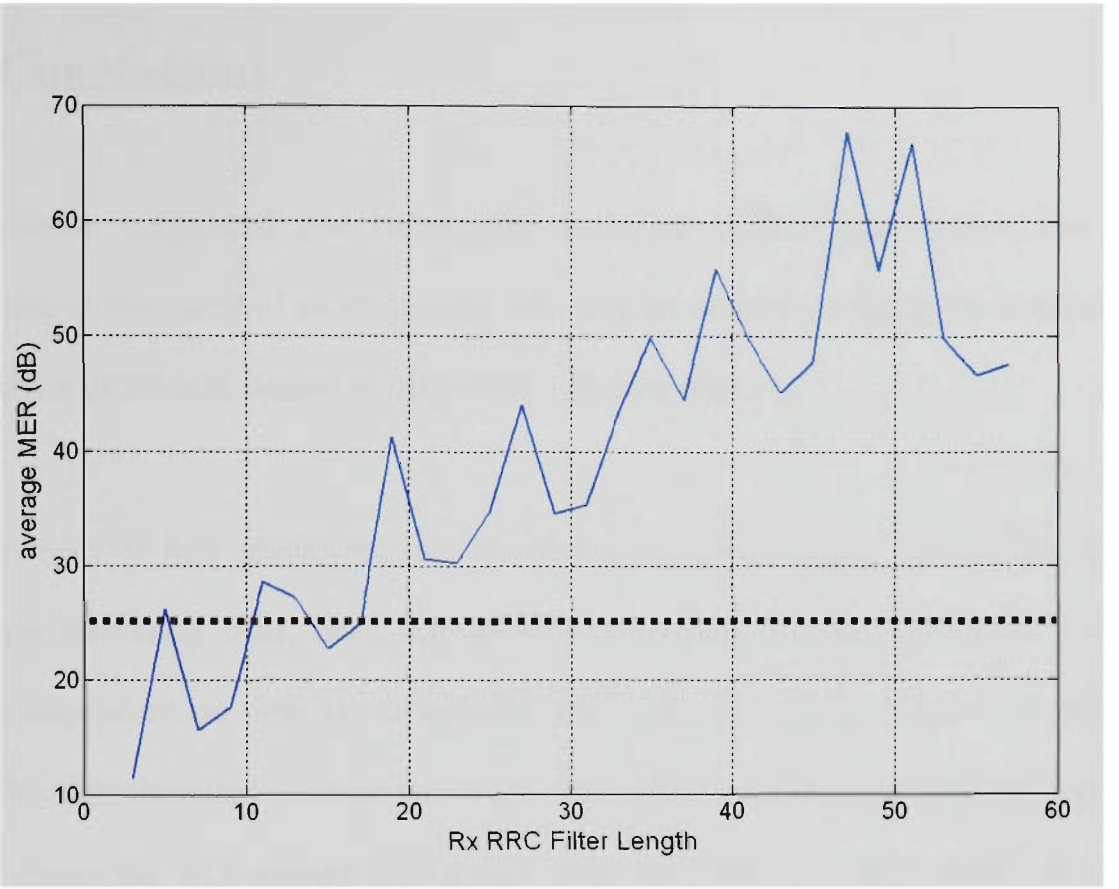


Figure 3.19 Average MER (dB) of variable lengths for the receiver RRC filer

The MER represents a similar analysis of ISI except that the information presented is in terms of a ratio. The ratio is the error between transmitted and received symbols, to the transmitted symbols. Identical QoS margin is used (SNR of 6.51 dB and safety margin of 20 dB), which leads to 26.51 dB of MER.

Figure 3.19 illustrates that filter length above the dotted line is adequate and will not affect the noise performance of the receiver. In terms of acceptable filter lengths for a reconfigurable filter, the identical filters lengths of the EVM analysis applies to this analysis. Therefore, both analyses provided the same concluding results.

3.4 Conclusions

This chapter considered two issues inherent to an UTRA-TDD system. The first investigation consisted of an analysis of ACI and the second investigation consisted of an analysis of ISI with respect to the receiver channel filter.

The analysis of ACI considered two interfering scenarios; single interfering cell and multiple interfering cells. Both scenarios demonstrated that the severity of ACI is greatly dependent on time synchronisation and channel asymmetry between adjacent cells. Non-synchronised cells for the single interfering scenario can cause between 2.07 to 2.9 times the ACI powers for various σ as compared to synchronised cells. The severity is higher in the multiple interfering cells scenario yielding 2.63 to 3.65 times the ACI powers. This is dependent on cell cluster geometry and user distribution.

Contrasting the ACI powers in both scenarios, the multiple interfering cells scenario can be 2.52 to 3.24 times more severe than the single interfering cell due to the addition of six interfering cells. Lognormal shadowing also affected the severity of ACI powers. It was found that varying the standard deviation of the lognormal shadowing variable increased or decreased the mean and standard deviation of ACI powers. The single interfering cell scenario yielded mean and standard deviation variances of (1.07 dB to 1.82 dB) and (0.227 dB to 0.84 dB) respectively for σ between 4 dB and 8 dB. Increasing σ from 8 dB to 16 dB further varies the mean and standard deviation of ACI powers by (3.84 dB to 4.68 dB) and (1.23 dB to 2.46 dB) respectively. The multiple

interfering cells scenario yielded mean ACI power variations of (6.57 dB to 8.84 dB) and (0.42 dB to 1.24 dB) standard deviation variations for σ values of 4 dB to 16 dB.

It is relatively apparent that the strength of ACI power is dependent on various dynamics. It is never constant and varies greatly. Therefore, it is inefficient to employ a standard fixed length receiver channel filter to mitigate ACI. The fixed length ensured the filters' attenuation caters for the worst-case environment set by the specifications of the system. This is disadvantageous as the system will not always operate in the worst-case is environment. Complex high order digital filters are demanding on battery power in the MS and a fixed length will result in unnecessary power drain. A high filter length may be required when a MS of interest is operating in the vicinity of an adjacent BS or MS and the adjacent operators are not synchronised. The pdfs and cdfs illustrated in the ACI analysis indicate that there is a low probability of high ACI. Other times, a lower filter length may be required when ACI is not quite severe. This investigation has given insight to ACI and has prompted the design and implementation of a reconfigurable digital channel filter with a variable length for the TDD receiver and is discussed in the next chapter.

This chapter also examined the effect a variable length receiver channel filter has on ISI in the UTRA-TDD system. The investigation revealed that decreasing the length of the receiver filter resulted in an increase of ISI. The received symbols on the constellation map showed a spread variance when the length of the filter was reduced. The spread variance tended to rise when the length of the filter was further reduced. An EVM and MER analysis was conducted to yield acceptable filter lengths that do not affect the noise performance of the receiver. A QoS margin was set to −26.51 dB for the EVM

analysis and 26.51 for the MER analysis. Both analyses produced the same concluding results yielding acceptable filter lengths of 5, 11, 13 and ≥19 where the minimum filter length can be 5.

Chapter 4

Reconfigurable Root Raised Cosine Filter Design

4.1 Introduction

In this chapter, a novel reconfigurable root raised cosine (RRC) filter applicable to the mobile receiver of time division duplex (TDD) mode of the universal mobile telephone service (UMTS) terrestrial radio access (UTRA) is presented. The discovery made in this chapter exploits the major findings of Chapter 3; that is, the strength of adjacent channel interference (ACI) power is dependent on various dynamics and there is a minor probability of highly severe ACI powers. Therefore, a fixed length for the receiver filter will be inefficient and result in unnecessary power drain of the mobile battery. The findings in Chapter 3 also yielded acceptable filter lengths that will not affect the noise performance of the receiver by inter-symbol interference (ISI) analysis.

The basic concept of the novel filter is to only utilise the required adjacent channel selectivity (ACS) to meet the specified bit-energy to interference ratio (Eb/No) by

employing variable ACS, which would improve the efficiency of the system. ACS is a measure of a receiver's ability to receive a wanted signal at its assigned channel frequency in the presence of an adjacent channel signal at a given frequency offset from the centre frequency of the assigned channel. Explicitly, it is the ratio of the receive filter attenuation on the assigned channel frequency to the receiver filter attenuation on the adjacent channel(s) [25, 78]. The ACS power, which meets the required Eb/No depends on the strength of ACI powers (out-of-band) received and the power of the in-band (desired signal and intra-cell interference) received power. This concept is demonstrated in a spectrum analysis presented in Figure 4.1. If ACI and intra-cell interference powers are low, the ACS of the filter can be reduced to a level that satisfies the Eb/No, therefore saving battery power. Otherwise, if ACI and intra-cell interference powers have increased in severity, the ACS of the filter may have to increase to meet the Eb/No and not affect the noise performance of the receiver. The in-band and out-of-band signal powers are monitored in real time.

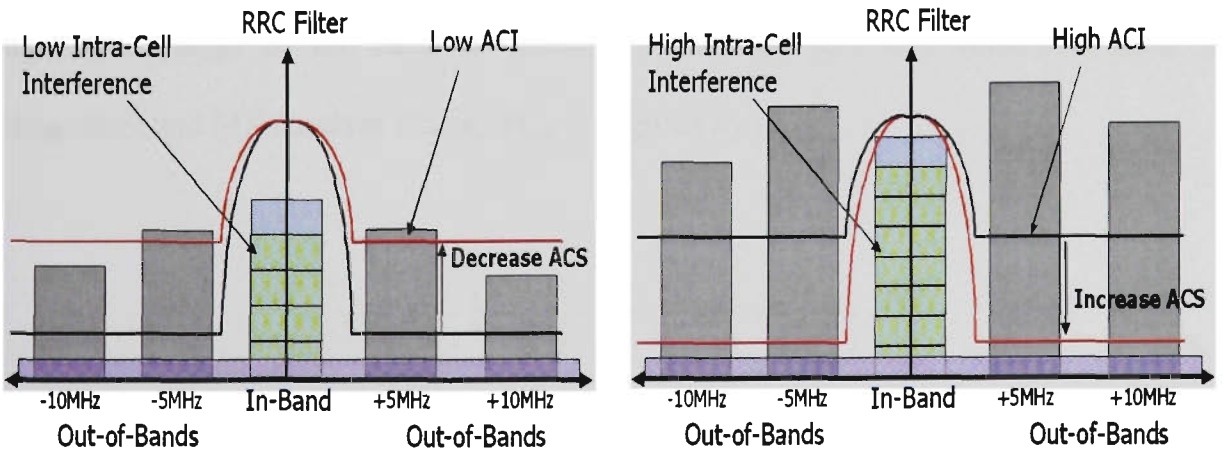


Figure 4.1 Spectrum analysis of operational concept of reconfigurable filter

This chapter is structured as follows: section 4.2 details the specifications of the receiver RRC filter based on 3rd Generation Partnership Project (3GPP) specifications. Details of the reconfigurable filter system architecture are presented in section 4.3. All components in the architecture are described and their operations are presented. Conclusions to this chapter are presented in section 4.4.

4.2 Specification Considerations

Design aspects of the mobile station (MS) receiver RRC filter to some degree depend on the design aspects of the transmitter RRC filter in the base station (BS) (for downlink operation). The unique property of RRC filters, apart from mitigating interference in unwanted frequency bands is that they are commonly used in digital data communication systems to limit ISI. Another unique property is the impulse response is zero at each adjacent symbol period. The sampling frequency of the transmitter and receiver filters must be matched and the key factor that determines it is the interpolation factor of the transmitter. Therefore, an analysis of the transmitter filter is performed to assist the design of the receiver filter. The impulse response mutual to both BS transmitter and MS receiver filters, $RC_0(t)$ is given by [23]:

$$RC_0(t) = \frac{\sin\left(\pi \frac{t}{T_C}\left(1-\bar{\alpha}\right)\right) + 4\bar{\alpha}\frac{t}{T_C}\cos\left(\pi \frac{t}{T_C}\left(1+\bar{\alpha}\right)\right)}{\pi \frac{t}{T_C}\left(1-\left(4\bar{\alpha}\frac{t}{T_C}\right)^2\right)} \tag{4.1}$$

where the roll-off factor, $\bar{\alpha}$, is 0.22. Both filters are low pass filters (LPF). The roll-off factor defines the cut-off frequency sharpness where a higher roll-off factor is more lenient. *Tc* is the chip duration defined by:

$$T_C = \frac{1}{chiprate} \approx 0.26042\ microseconds\ (\mu s) \tag{4.2}$$

where the chip rate = 3.84 Mega chips per second (Mcps).

4.2.1 Transmit RRC Filter Considerations

The responsibility of the transmit RRC filter is to bound the bandwidth of the transmitted signal and to reduce the amount of adjacent channel leakage power. Three transmit FIR filter designs of various interpolation factors are investigated. Table 4.1 presents the specifications of the filter based on 3GPP specifications [24]. Three interpolation factors are used to produce three varying filters of diverse sampling frequencies and complexities. The transmit filter must satisfy the adjacent channel leakage ratio (ACLR) specified by 3GPP. The ACLR is the ratio of the transmitted power to the power measured in an adjacent channel. Both the transmitted and the adjacent channel power are measured through a matched filter (RRC with a roll-off = 0.22) with a noise power bandwidth equal to the chip rate and shall apply for all configurations of a BS (single carrier or multi-carrier) [24].

Table 4.1 Transmit RRC Filter Specifications

Parameter	*Value*
Chip Rate	3.84 Mega symbols per second [24]
Cut-off Frequency, *Fo*	Chip Rate / 2 [24]
Sampling Frequency, *Fs*	Interpolation factor (1, 4 and 8) * Chip Rate
ACLR	45 decibels (dB), ± 5 Megahertz (MHz) BS adjacent channel offset [24]
	55 dB, ± 10 MHz BS adjacent channel offset [24]

3GPP specifications assert that in case the equipment is operated in proximity to another TDD BS or frequency division duplex (FDD) BS operating on the first or second adjacent frequency, the ACLR shall be higher than the values specified in Table 4.1 and will be 70 dB for ± 5 MHz and ± 10 MHz BS adjacent channel offsets. The requirement is based on the assumption that the coupling loss between the base stations is at least 84 dB [24].

Table 4.2 presents the results for each filter design with various interpolation factors. The designs were not considered for BS close proximity operation with other BS's. The results were obtained in a simulation environment. It is apparent from the results that various interpolation factors produce diverse filter designs and characteristics. It affects the sampling frequency, complexity and the attenuation of the filter.

Table 4.2 Simulation Results of transmitter pulse-shape filters

Parameter	*Filter 1*	*Filter 2*	*Filter 3*
Interpolation Factor	2	4	8
Roll-off factor	0.22	0.22	0.22
Cut-off Frequency, *Fo*	1.92 MHz	1.92 MHz	1.92 MHz
Sample Frequency, *Fs*	7.68 MHz	15.36 MHz	30.72 MHz
Filter Length	33	65	129
ACLR, ± 5 MHz adjacent channel (dB)	44.288	55.876	63.230

The major factor influencing which filter design to choose is the tradeoff that there is between the transmitter pulse-shaping filter and the analog reconstruction filter. If the RRC filters length is low and the sampling frequency is low, the reconstruction filter will need to be of a high order to achieve a sharp roll off. This is due to the low

sampling frequency of the pulse-shape filter that only allows a smaller transition bandwidth for the reconstruction filter. Although the RRC filter will dissipate less power due to its low complexity, the reconstruction filter will be of high complexity. Figure 4.2 illustrates the magnitude response of the three transmit filter designs.

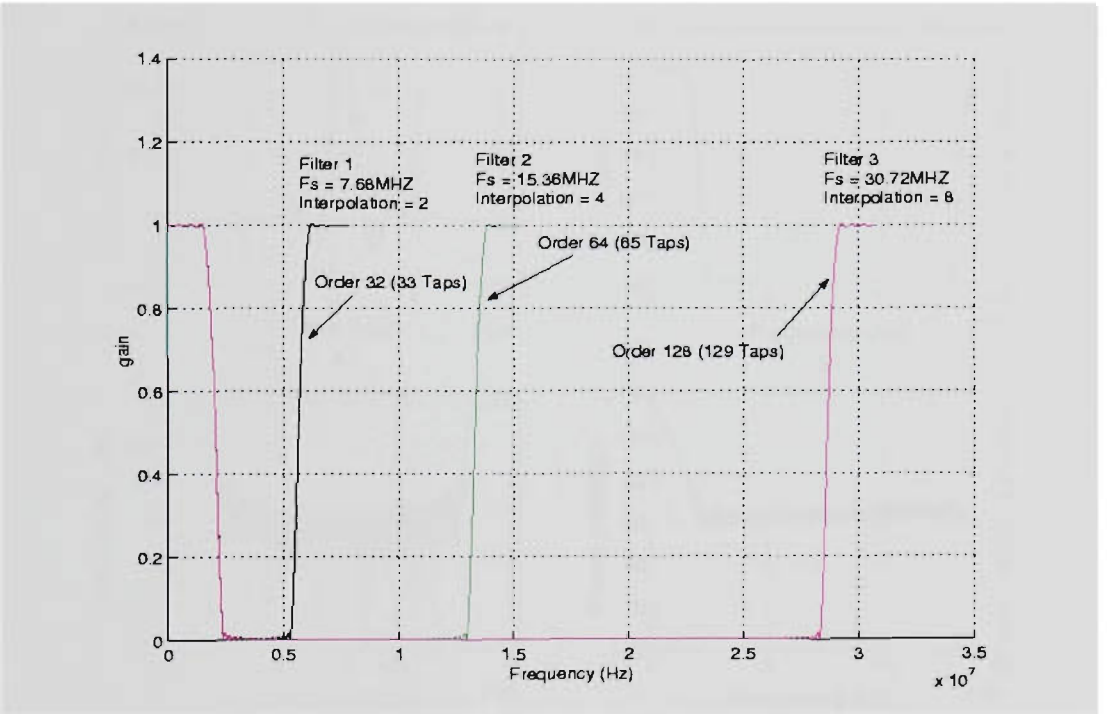


Figure 4.2 Comparison of magnitude frequency response of transmit filters

Filter 1 does not meet the ACLR specifications due to its low complexity. *Filter 3* meets the specified ACLR but is of high complexity and is costly to implement. *Filter 2* satisfies the tradeoff with the analog reconstruction filter and meets the ACLR specification. Figure 4.3 depicts the characteristics of *Filter 2*. The impulse response of the filter is presented in Figure 4.3 a) where *RCo* are the impulse response values. It is convolved with the filters input to obtain the filters output. The magnitude and log magnitude frequency responses are presented in Figure b) and c) respectively. The magnitude response illustrated in Figure 4.3 b) indicates that the filter will only output frequencies shown in the spectrum with a gain of 1 (subject to ideal transition bands).

Frequencies with a gain of 0 are to be attenuated by a certain dB level. The log magnitude response in Figure 4.3 c) correspondingly shows the attenuation dB level of each frequency in the spectrum. Figure 4.3 d) presents the linear phase response of the filter that depicts the phase or angle of the frequency response.

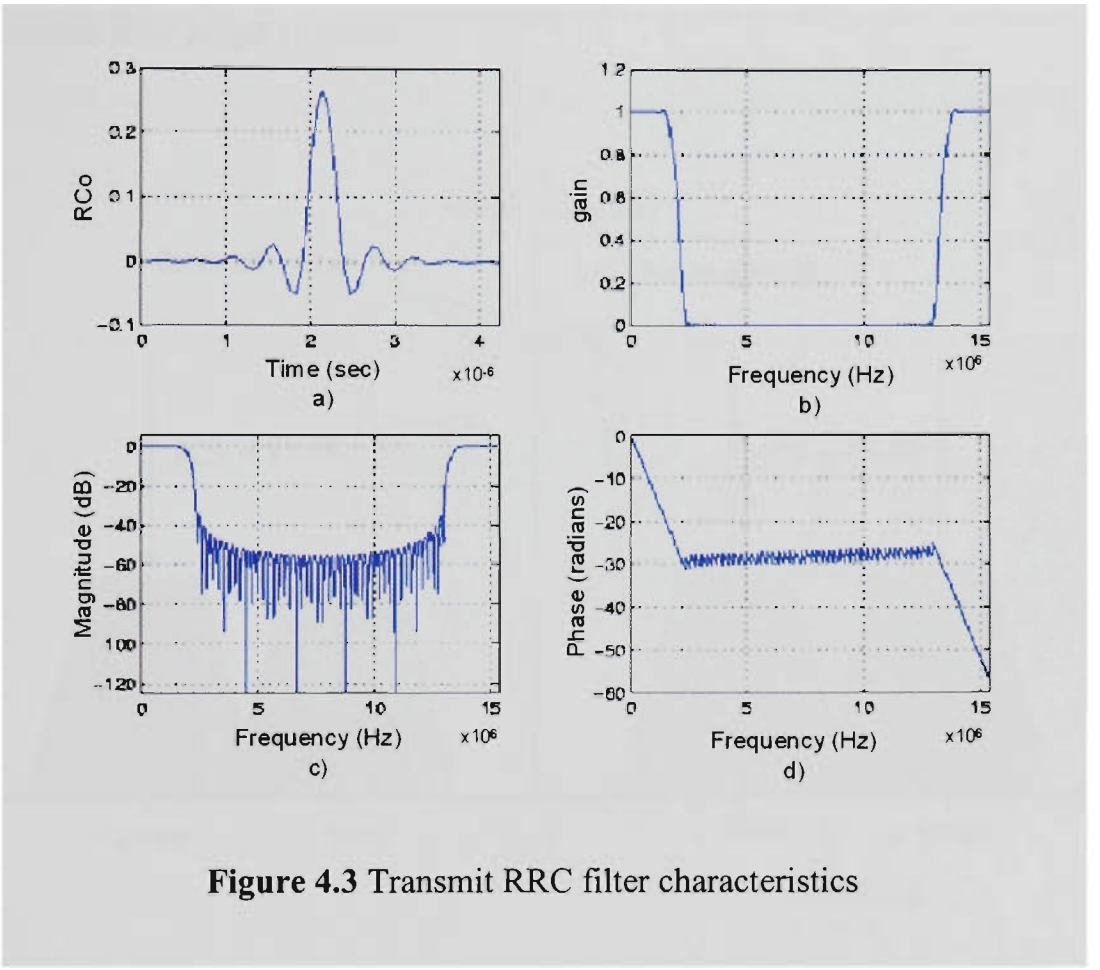


Figure 4.3 Transmit RRC filter characteristics

4.2.2 Receiver RRC Filter Considerations

The investigation in section 4.2 has concluded that an interpolation factor of 4 for the transmitter filter is suitable with respect to complexity, specifications as well as trade offs that exist with the reconstruction filter in the BS transmitter. Therefore, the receiver filter will employ the same sampling frequency of 15.36 MHz with a decimation stage down sampling the data by a factor of 4. The 3GPP specifications require the receiver filter to have a minimum ACS of 33 dB in the ± 5 MHz and ± 10 MHz adjacent

channels [25] and this is graphically demonstrated in Figure 4.4. The figure also shows the bandwidth of the filter along with the cut-off frequency and the attenuation level, ACS, on the assigned adjacent channels. The reconfigurable filter will employ variable ACS where the maximum filter length is 65 (identical as the transmit RRC filter) and the minimum filter length is 5.

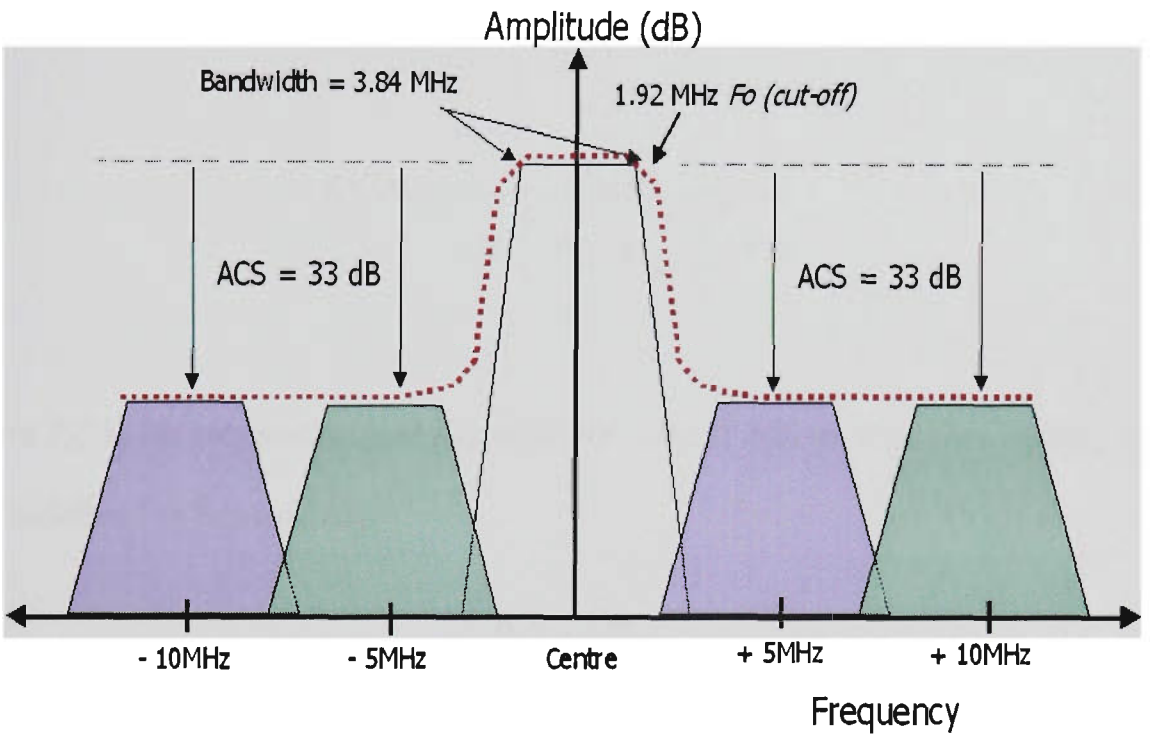


Figure 4.4 Receiver RRC Filter 3GPP Specifications with minimum ACS

4.3 System Design

The reconfigurable RRC filter is described in this section. The architecture consists of a number of components to enable variable ACS. Firstly, the algorithm enabling the filter to exploit variable ACS is formulated and the corresponding system architecture is introduced. The subsequent sections describe the operation of each component in the reconfigurable architecture.

4.3.1 Algorithm Formulation

The algorithm for reconfigurable receiver filtering is formulated from the Eb/No model given in equation (3.2). Considering intra-cell interference is always present as orthogonality may not be achievable in practice and the received signal powers have been propagated, the Eb/No can be defined as [62]:

$$Eb/No = \frac{P_{rx}^{\ i} pg}{(M-1)P_{rx}^{\ i} + \frac{I_{adj}^{\ i}}{ACP^{i}} + \eta} \tag{4.3}$$

where $P_{rx}^{\ i}$ is the received desired signal power at the i^{th} MS in the cell of interest (COI) and is defined as follows [62]:

$$P_{rx}^{\ i} = \frac{P_{rec}^{\ i}}{\kappa^{i}} \tag{4.4}$$

$P_{rx}^{\ i}$ is determined by the code power of the BS divided by the path loss of the i^{th} MS within one time slot in the COI. The code power is determined by the power control model specified in section (3.2.1.1).

The key to the reconfigurable algorithm is specifying a variable adjacent channel protection (ACP) as the ACS is a function of ACP and the ACLR of the transmitter RRC filter. Solving equation (4.3) in terms of ACP yields:

$$ACP^i = \frac{I_{adj}{}^i}{\mathrm{P}_{rx}{}^i\left(\frac{pg}{Eb/No}+1-M\right)-\eta} \tag{4.5}$$

where ACP^i is the ACP factor required to satisfy the required *Eb/No* at the i^{th} MS in the COI. Equation (4.5) must be expressed in terms of in-band and out-of-band signal powers to solve for the required ACP factor. This is expressed in the following equation:

$$ACP^i = \frac{I_{adj}{}^i}{P_{rx}{}^i\left(1+\frac{pg}{Eb/No}\right)-P_{rx}{}^iM-\eta} \tag{4.6}$$

where $I_{adj}{}^i$ is the *out-of-band* signal, $P_{rx}{}^i$ is the *desired* signal and $P_{rx}{}^iM$ is the *in-band* signal. The processing gain and thermal noise are known (static) as well as the target Eb/No is set. All three signals are enclosed in the input signal to the receiver RRC filter. To distinguish the signals the following processing is required:

- *In-band* signal power– This is purely the output of the filter containing the *desired* signal power as well as intra-cell interference power from other MS's served by the BS within the same timeslot.

- *Out-of-band* signal power– This signal is the ACI the receiver RRC filter has mitigated. It can be obtained by using a high-pass filter (HPF) corresponding to an inverse of the receiver RRC filters' frequency response. This method is inefficient, as the processing complexity will be doubled. In digital signal processing, a HPF equivalent filter can be a subtraction operation where the

output of the LPF (presuming a LPF) is subtracted from an input stored at its center delay unit. This is efficient to implement in hardware and is significantly less costly than a complex HPF.

- *Desired* signal power- This signal can only be obtained once the *in-band* signal power is de-spread with the corresponding user orthogonal variable spreading factor (OVSF) code.

It is clear that based on the above descriptions, the reconfigurable filter will be based on a feed back structure as some receiver processing is required to obtain the necessary signals for ACP calculation. Once the ACP is obtained, the corresponding ACS can be found. The relationships have been investigated in [79] and it is found that:

$$ACS^i = \frac{1}{\frac{1}{ACP^i} - \frac{1}{ACLR}} \tag{4.7}$$

where ACS^i is the stop band attenuation level for the receiver filter required to give and overall ACP performance in the ± 5 MHz and ± 10 MHz adjacent channels. Based on the findings in this section, the reconfigurable receiver RRC filter architecture is presented in Figure 4.5. The architecture consists of a *FIR filter structure*, two *decimation* units that will down sample the in-band and out-of-band data by a factor of 4 and a *subtraction* operation that obtains the out-of-band signal. Clearly varying amplitudes of each signal is required before they are processed by the *control unit* where the most efficient ACS is calculated. This is achieved by the *signal power measurement* components in the architecture where the signals will be averaged over a

certain length of time. The *shaver* signal switches taps on/off in the FIR structure corresponding to the required length

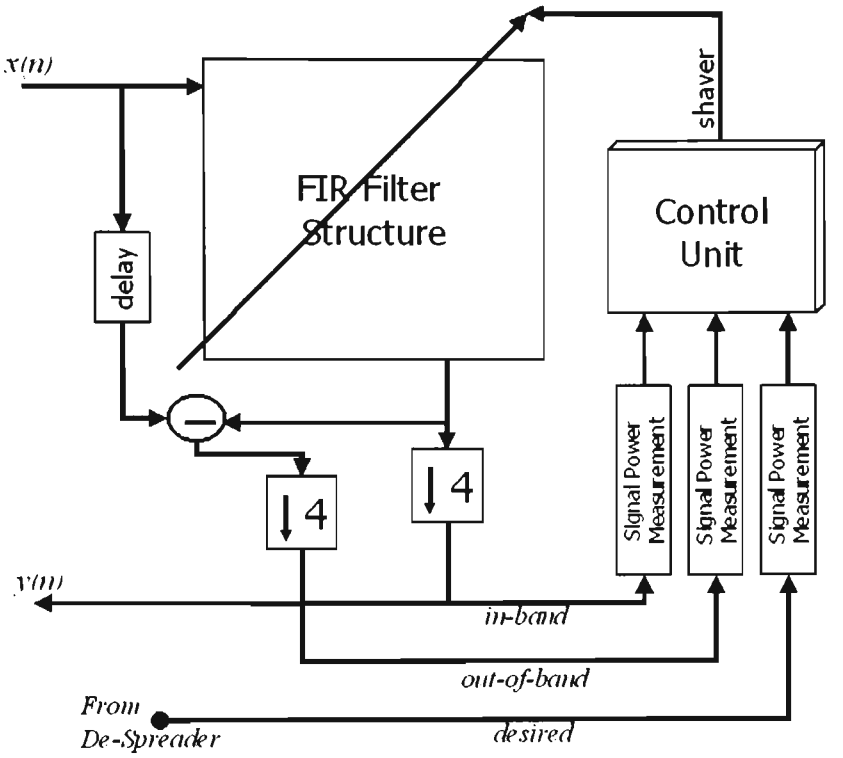


Figure 4.5 Reconfigurable receiver RRC filter architectural block diagram

4.3.2 FIR Low Pass Filter Structure

The FIR structure is based on the linear phase technique described in Chapter 2, section (2.4.2). This structure is efficient as it takes advantage of symmetrical coefficients and uses half the required multiplications and additions. The structure is customised with switches that can switch off or switch on coefficients with their corresponding registers, depending on the required ACS requirements. Figure 4.6 presents the FIR structure.

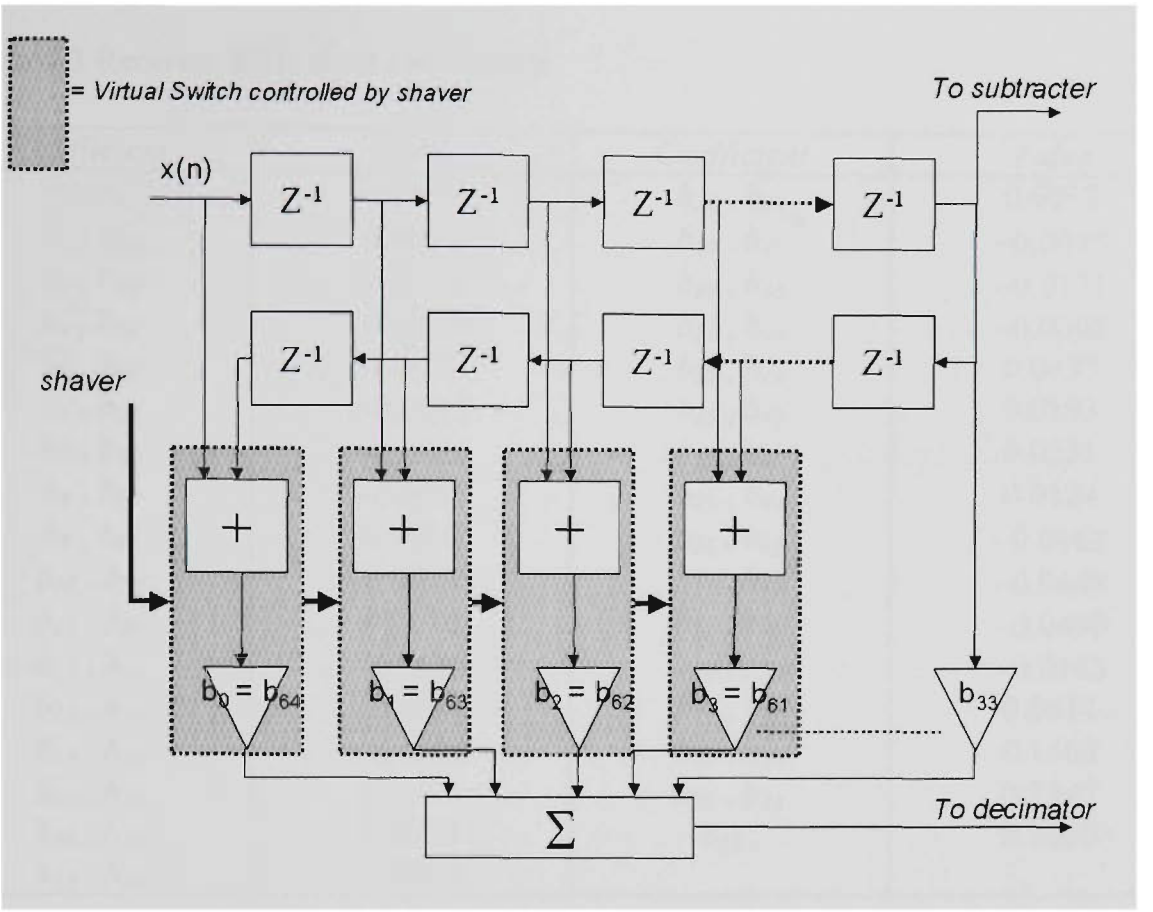


Figure 4.6 Linear phase FIR filter structure customised for variable ACS

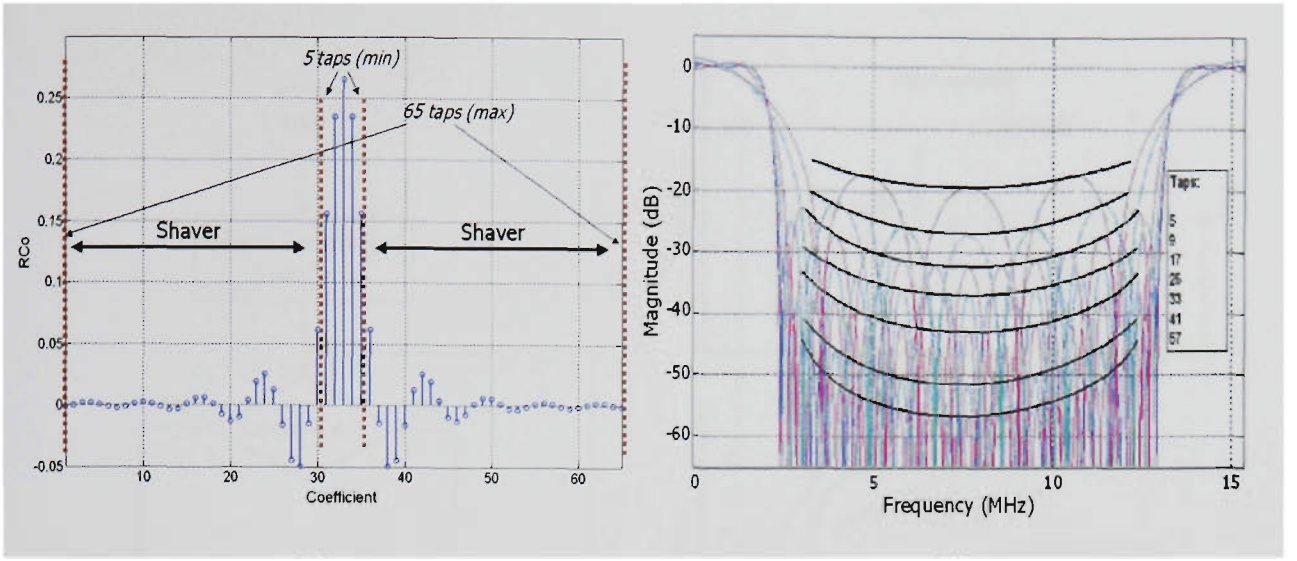
The above structure exploits a filter length of 65 (filter order of 64) where b_n corresponds to a coefficient in the impulse response of the filter. The maximum filter matches the simulated transmitter filter characteristics. The shaded rectangles depict the switches that determine if there should be a multiplication (depicted by a triangle in the structure) with the delayed input data and a coefficient, which is all controlled by the *shaver* signal from the control unit. There are no switches on the middle tap, b_{33}, as well as $b_{31}=b_{35}$, $b_{32}=b_{34}$ as five taps is the minimum filter length determined by the simulated ISI analysis in Chapter 3. The coefficients are listed in Table 4.3.

Table 4.3 Receiver RRC filter coefficients

Coefficient	*Value*	*Coefficient*	*Value*
b_1 , b_{65}	–0.0012	b_{18} , b_{48}	0.0012
b_2 , b_{64}	0.0002	b_{19} , b_{47}	–0.0075
b_3 , b_{63}	0.0016	b_{20} , b_{46}	–0.0131
b_4 , b_{62}	0.0018	b_{21} , b_{45}	–0.0095
b_5 , b_{61}	0.0005	b_{22} , b_{44}	0.0037
b_6 , b_{60}	–0.0013	b_{23} , b_{43}	0.0193
b_7 , b_{59}	–0.0021	b_{24} , b_{42}	0.0251
b_8 , b_{58}	–0.0011	b_{25} , b_{41}	0.0124
b_9 , b_{57}	0.0010	b_{26} , b_{40}	–0.0163
b_{10} , b_{56}	0.0023	b_{27} , b_{39}	–0.0448
b_{11} , b_{55}	0.0014	b_{28} , b_{38}	–0.0499
b_{12} , b_{54}	–0.0012	b_{29} , b_{37}	–0.0143
b_{13} , b_{53}	–0.0034	b_{30} , b_{36}	0.0617
b_{14} , b_{52}	–0.0026	b_{31} , b_{35}	0.1563
b_{15} , b_{51}	0.0014	b_{32} , b_{34}	0.2347
b_{16} , b_{50}	0.0057	b_{33} ,	0.2650
b_{17} , b_{49}	0.0064		

To acquire an understanding of how shaving or switching coefficient multiplications (taps) on or off in the structure affects the ACS, consider Figure 4.7. The figure illustrates the impulse response and the frequency response of the filter with variable ACS.

This figure clearly demonstrates that as the *shaver* signal switches coefficients off from the ends of the impulse response (as FIR coefficients are symmetrical); the ACS in the frequency response accordingly decreases. The power consumption will also decrease proportionally when lower ACS is required as the multipliers are a key driver contributing to power consumption in FIR filters.



a) b)

Figure 4.7 The effect on the frequency response of the receiver RRC filter when *shaver* switches on or off coefficients (taps) in the impulse response *a) Impulse Response, b) Frequency Response*

4.3.3 Decimation

The decimation process is a fundamental operation in multi-rate signal processing. It proficiently allows the sampling frequency of the system to reduce without unwanted effects on the signal such as quantisation noise.

The decimation stage in the architecture purely down samples the received symbols by the same factor used in the interpolation stage in the transmitter. The decimation algorithm is described with a flow chart in Figure 4.8 a) along with a timing example in Figure 4.8 b). Findings in section 4.2.2 yielded a decimation factor of 4 for the receiver RRC filter to down sample the data rate to 3.84 MHz. The decimation stage only allows every fourth sample of its input to pass through to the output, therefore skipping every three samples of its input.

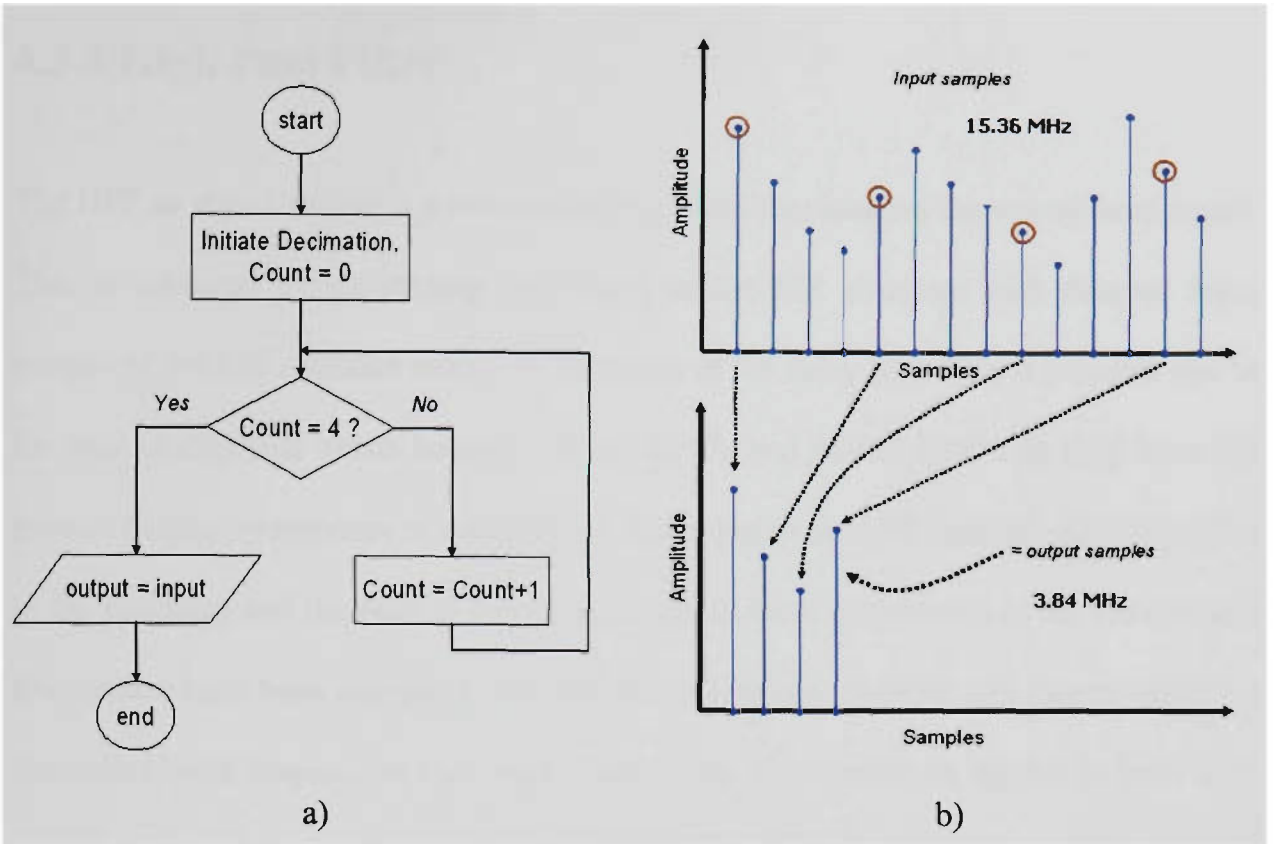


Figure 4.8 Decimation operations down sampling data by a factor of four *a) Flow chart, b) Timing diagram*

In the architecture, decimation occurs after filtering as the rake receiver in the mobile receiver, depending on the design, may require the signal at an over sampled rate rather than the critical sampled rate of 3.84 MHz. If the data is required at the critical sampled rate, the filter structure can be optimised by employing decimation before filtering. This method can reduce the number of multiplications thus reducing power dissipation as the decimation occurs before filtering [34]. The structure is further explained in the future work section of the conclusion chapter.

4.3.4 High Pass Filter

The HPF as stated earlier is a subtraction operation that isolates the out-of-band signal. This is achieved by subtracting the output of the FIR structure with delayed input sample of the FIR structure stored in the centre of the delay line. This is possible due to the relationship that exists between digital LPF's and digital HPF's as they have the inverse frequency response to one another. The input to the LPF contains all frequencies in the spectrum and the output only contains the in-band frequencies as the out-of-band frequencies have been mitigated. The difference between the input and output would be the out-of-band frequencies that were filtered out. This technique applies to both time and frequency domain. Figure 4.9 presents the block diagram of the system with an example in the frequency domain.

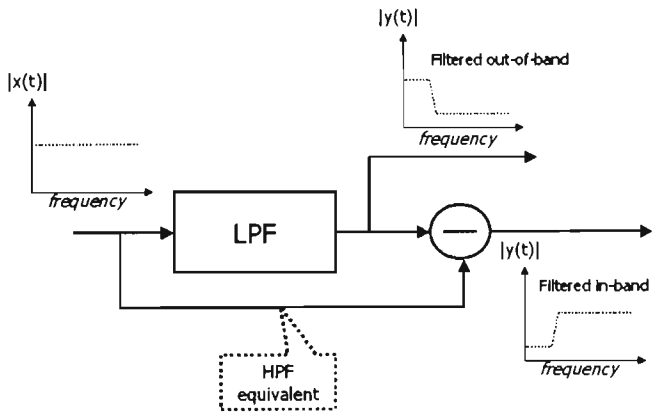


Figure 4.9 Equivalent HPF with inverse LPF frequency response using subtraction method

As FIR filters have a delay line, it is important to select the input delay of the LPF that falls exactly in the middle of the impulse response, otherwise the cancellation will not function correctly and the HPF will produce an erroneous response. For the receiver

RRC filter, the input sample that is subtracted from the output sample to obtain the out-of-band noise is delayed by 32 samples, as the maximum filter length is 65. Figure 4.10 presents the amended block diagram of the LPF and HPF relationship.

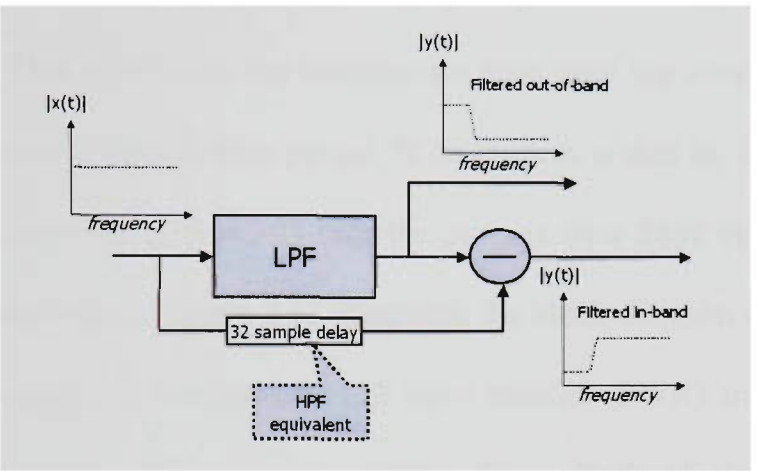


Figure 4.10 Equivalent HPF with inverse LPF frequency response using subtraction method and incorporating delay line matching the middle of the impulse response of the receiver RRC filter.

Figure 4.11 presents a frequency response of the LPF and the equivalent HPF with a white Gaussian noise input signal. It is clear that the high pass output response is the exact complement of the low pass response.

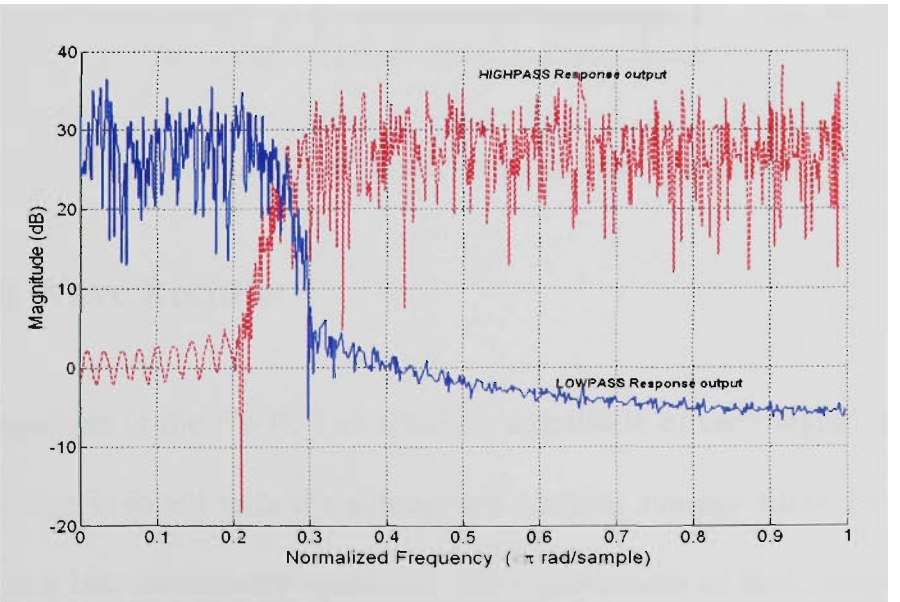


Figure 4.11 Low pass and high pass frequency response using white Gaussian noise input.

4.3.5 Signal Power Measurement

Before the control unit processes the three signals (in-band, out-of-band and desired), they must be processed to obtain clearly varying amplitudes in order to calculate the new filter length. This is because the architecture must take the average amplitude of each input signal over a certain time period. If the system scales its filter length every frame (10 milliseconds (ms)), it would take the average over 2650 samples for the in-band and out-of-band signal. Figure 4.12 illustrates the block diagram of a signal power measurement component. It consists of a full wave rectifier (FWR) and a low complex infinite-impulse response (IIR) running average filter. Each of the components is discussed in the following subsections.

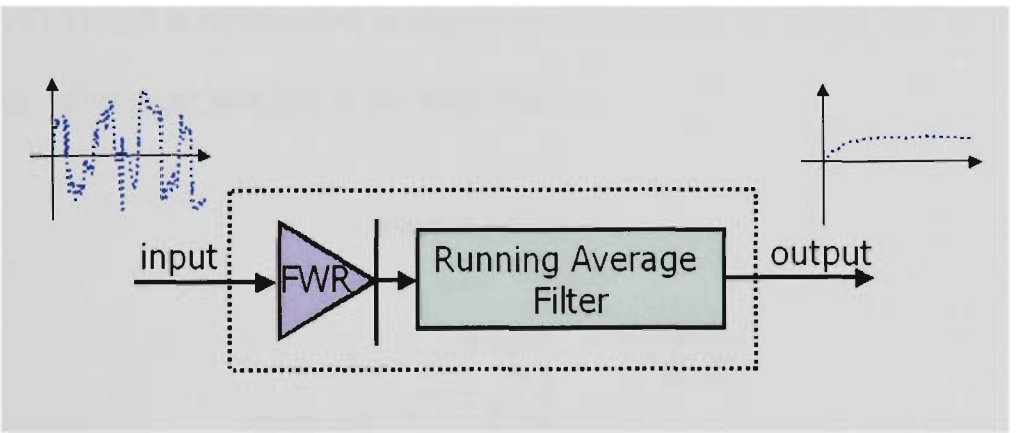


Figure 4.12 Signal power measurement component

4.3.5.1 Full Wave Rectifier

The first component is the FWR. The absolute amplitude of each signal must be taken before an average is found with the subsequent running average filter. In digital signal processing it is a low complexity operation. The complement of each sample is found if the magnitude is negative. Figure 4.13 presents a flow chart of the operation.

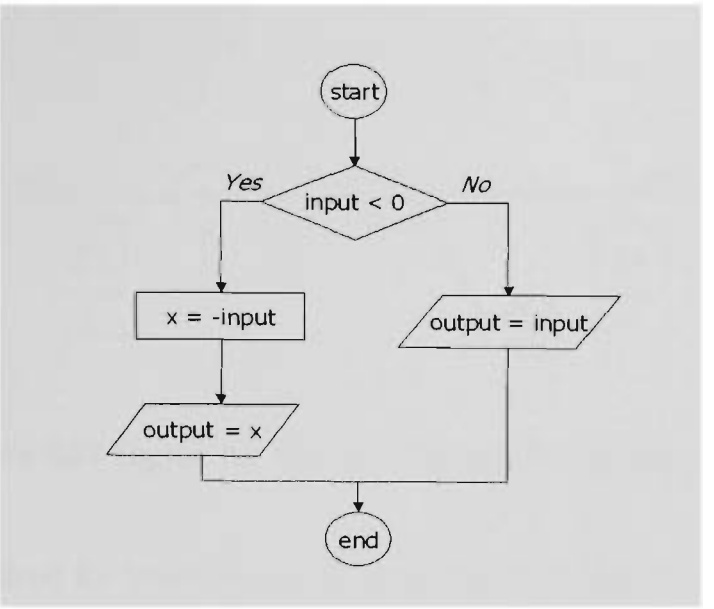


Figure 4.13 Digital full wave rectifier operation flow chart

In hardware, the FWF is a conditional complement operation. Figure 4.14 depicts an example demonstrating the operational steps for a negative input with a word length of five bits. The word is represented in signed two's complement where first bit is the sign bit and the subsequent four bits is the magnitude.

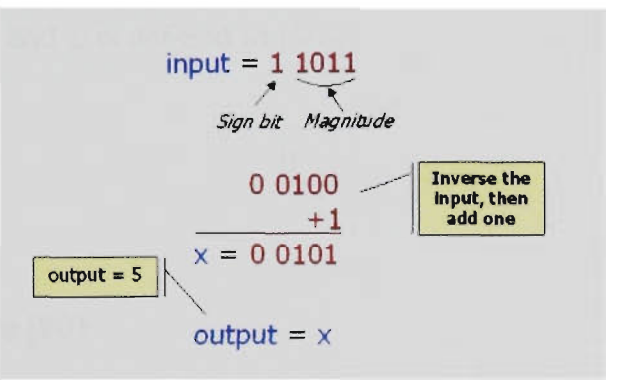


Figure 4.14 Complement operation in digital hardware with a signed two's complement word

4.3.5.2 Running Average Filter

The running average filter is a first order IIR digital LPF. It computes a running average on a vector of sampled data using a delayed input sample and the previous output sample for each input sample. The system block diagram is presented in Figure 4.15.

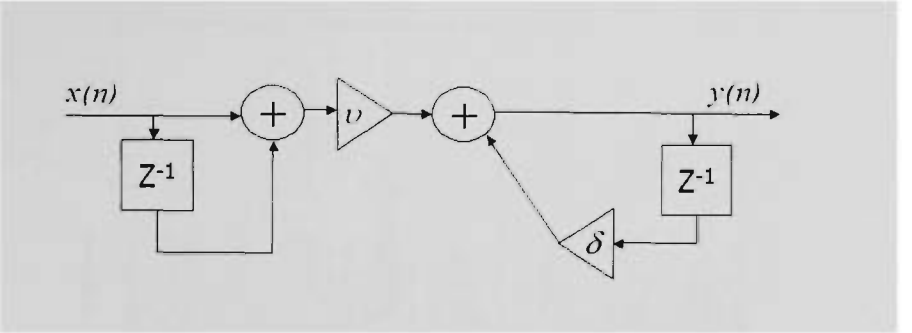


Figure 4.15 Digital IIR running average LPF system diagram

The hardware required for implementation is not costly as only two multipliers and two addition units are required. A delay unit is represented by z^{-1}, and the difference equation *y(n)* is defined as follows [80]:

$$y(n) = [(x(n) + x(n-1))\upsilon] + [y(n-1)\delta] \tag{4.8}$$

where *x(n)* is the current input sample, *x(n–1)* is a delayed input sample, *y(n–1)* is a delayed output sample, and υ is defined as [80]:

$$\upsilon = \frac{(1-\delta)}{2} \tag{4.9}$$

δ is described as follows [80]:

$$\delta = \frac{\cos\theta c}{1+\sin\theta c} \tag{4.10}$$

where θc is a normalised frequency of 0.002π [80]. Figure 4.16 presents pre and post filtering of white Gaussian noise (after FWR processing) over 2650 samples. The final output sample of the filtered data is the average amplitude of the entire stream of input samples, which is fed to the control unit.

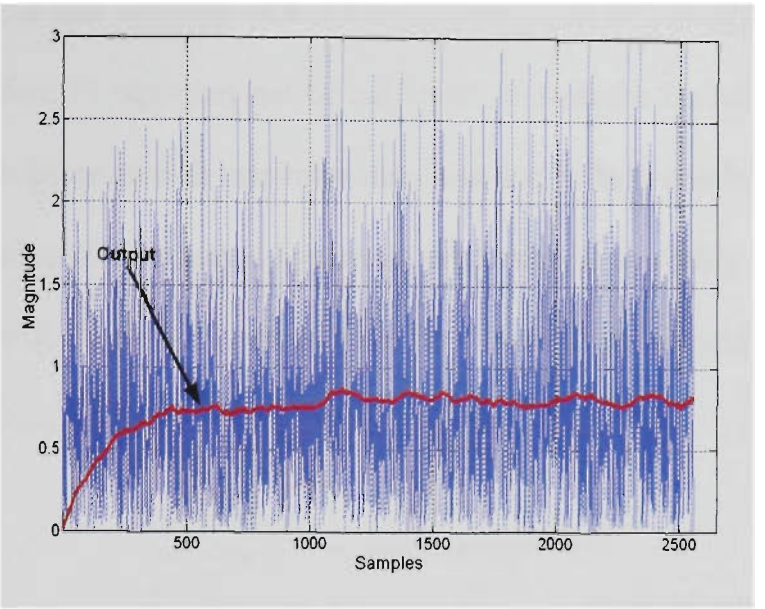


Figure 4.16 Input versus output of running average filter with 2650 samples

4.3.6 Control Unit

The control unit is the intelligence behind the architecture. It calculates the required filter length based on the three signals powers and adjusts the filter length by shaving off or adding taps to the ends of the impulse response, therefore, lowering or raising the ACS dB level that achieves an overall ACP requirement.

The ACS purely is not the only factor to determine the new lengths of the filter. If it were, there would be chances of immense data loss. As the architecture employs a feedback approach, the new filter length applies to the next lot of samples, not the current. An example of data loss could be as follows: The current filter length is 33 and the new calculated filter length is 11. The architecture scales the filter to the new length and applies it to the frame of samples. As it is a TDD system with a near far problem, an adjacent MS may switch on close to the MS of interest the same time it is receiving the

frame of samples. If this adjacent MS is transmitting to its BS, it will result in a major signal jam. Therefore 11 taps may not be sufficient to meet the Eb/No. The control unit employs hysteresis protection to minimise data loss and to help combat such a scenario. Data loss is still inevitable whether hysteresis protection is available or not but it will, on average, reduce it. Figure 4.17 presents the flow chart of the control unit operation.

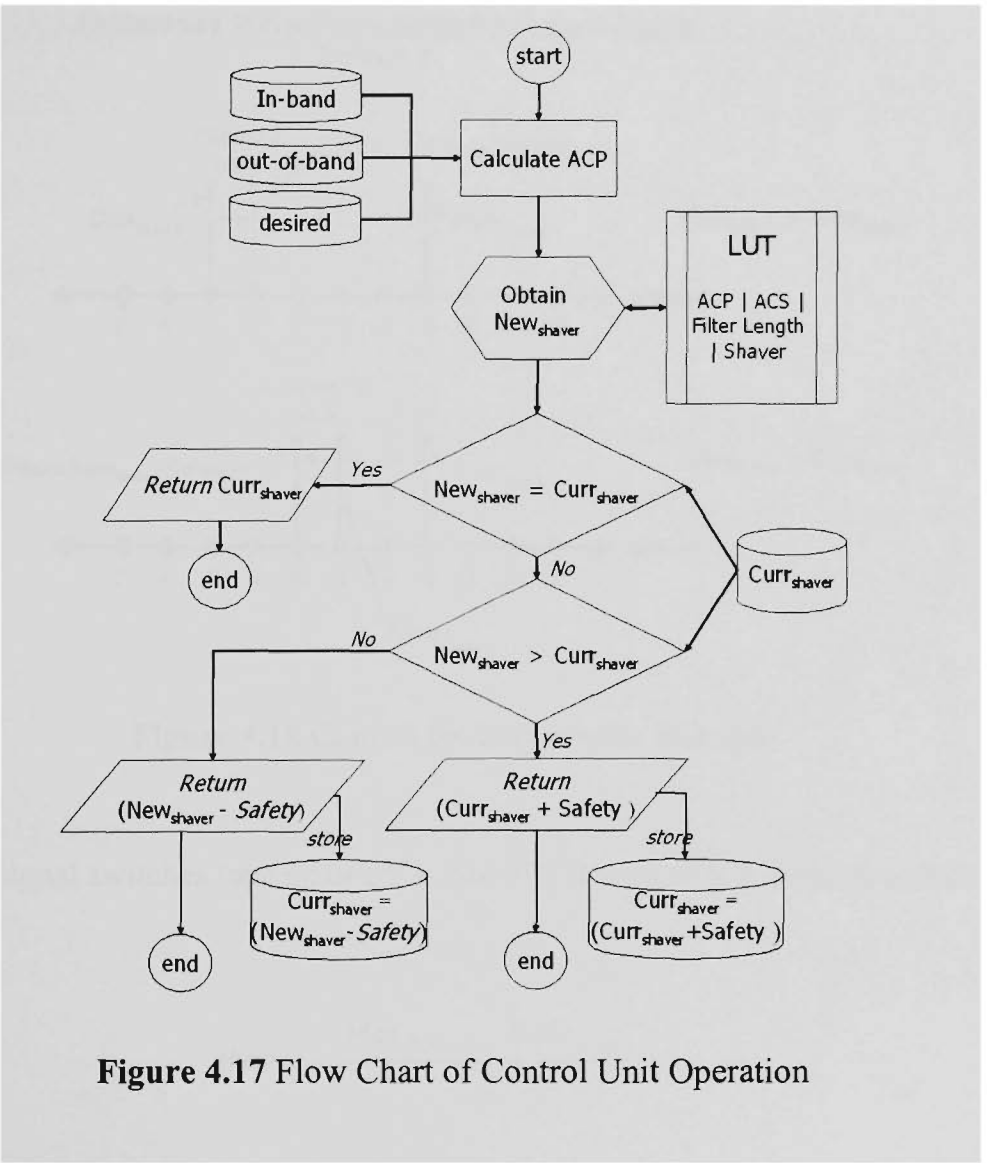


Figure 4.17 Flow Chart of Control Unit Operation

The first operation required is to calculate the ACP factor. This is achieved by solving equation (4.6). Once the ACP is found, the control unit performs hysteresis protection. The fundamental scheme is if the filter length requires decreasing; it decreases slowly (*Safety**2 taps at a time) instead of instantaneously to the new filter length. If the filter length needs to increase, it increases instantaneously to the new filter length in addition

to (*Safety**2) taps. This ensures the filter has ample ACS to attenuate the out-of-band signal in the next lot of samples as the ACI power maybe to some extent higher. Figure 4.18 illustrates an example of the hysteresis protection in the control unit where a decrease and an increase in the filter length are required.

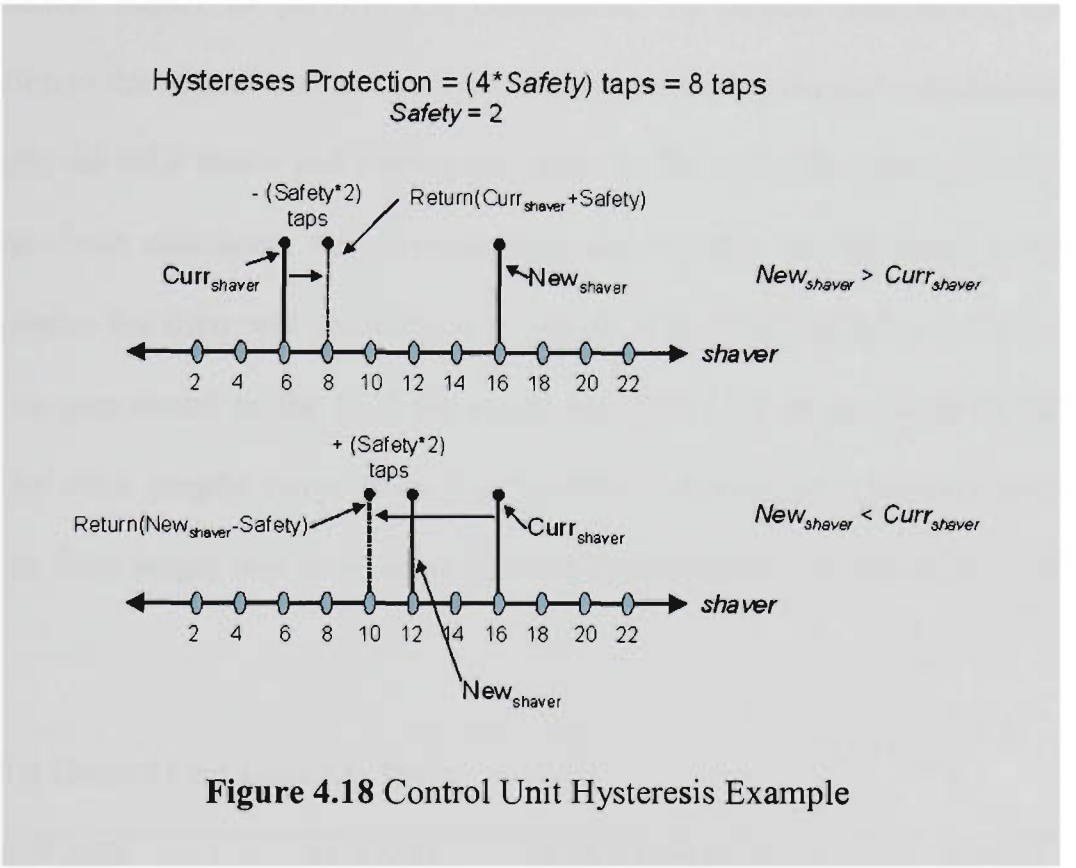


Figure 4.18 Control Unit Hysteresis Example

The *shaver* signal switches taps on or off in the FIR structure. It is defined as follows:

$$shaver = \frac{Max_{flength} - New_{flength}}{2} \tag{4.11}$$

where $Max_{flength}$ is the maximum filter length available and $New_{flength}$ is the new calculated filter length. For example, if $New_{flength}$ is 19 and $Max_{flength}$ is 65, shaver is set to 23. Therefore, 23 taps from each end of the impulse response will be switched off and the other will be switched on. New_{shaver} is defined as the newly calculated *shaver* value that will scale the filter structure whereas $Curr_{shaver}$ is the current shaver value.

The look up table (LUT) employed in the control unit flow chart is an efficient technique to obtain data as an alternative to mathematical calculations. The output of the control unit is the *shaver* signal which can only be obtained by corresponding it to the ACS of the filter. This can only be implemented using a LUT as there is no mathematical model to perform the conversion. To reduce complexity, the ACS calculation in the control unit can be bypassed by performing manual calculations of the ACS from the ACP factor and storing the values in the LUT. Therefore, once the ACP factor has been calculated, the corresponding *shaver* value can be found in the LUT each instance the filter will reconfigure its length. The other variables; ACS and filter length are also stored in the LUT for future use. The LUT is presented in Table 4.4 where the filter lengths range from 5 to 65 with a margin of 4 between them. The minimum filter length was determined by inter-symbol interference analysis in Chapter 3.

Table 4.4 Control Unit Look-Up Table

ACP (dB)	*ACS (dB)*	*Filter Length (taps)*	*Shaver*
$44.8 < \& \leq 44.9$	60	65	0
$44.7 < \& \leq 44.8$	58	61	2
$44.5 < \& \leq 44.7$	56	57	4
$43.8 < \& \leq 44.5$	54	53	6
$43.6 < \& \leq 43.8$	50	49	8
$43.2 < \& \leq 43.6$	49	45	10
$42.0 < \& \leq 43.2$	48	41	12
$38.8 < \& \leq 42$	45	37	14
$36.4 < \& \leq 38.8$	40	33	16
$34.6 < \& \leq 36.4$	37	29	18
$29.8 < \& \leq 34.6$	35	25	20
$27 < \& \leq 29.8$	30	21	22
$25 < \& \leq 27$	27	17	24
$20 < \& \leq 25$	25	13	26
$14 < \& \leq 20$	20	9	28
≤ 14	14	5	30

4.4 Conclusions

This chapter presented the design of the reconfigurable RRC filter inherent to the UTRA-TDD mobile terminal receiver. As ACI is a concerning topic due to the addition of same entity interference (MS→MS), the design of a receiver filter that caters to the specifications (33 dB of ACS; minimum) will be complex and inefficient.

The intention of the reconfigurable filter is to provide a resolution to the cost issues associated with the TDD cellular system; primarily to increase the battery life of the mobile terminal by minimising power consumption. The architecture in real-time observes in-band and out-of-band powers, and by employing intelligent functionality, calculates the required ACS and regulates the filter length accordingly. This reduces the power consumption as only the required multiplications and additions in the architecture will be used to process the convolution between input samples and coefficients.

A sampling frequency of 15.36 MHz was chosen before down sampling the data by decimation factor of 4 was considered. This was primarily due to transmitter filter considerations with respect to the complexity tradeoffs and concluded that an interpolation factor of 4 was sufficient. The formulation of the algorithm for reconfigurable filtering concluded that three signals are required to determine the appropriate ACS that gives overall ACP performance. The formulation led to the proposal of the system architecture. It consists of a number of components; FIR structure with tap switches managed by the control unit, a low complex HPF equivalent subtraction operation to obtain the ACI signal as well as signal power measurement

components to provide clearly varying amplitudes of each three input signals to the control unit. The control unit calculates the appropriate ACP and by employing a LUT as well as hysteresis protection it determines how many taps need be switched off or turned on to provide the required ACS.

Statistical analysis of the reconfigurable filter is provided in Chapter 5 of this thesis along with an evaluation of the implementation's performance in terms of power consumption and speed.

Chapter 5

Reconfigurable Filter Analysis

5.1 Introduction

In this chapter, the reconfigurable receiver root raised cosine (RRC) filter design presented in Chapter 4 is analysed statistically. The analysis is performed in a simulation environment considering universal mobile telephone service (UMTS) terrestrial radio access (UTRA) – time division duplex (TDD) properties. The purpose of this investigation is to evaluate the efficiency of the reconfigurable filter in terms of power dissipation in the UTRA-TDD mobile handset.

This chapter also describes the implementation of the reconfigurable digital filter. The implementation considers a hardware and software partitioned approach. It consists of an application specific integrated circuit (ASIC) for power and performance critical components in the architecture and digital signal processor (DSP) core for components requiring flexibility. A performance analysis is carried out in terms of speed and power

consumption as well as providing a statistical analysis of power consumption when the filter is operated in an UTRA-TDD environment.

This chapter is structured as follows: a statistical analysis of the reconfigurable filter in a simulation environment is achieved in section 5.2. The analysis evaluates the efficiency of the design when applied to the UTRA-TDD system. Both static and dynamic analysis is performed. The implementation of the reconfigurable filter is presented in section 5.3 along with a performance analysis and conclusions are presented in section 5.4.

5.2 Statistical Analysis

In this section, a statistical analysis of the reconfigurable filter is presented in a simulation environment. The statistical analysis is considered to evaluate the efficiency of the reconfigurable filter in an UTRA-TDD indoor environment.

Two categories of analysis are performed. Firstly, a static analysis is performed in section 5.4.2 on adjacent channel protection (ACP) factors and adjacent channel selectivity (ACS) of the filter as well as an analysis of the corresponding filter lengths. Secondly, a dynamic analysis in section 5.4.3 is performed to evaluate its efficiency with simulated Rayleigh channel data. Simulated Rayleigh channel data has its limitations due to the wideband nature of the transmissions; therefore the results would vary if measured Rayleigh channel data was used in the simulations.

This analysis looks at the probability of ACP factors and filter lengths as well as analysing the bit-energy to interference ratio (Eb/No) of the system.

5.2.1 Simulation Platform

The simulation platform and cell topology for the static analysis are identical to that in Chapter 3, section 3.2.2.2 for a multiple interfering cell scenario. The corresponding simulation parameters are identical as in table 3.1 in Chapter 3. The reconfigurable filter will only be analysed in a multiple interfering cell scenario as this provides a better approximation to a practical, real life cellular system compared to a single interfering cell scenario. The dynamic analysis employs the same cell topology as the static analysis but the simulation parameters differ and are presented in table 5.1.

Table 5.1 Dynamic analysis simulation parameters

Parameter	*Value*
Bit Rate	32 Kilo bits per second (Kbps)
Required Eb/No (decibels (dB))	3.5
Thermal Noise (dB milli watts (dBm)	−102.85
Cell Radius (meters (m))	100
# of Interfering Adjacent Cells	7
# of mobiles in each Interfering Adjacent Cell	8
# of Intra-cell Interfering Mobiles	7
Sampling Frequency (F_s) (Mega hertz (MHz))	15.36
Channel Type	Simulated Rayleigh Flat Fading
Mobile Velocity (meters per second)	0.5, 2, 4 and 8
Carrier Frequency (F_c) (MHz)	1912.5
OVSF Code Lengths	16
Control Unit *Hysteresis* protection	8 taps (*Safety* = 2)
TDD Frame length (F_l)	10 milliseconds (ms)
Frequency of Reconfiguration (F_r)	$1 / F_l$
Time Slot Length (T_l)	6.667e-4 seconds

In this analysis, there are 56 adjacent channel mobile station (MS) interferers, 7 adjacent base station (BS) interferers and 7 intra-cell interferers each with a Rayleigh flat fading

channel. Intra-cell interference in theory should not be present due to the orthogonal nature of orthogonal variable spreading factor (OVSF) codes. In reality, this cannot be assumed, therefore a twiddle factor is used set to the worst case, and therefore, intra-cell interference is present. The control unit F_r is set at 10 ms which results in a new filter length every TDD frame. The control unit hysteresis protection is set to 8 taps; therefore when there is the need to increase the filter length (in-band signal power is heading into a trough or/and out-of-band signal power is increasing), an additional 4 taps will be added for protection. When the filter length requires decreasing, it will decrease 4 taps less rather than directly to the new calculated filter length.

5.2.2 Static Environment

All MS's in the COI and adjacent cell are distributed uniformly. ACP factors and ACS levels are calculated at the MS within the COI using equation (4.6) and (4.7) respectively. Monte Carlo simulations are used to calculate the probability density functions (pdfs) and cumulative distribution functions (cdfs) of ACP factors and ACS powers. Once ACS powers are found, the corresponding filter length is established using the look up table (LUT) presented in Table 4.4 in Chapter 4.

5.2.2.1 Adjacent Channel Protection Factor Analysis

Figure 5.1 presents cdfs and pdfs of ACP factor powers with various synchronisation factors, α and lognormal shadowing of 12 dB. The corresponding recorded results are presented in Table 5.2. The cdfs and pdfs in the figure interpret the same findings and clearly illustrates that there are various probabilities of ACP factors. This establishes

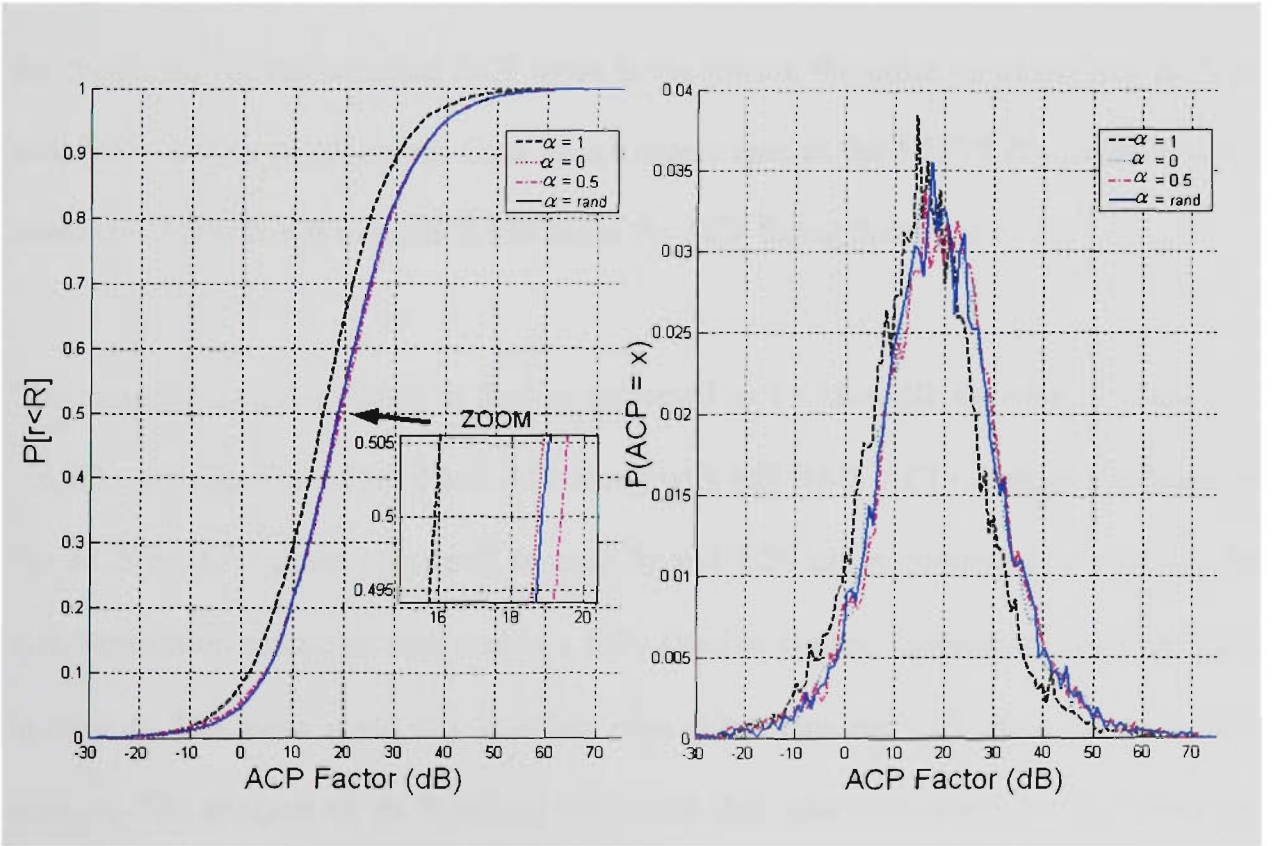
that the receiver filter with variable ACS will be efficient as there are minor probabilities of high ACP factors inherent to the UTRA-TDD. The analysis considers four cases as there are four distinct α values and are listed as follows:

e) ($\alpha = 1$): The results presented in this case only exploit MS→MS ACI

f) ($\alpha = 0$): This case is the opposite of a) as it only considers BS→MS ACI

g) ($\alpha = 0.5$): The results in this case allow 50 percent from each interfering entity, therefore considering BS→MS and MS→MS ACI

h) (α = uniform random): This case considers that fixed synchronisation cannot be assumed in a fully flexible system, therefore synchronisation factors are random (0 to 1)



a) b)

Figure 5.1 Statistical analysis ACP factors
a) cdf, b) pdf

Table 5.2 Statistical analysis results of ACP factors

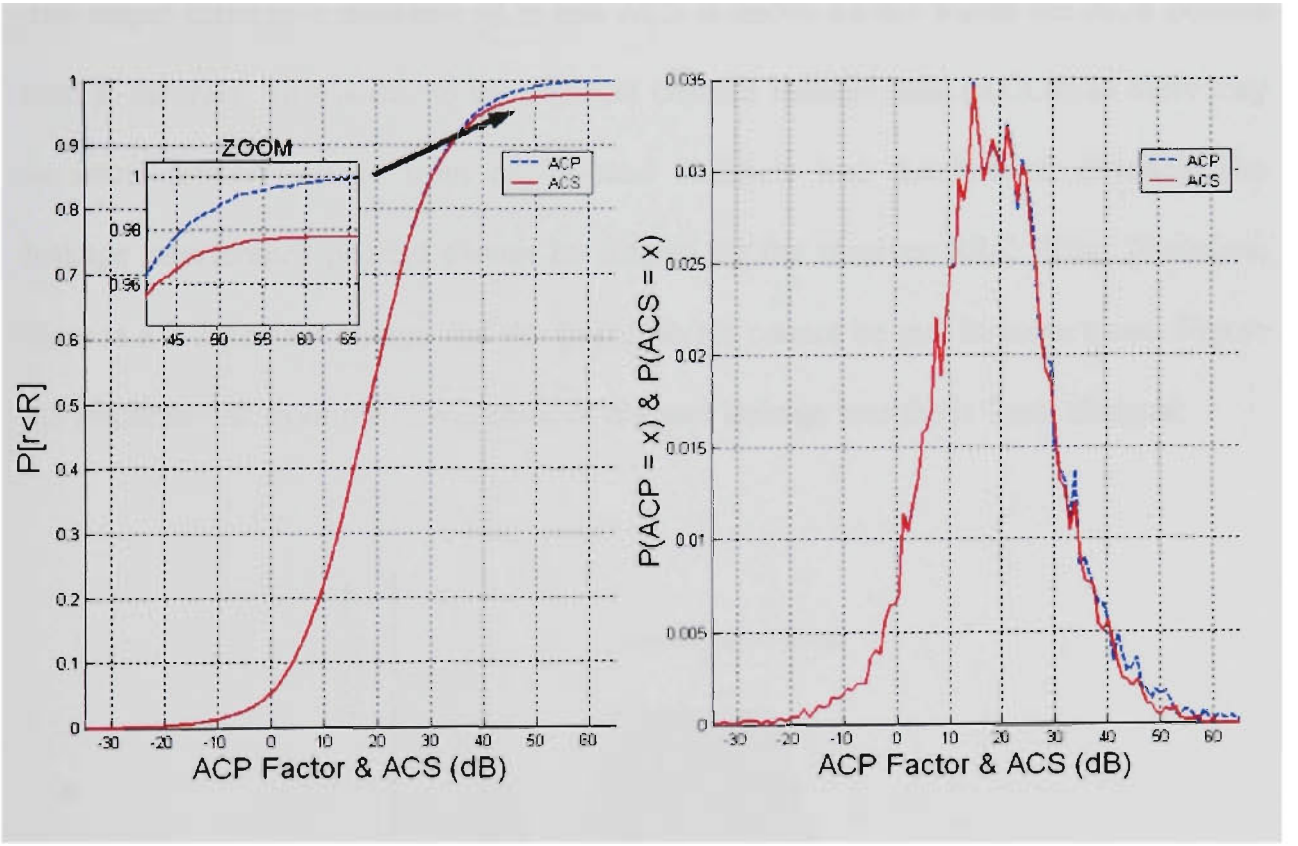
Synchronisation Factor, α	*E (ACP)* (dB)	*STD (ACP)* (dB)
1	15.8514	11.9468
0	19.1887	12.2429
0.5	19.3864	12.6574
Uniform Random 0 to 1	19.2617	12.3802

Varying the synchronisation factor yields various means of ACP factors. The mean tends to increase by a maximum of 3.535 dB and the standard deviations of ACP factors increases by a maximum of 0.7106 dB when α is varied. The findings yield that synchronisation plays a key role in the amount of ACP factor power requirements besides the strength of signal powers (in-band, out-of-band and desired). For *case b)* when $\alpha = 0$ (only BS→MS ACI) the mean ACP factor is 19.1887 dB and for *case a)* when $\alpha = 1$ (only MS→MS ACI) the mean ACP factor is 15.8514 dB. *Case a)* presents the 'best case' as the recorded ACP mean is the lowest, therefore requiring less ACS to satisfy the Eb/No requirement. *Case b)* is a worse case as the 3.3373 dB increase in the mean concludes that it requires 2.156 times the ACP factor than *case a).*

The mean of the ACP factor is further increased to 19.3864 dB for *case c)* when $\alpha = 0.5$. The introduction of BS→MS ACI along with MS→MS ACI increases the mean of the ACP by 1.05 times compared to *case b)* and 2.26 times compared to *case a).* As synchronisation cannot be assumed in a fully flexible system, random α values are used in *case d).* The mean is slightly less than *case c)* but requires 2.19 times the ACP than *case a).* The analysis of ACP factors concludes that synchronisation factors affect the amount of ACP required to meet the noise requirements of the receiver. Findings have also demonstrated that there are minor probabilities of ACP factors above 30 dB.

5.2.2.2 Adjacent Channel Selectivity Analysis

Further analysis was performed on the corresponding ACS powers. In this analysis, uniform random α were used and are the basis for other investigations from this point forward. Figure 5.2 presents a statistical analysis of ACS powers and is compared against the corresponding ACP factors. The figure consists both cdf and pdf analysis. Table 5.3 lists the recorded results corresponding to Figure 5.2.



a) b)

Figure 5.2 Statistical analysis ACS powers versus the corresponding ACP factors
a) cdf, b) pdf

The results in Table 5.3 yield that there are insignificant differences in the mean and standard deviations of ACP factors and ACS powers. There is only a 0.0116 dB

difference in the means of ACS and ACP and an 1 $x10^{-4}$ dB difference in the standard deviations.

Table 5.3 Statistical analysis results of ACP factors and ACS powers

Quantity	*E (Quantity)* (dB)	*STD (Quantity)* (dB)
ACP Factor	19.2617	12.3802
ACS Power	19.2733	12.3801

The major difference between ACP and ACS is above 33 dB where the ACS powers tend to saturate. This is due to the adjacent channel leakage ratio (ACLR) as there may be some power leakage from out-of-band channels into the in-band channel. The leakage interference powers cannot be filtered by the receiver RRC filter. Therefore, there is a 2.2 percent outage and the target Eb/No cannot be met in some cases. Figure 5.3 illustrates an example of out-of-band channel leakage into the in-band channel.

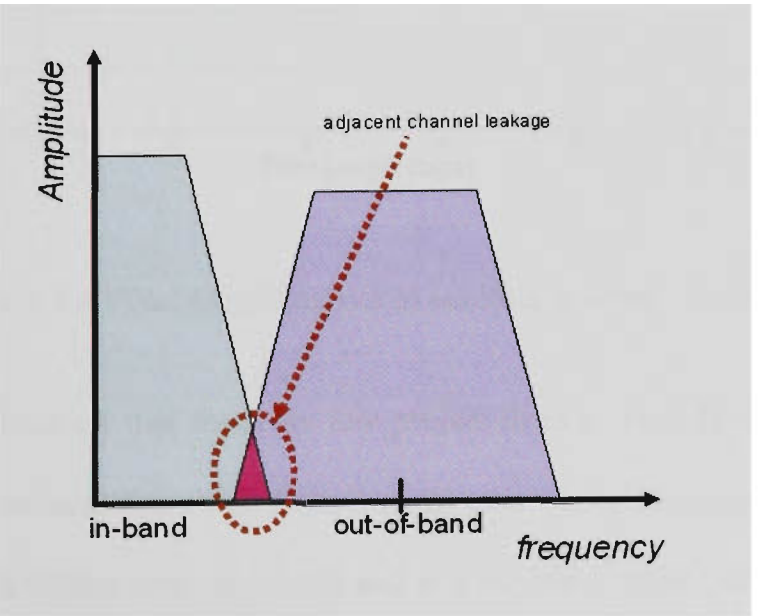


Figure 5.3 Example of out-of-band channel leakage power into in-band channel

5.2.2.3 Filter Length Analysis

The ACS powers were converted to the corresponding filter lengths (taps) using the LUT in Table 4.4. Figure 5.4 illustrates the statistical analysis of filter lengths in terms of cdf. The figure clearly shows that various probabilities exist for various filter lengths. Cell coverage of 20 percent is achievable with 3 taps and 5 taps can obtain cell coverage of 47 percent.

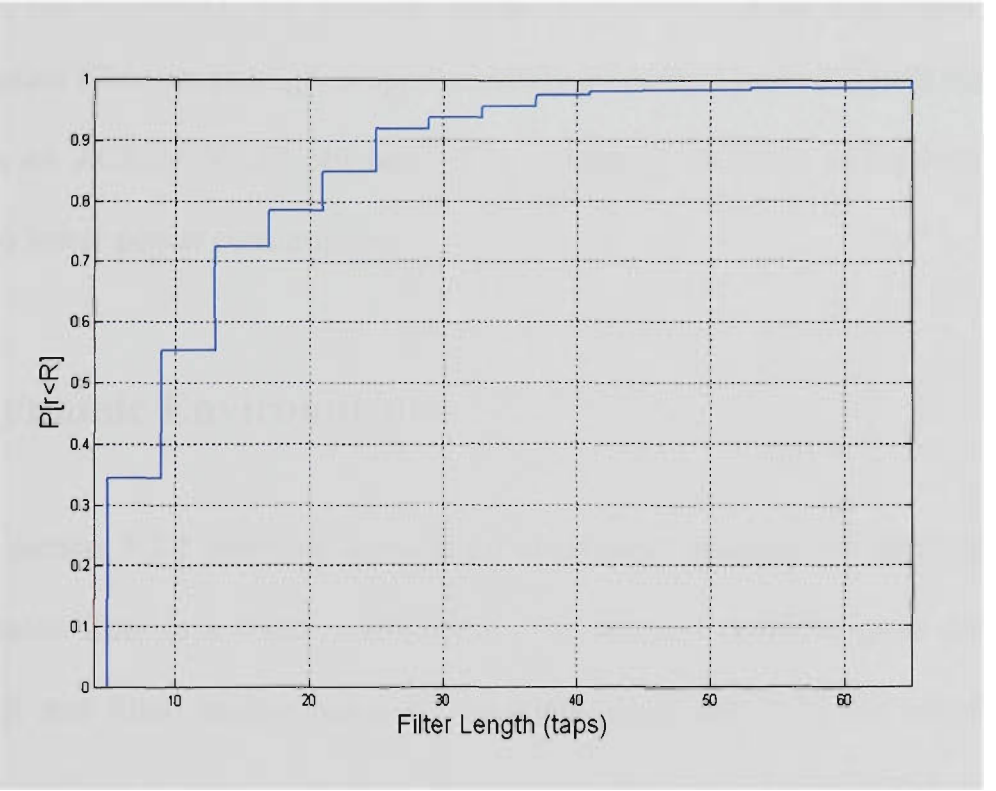


Figure 5.4 Filter length statistical analysis in terms of cdf

The findings also illustrate that there are low probabilities of high filter lengths above twenty taps. High probabilities range from 5 to 20 taps where the mean is 9 taps. The average filter length differs from the mean and is a function of the percentage of each length and the tap value. It is defined as $Average_{length}$ and is as follows:

$$Average_{length} = \sum_{1}^{n}\left(\frac{\rho(n) \bullet Tap(n)}{100}\right) \tag{5.1}$$

where $\rho(n)$ is the percentage of time at a filter length n and $Tap(n)$ is the filter length value. Solving equation (5.1) yields an average filter length of 10.1 taps. 3rd Generation Partnership Project (3GPP) specifications require a minimum ACS of 33 dB. Key ACS findings presented Figure 5.2 a) shows that an ACS of 33 dB will result in a 10 percent outage. Therefore, for comparison reasons with the average filter length, an ACS of 50 dB is considered corresponding to a receiver filter length of 49 taps. This ACS value results in approximately 2.2 percent outage probability. This concludes that the reconfigurable filter, on average, is approximately 80 percent more efficient than a fixed filter with an ACS of 50 dB (49 taps). The efficiency, in terms of hardware, would translate to lower power consumption.

5.2.3 Dynamic Environment

Thus far, section 5.2.2 provided a statistical analysis to evaluate the efficiency of the reconfigurable filter in a static environment. The analysis provided good insight into ACP, ACS and filter lengths based on equations (4.6) and (4.7) but overall cannot provide an analysis in terms of Eb/No. This is due to the static nature of the simulations as the Eb/No, when calculated will always be met as the signal powers are static. The analysis also did not consider hysteresis protection as discussed in Chapter 4 as there was no need. Therefore, this section provides a statistical analysis in a dynamic simulation environment of the reconfigurable filter. This analysis can better estimate the performance of the filter as 'real' channels are simulated for signal powers and are changing dynamically with time, especially as the filter employs a feedback approach.

Each signal source (interfering or desired) was generated with a simulated base band transmitter (see Annex A for 3GPP specifications for spreading and modulation) before being processed by a Rayleigh flat fading channel (see Annex B). All signals were combined to produce one channel that is processed by a simulated base band mobile receiver. Figure 5.5 presents the block diagram of the mobile base band UTRA-TDD receiver with reconfigurable in-phase (I) and quadrature (Q) filters. The simulation parameters were described in section 5.2.1 for this analysis.

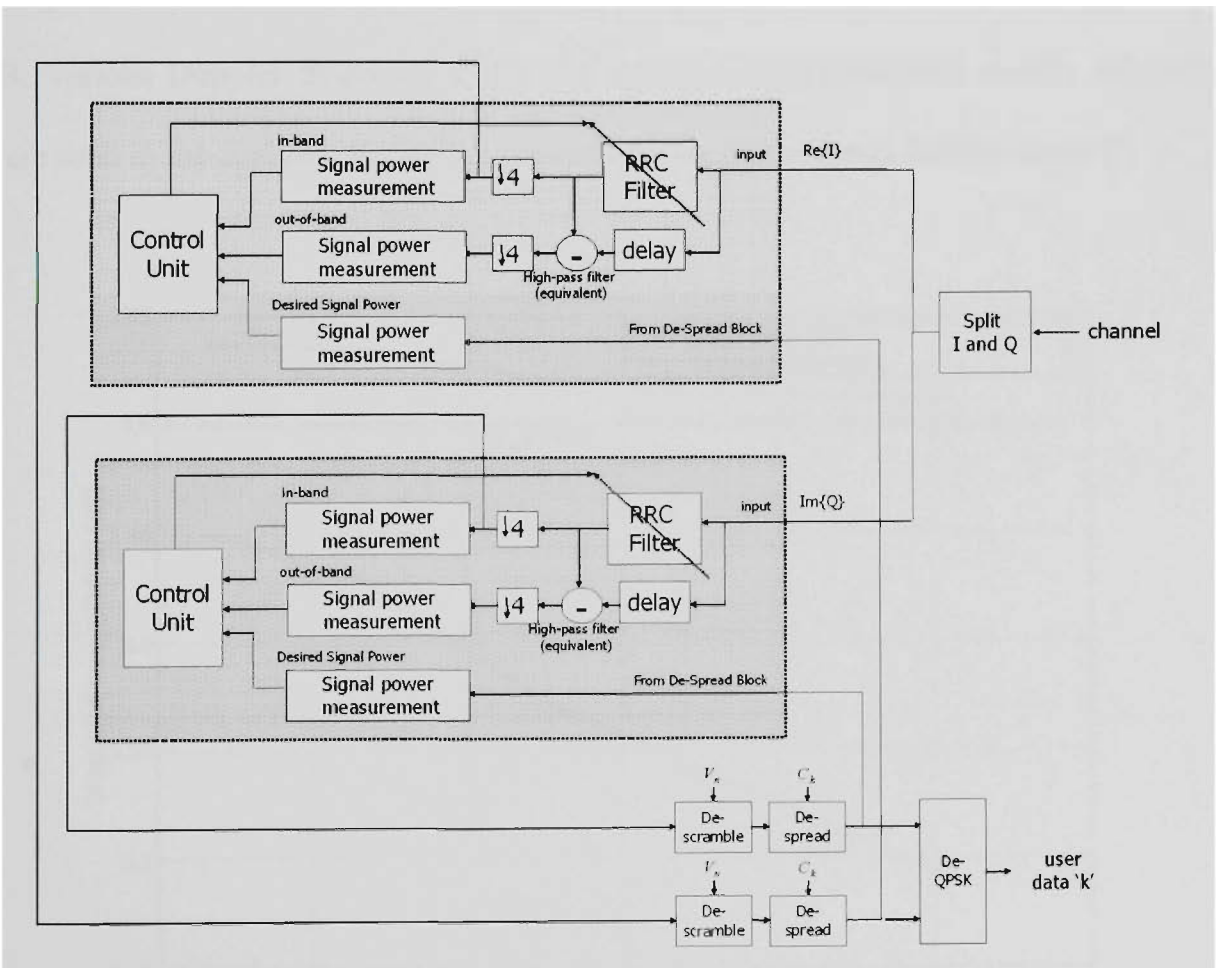


Figure 5.5 Simulated base band receiver with reconfigurable filters in I and Q

The reconfigurable filters (shaded) are identical as described in Chapter 4. The other components in the receiver were described in Chapter 2. The channelisation OVSF codes, C_k, are of length 16 which yields data rates listed in Table 5.4.

Table 5.4 Data rates in UTRA-TDD receiver based on simulation parameters

Location in Receiver	*Sampling Frequency*	*Data Rate / Time Slot*
Input to Filter	15.36 MHz	1.024 Mega symbols/second
Output of Filter	3.84 MHz	256 Kilo symbols/second
Output of De-spread units	240 Kilohertz (kHz)	16 Kilo symbols/second
A symbol rate of 16 Kilo symbols/s corresponds to a bit rate of 32 Kbps for each user for QPSK data mapping		

5.2.3.1 Bit-Energy to Interference Ratio Analysis

The performance of the filter was measured in terms of Eb/No where the target is 3.5 dB. Various Doppler frequency shifts (F_d) corresponding to various mobile velocities were used in the analysis. Figure 5.6 presents the measured mean Eb/No versus F_d.

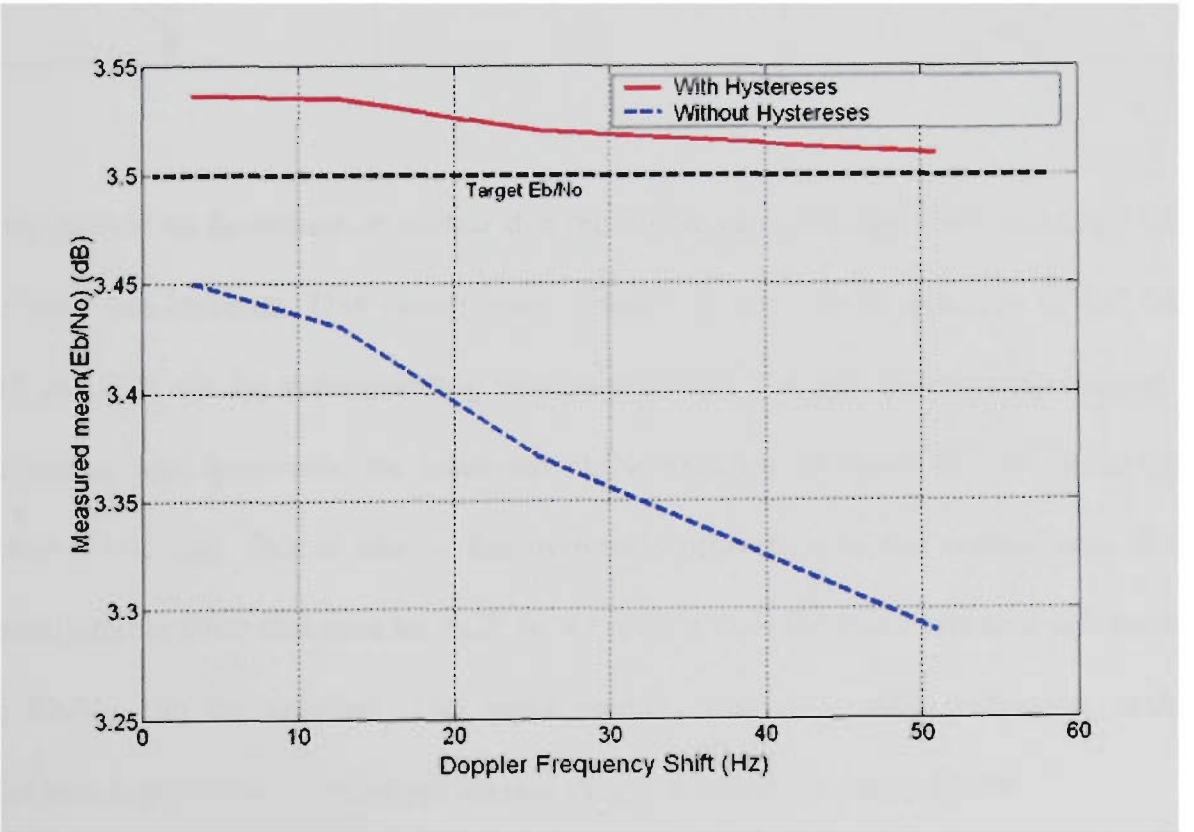


Figure 5.6 Doppler Frequency Shift vs. Measured Eb/No

The figure consists of two Eb/No measurements. The dotted line illustrates the measured Eb/No before hysteresis protection and the solid line corresponds to the

Eb/No measured after hysteresis protection. The figure clearly demonstrates that as F_d increases, the measured Eb/No drops. This is due to the fact that all mobiles (adjacent, intra-cell and desired) velocity is increasing but the F_r remains fixed. Therefore, there may be a dramatic change in signal powers in the next frame of samples compared to the frame where the new filter length was calculated. Table 5.5 presents the measured Eb/No corresponding to Figure 5.6

Table 5.5 Measured Eb/No versus mobile velocity for before and after hysteresis protection

Mobile Velocity (meters/s)	*Eb/No (no hysteresis)*(dB)	*Eb/No (with hysteresis)* (dB)
0.5	3.45	3.537
2	3.43	3.535
4	3.37	3.532
8	3.29	3.519

In the case of *no hysteresis*, it is clear that the Eb/No cannot be satisfied especially when the velocities increase. This causes great concern as it results in data loss of 0.5, 0.07, 0.13 and 0.21 dB for corresponding velocities of 0.5, 2, 4 and 8 meters per second. In the case of *with hysteresis*, the measured Eb/No satisfies the target Eb/No for the same mobile velocities. This is due to the hysteresis protection in the control unit of the reconfigurable filter that uses an ACP factor greater than the exact required and ensures the Eb/No can be satisfied. The trend predicts that even with protection, mobile velocities higher than 8 meters per second might not meet the target Eb/No.

5.2.3.2 Adjacent Channel Protection Factor and Filter Length Analysis

As UTRA-TDD is primarily intended for operation in an indoor environment, a mobile velocity of 2 meters per second (F_d = 12.75Hz) is suitable and is used for the statistical analysis of ACP factors and the corresponding filter lengths. Figure 5.7 illustrates the statistical analysis of ACP factors for the dynamic environment. The figure presents two analyses. The dotted line presents the cdf of ACP factors before hysteresis protection and the solid line presents the analysis after the protection. The corresponding recorded results are presented in Table 5.6

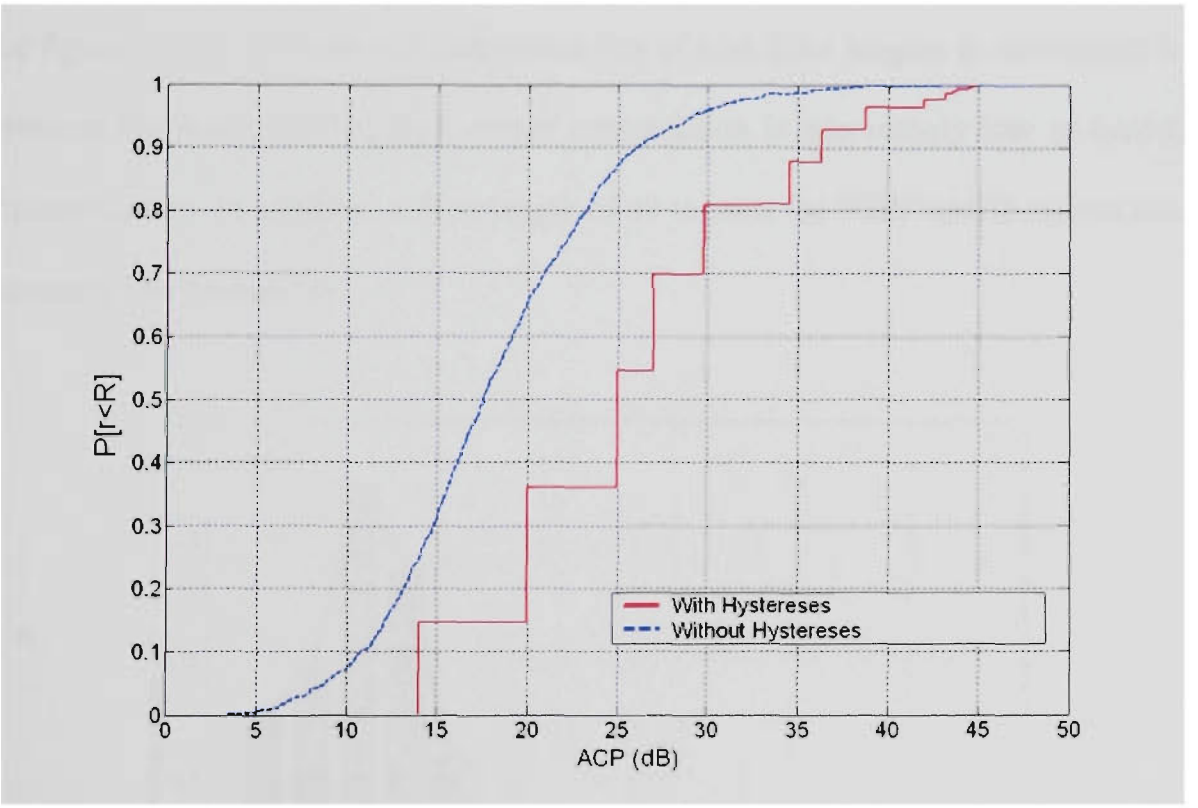


Figure 5.7 cdf of ACP before and after being processed by hysteresis protection

There are low probabilities of ACP factors above 33 dB and 25 dB for with and without hysteresis protection respectively. The mean and standard deviation of the ACP factors with hysteresis protection increases by 7.26 dB and 1.314 dB respectively compared to

without protection. The 7.26 dB difference in the mean yields that protection requires 5.32 times the ACP factor than without protection. Nevertheless, the protection is required to ensure the Eb/No requirement is satisfied.

Table 5.6 Statistical analysis results of ACP factors before and after hysteresis protection

Hysteresis Protection	*E (Unit)* (dB)	*STD (Unit)* (dB)
No	18.24	6.204
Yes	25.5	7.518

The corresponding analysis of filter lengths is presented in Figure 5.8 in terms of pdf. The figure visibly demonstrates that probability of high filter lengths is particularly low; therefore the probability of high power consumption is accordingly low in hardware implementation. In addition, a filter length of 49 to meet the 3GPP specifications has an extremely low probability.

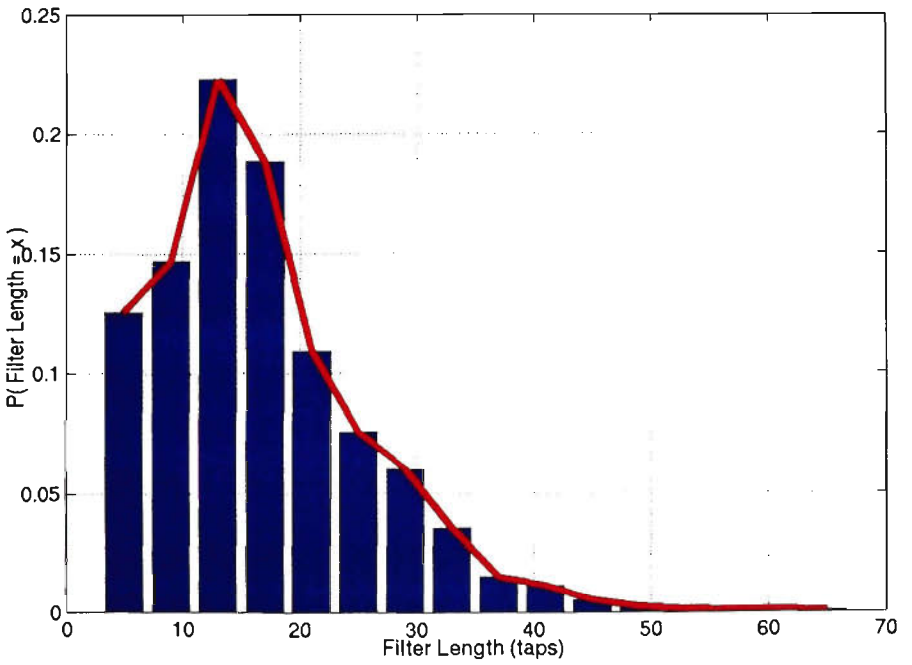


Figure 5.8 pdf of filter lengths after hysteresis and safety margin protection

The average filter length recorded was 16.7 which is comparably higher compared to the 10.1 average in the static analysis performed in section 5.2.2.3 due to the addition of hysteresis protection in these dynamic simulations. Nevertheless, average of 65 percent efficiency for each I and Q filters is available for UTRA-TDD compared to a fixed filter length of 49.

5.3 Implementation Approach

This section of the chapter describes the implementation of the reconfigurable digital filter and presents a performance analysis in terms of power consumption. Realisation and considerations of the implementation approach are presented in section 5.3.1 and the performance analysis is presented in section 5.3.2.

5.3.1 Realisation and Considerations

The realisation of the reconfigurable digital filter should be flexible to allow reconfiguration of parameters in the control unit apart from reconfiguration of filter lengths. This will allow the filter to be reconfigured to various operating environments, such as TDD, frequency division duplex (FDD) or others. It will also allow algorithm updates to be configured in the control unit to employ more efficient operation.

To achieve such a realisation, the reconfigurable digital filter was hardware and software partitioned. For flexibility, a DSP core was chosen for the control unit realisation and a semi-custom ASIC (see Annex C for semi-custom ASIC design

methodology) was chosen for other components in the system architecture. Figure 5.9 illustrates the partition.

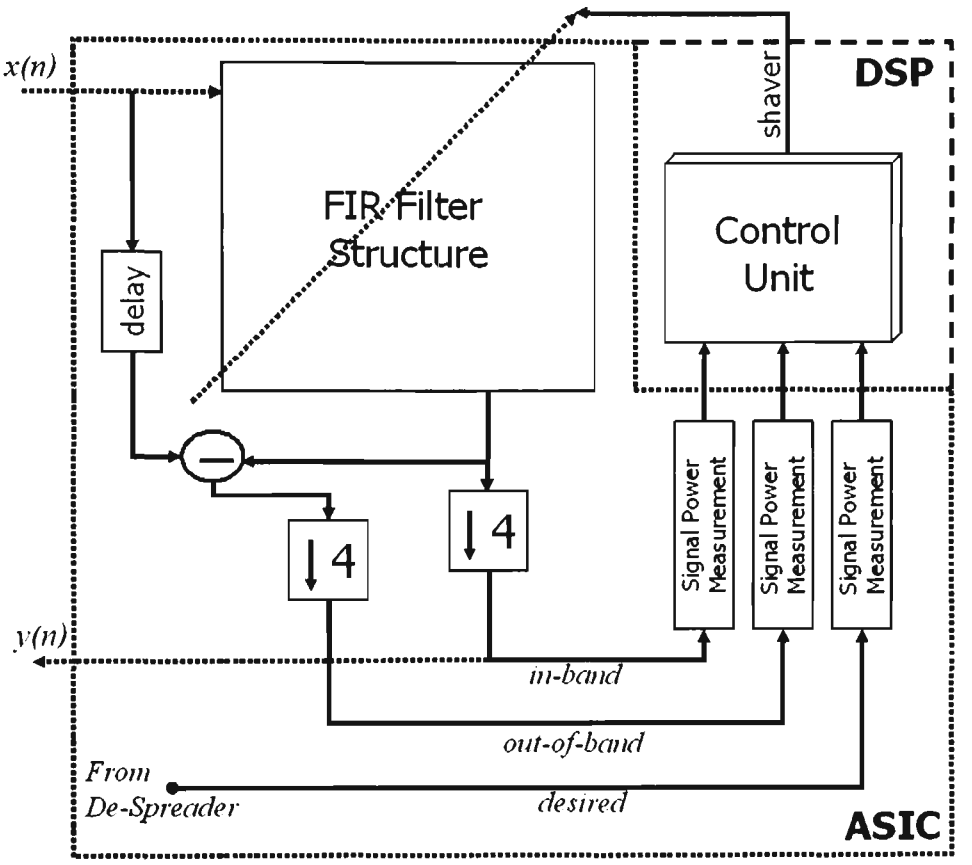


Figure 5.9 Hardware / Software partition of reconfigurable digital filter

The grey shaded components in the above figure illustrate the components that were implemented as a semi-custom ASIC and the non-shaded component (control unit) is partitioned for the DSP. A DSP allows the software to be reprogrammed or updated which allows the filter to be flexible. An ASIC possesses high speed and low power properties, as it is in nature, specific to a certain application, therefore, providing maximum efficiency. A multiplier in hardware uses a shift and sum algorithm, which depending on the word length of its operands, it can be costly on power; therefore, the ASIC is the appropriate partition. The ASIC was coded in Very High Speed Integrated

Circuit Hardware Description Language (VHDL) – register transfer level (RTL) and synthesised in Synopsys Design Compiler using DesignWare digital libraries. Figure 5.10 presents the top-level entity of the ASIC and the corresponding synthesised schematic is presented Figure 5.11.

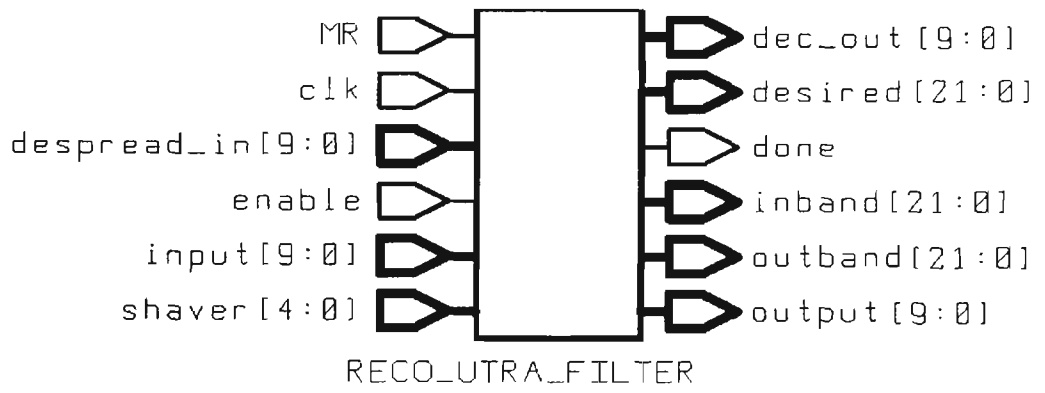


Figure 5.10 Reconfigurable digital filter ASIC top level entity

A word length of 10 bits is used for the *input* and *despread_in* (signal from de-spread block in receiver). The input word lengths depend on the resolution of the analog to digital converter in the receiver. In this implementation the word lengths were arbitrarily selected. Reducing the word length would save power as the computational complexity would reduce. The maximum *shaver* value is 30 that corresponds to '11110' in binary, therefore 5 bits is ample for scaling the filter length. The output of the filter; *decimated_output* and *output* also have word lengths of 10 bits to keep consistency with the input word lengths. The three inputs to the control unit (*in_band, out_of_band* and *desired*) have word lengths of 22 bits as higher precision is required to represent the signal powers. It is a synchronous system controlled by the clock (*clk*) and has an asynchronous master reset (*MR*). The *output* signal is processed in one clock cycle and

the *dec_out* signal every four clock cycles as it is decimated by a factor of four. The *enable* signal initiates the filtering and *done* signals completion.

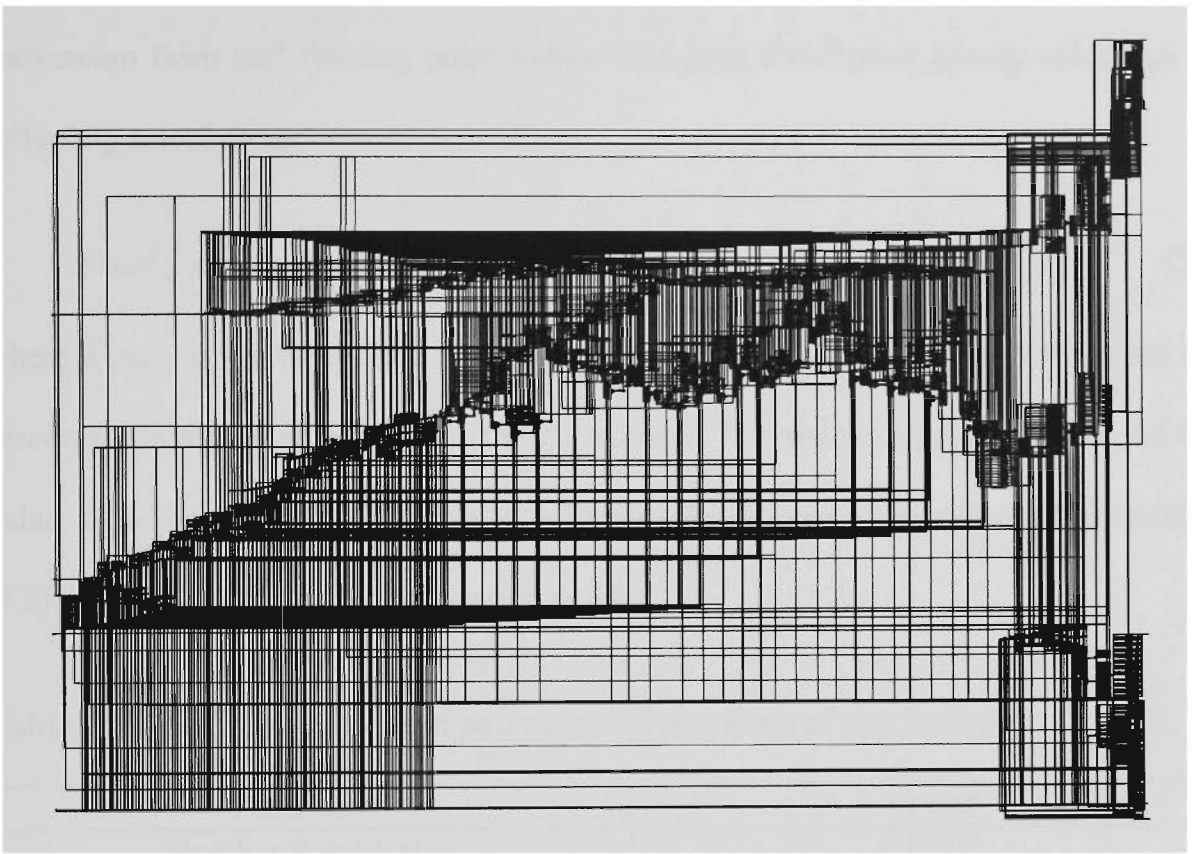


Figure 5.11 Reconfigurable digital filter ASIC synthesised schematic

The number representation in the reconfigurable filter system is signed 2's complement fixed-point. Fixed-point numbers practically have the same precision as floating point numbers and have the advantage of lower power consumption in digital hardware. This is desirable for mathematical operations such as multiplications. Figure 5.12 presents a comparison of signed integer and signed fixed-point numbers.

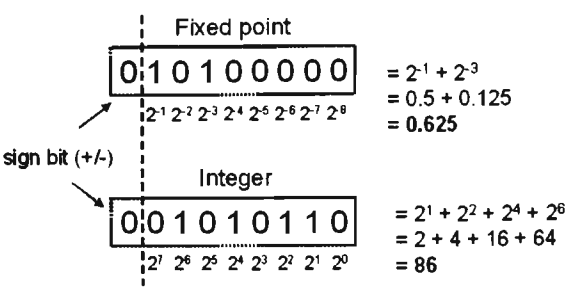


Figure 5.12 Signed integer versus signed fixed-point numbers

As the filter deals with real value (floating point) coefficients, they must be represented by fixed point values in hardware. Two examples are considered to demonstrate the conversion from real floating point values to signed fixed point binary values by the following calculations:

$$Fixed_p = truncate\left(real \bullet \left[1 << (resolution - 1)\right]\right) \quad or \quad = real \bullet \left[2^{resolution-1}\right]) \tag{5.2}$$

where $Fixed_p$ is the final fixed point conversion, *real* is the floating point number and *resolution* is the word length for the conversion. The first example converts the real value, 0.2650 (middle coefficient) to a 12 bit signed fixed point value using equation (5.2). Table 5.7 presents the conversion results.

Table 5.7 Floating point to fixed point conversion results of first example

Parameter	*Result*
Floating Point Value	0.2650
Fixed Point Value, $Fixed_p$	542
Corresponding 12 bit binary	001000011110
Fixed Point value converted back to Floating Point	0.2646484375

When the fixed point value is converted back to a real number, there is some degree of error due to the quantisation effects. In this example there is a 0.13 percentage of error. In the second example, a negative floating point number –0.0448 (coefficient 27 and 39) is considered. Results are presented in Table 5.8.

Table 5.8 Floating point to fixed point conversion results of second example

Parameter	*Result*
Floating Point Value	–0.0448
Fixed Point Value, $Fixed_p$	–91
Corresponding 12 bit binary	111110100101
Fixed Point value converted back to Floating Point	–0.00445

In this example, there is a greater error percentage of 0.78 percent. This is due to smaller floating point numbers in terms of magnitude (as well as floating point numbers with large magnitude) require greater precision in terms of word length. A higher precision would be more demanding on power consumption and a lower precision would increase the quantisation error, therefore 12 bits for the filter coefficients is suitable. Figure 5.13 presents the frequency response when the coefficients are quantised to 12 bits.

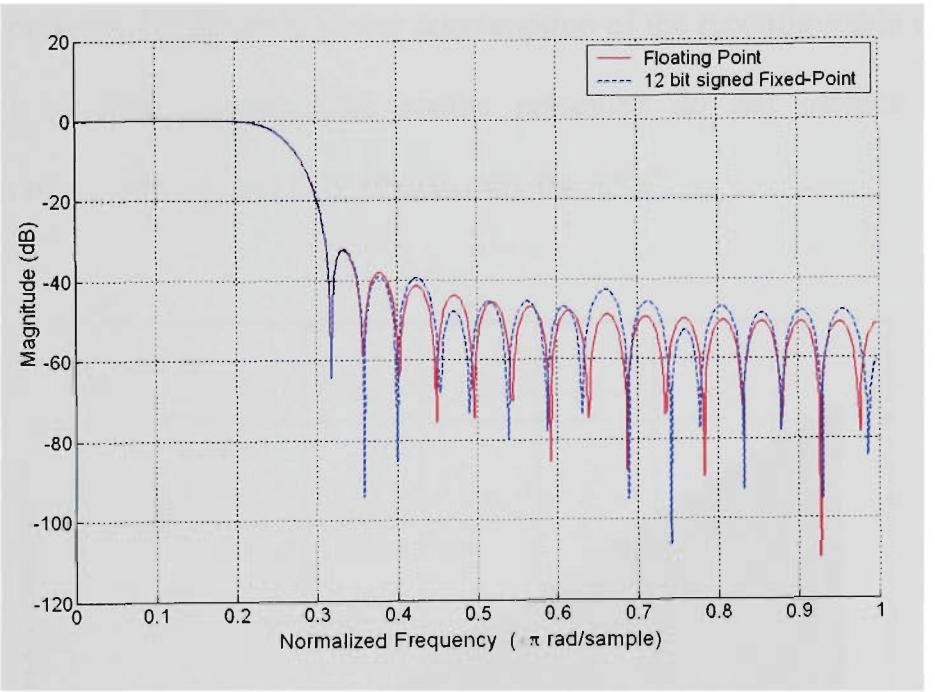


Figure 5.13 Frequency response of RRC filter with 12 Bit fixed-point coefficients

5.3.2 Performance Analysis

The performance analysis was carried out on the ASIC to ensure it meets the timing requirement (sampling frequency of 15.36 MHz) as well as low power requirements. The analysis was carried out at synthesis stage in Synopsys Design Compiler. Table 5.9 presents the simulated attributes of the ASIC at synthesis stage.

Table 5.9 ASIC specifications

Parameter	*Value*
Core Supply Voltage	1.62 Volts (V)
Maximum Clock Frequency	22 MHz
Critical Path	45.11 nano seconds (ns)
Synthesis Technology	*core_slow* (Synopsys educational libraries)
Resolution	10 bits

The dominating factor in power consumption for a digital filter is the multiplier. Therefore, the power consumption should increase linearly as the filter length increases. Figure 5.14 presents the dynamic power consumption of the reconfigurable digital filter with respect to filter lengths. The results presented do not include the power consumption of the control unit DSP (P_{DSP}), only the ASIC.

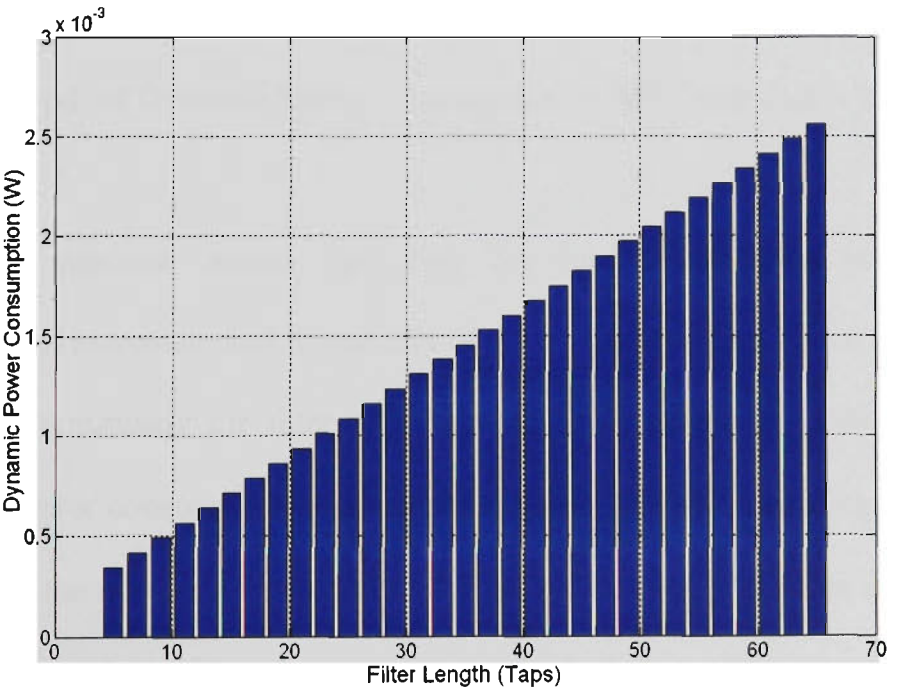


Figure 5.14 Dynamic Power Consumption of ASIC core (*clk* = 15.36 MHz)

The above figure demonstrates that as the filter length increases, the power consumption increases linearly. For a filter length of 5, the power consumption is 340 micro watts

(μW) excluding P_{DSP} and for a length of 65, it is 2.56 milli watts (mW) excluding P_{DSP}. Figure 5.15 illustrates a statistical analysis of the power consumption.

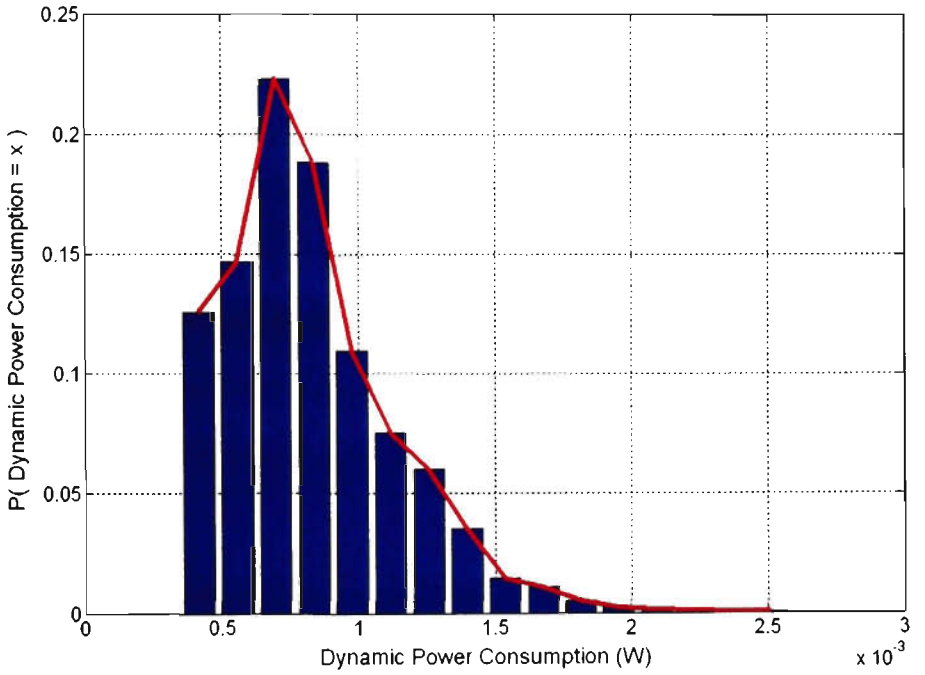


Figure 5.15 pdf of Dynamic Power Consumption of ASIC core (*clk* = 15.36 MHz)

The statistical analysis reveals that there are low probabilities of high power consumption and extremely low probability of power consumption above 1.5 mW. In an UTRA-TDD environment the filter will consume low amounts of power on average. The average power consumption was calculated to be 755 μW excluding P_{DSP}. P_{DSP} is proportional to the number of instructions for the control unit algorithm in a DSP core. If the control loop is performed every n samples, then the power consumption of the DSP core, P_{DSP}, could be estimated as follows:

$$P_{DSP} = \frac{P_{\#instructions}}{n} \tag{5.3}$$

where $P_{\#instructions}$ is the dynamic power consumption of a DSP core proportional to the number of instructions required for the control unit. This will result in a minor power consumption increase depending on the DSP core employed for implementation. The most suitable DSP core would employ low power properties while exhibiting high speeds and is suitable to wireless communications. Star*Core DSP cores are targeted at next generation wireless communication platforms they exhibit high speed and low power properties incorporating advanced power management [81, 82]. The Star*Core SC110 DSP core addresses the following needs and features [81 - 85]:

- Great Performance: 300 MHz (900 reduced instruction set computing (RISC) millions instruction per second (MIPS)) at 1.5 volts and 120 MHz (360 RISC MIPS) at 0.9 V
- Efficient Compatibility: 90 percent of coding can be developed in C and can reduce time to market
- Low System Cost: Excellent code density can reduce amount of memory for System-on-a-Chip (SoC) products
- Low Power Consumption: Peak power consumption of 90 mW and 13 mW at operating voltages of 1.5 V and 0.9 V respectively

If the control unit consumed peak power consumption in the SC110 and it was processed every TDD frame (2560 samples), the power consumption would yield 35 μW. As a result, the average power consumption of the entire reconfigurable digital filter would yield 790 μW. The power consumption of a fixed length 49 tap filter with no reconfigurable components yields 1.92 mW of power consumption. Therefore, an

average 59 percent power dissipation saving is available for both I and Q filters where the maximum power saving is 83 percent. The savings will be higher when the P_{DSP} is measured per instruction, not peak power. The drawback is when the reconfigurable filter requires 49 taps to meet the Eb/No it will consume more power than a fixed filter of the same length due to the additional components.

5.4 Conclusions

The focus of this chapter was to present a detailed analysis of the reconfigurable digital filter. It considered a statistical analysis in a simulation environment with both static and dynamic characteristics and also presented the implementation approach along with a performance in terms of power dissipation.

The static analysis of ACP factors, ACS and filter lengths was performed. The ACP factor analysis initially shows that the probability of high values is low and that synchronisation factors play a key role in the strength of ACP factors besides the strength of signal powers. The mean increases by a maximum 3.535 dB when varying the synchronisation factors. The static ACS analysis employed random synchronisation factor values. The analysis revealed that the mean and standard deviation varies by a minor percentage compared with the corresponding ACP factors. The major difference between ACP and ACS is above 33 dB where the ACS powers tend to saturate due to leakage from adjacent channel in the in-band. This cannot be filtered and a there is a 2.2 percent outage. The static filter length analysis concluded that the average filter length

is 10.1 for UTRA-TDD, which corresponds to an 80 percent efficiency saving compared to a fixed filter length of 49 to meet 3GPP requirements.

The dynamic analysis showed that without hysteresis protection in the control unit of the system, the required Eb/No is never met and drastically reduces when the mobile velocity increases. With protection, the Eb/No is met as it ensures a higher ACP factor is used than the minimum. The dynamic analysis also revealed that the mean of ACP factors varies by 7.26 dB for with and without protection, therefore, the average filter length will increase correspondingly. The mean ACP factor recorded was 25.5 dB with hysteresis protection. The corresponding filter length analysis demonstrated that probability of high filter lengths is particularly low; therefore the reconfigurable filter can save major power dissipation in hardware implementation. A 65 percent efficiency saving for each I and Q filters is available compared to a fixed filter length of 49.

The reconfigurable digital filter was hardware / software partitioned onto an ASIC and DSP to achieve high performance and exhibit flexibility. Realisation considerations were discussed in terms of resolution of the filter, number representation and coefficient quantisation effects. The ASIC was coded in VHDL - RTL and synthesised in Synopsys Design Compiler using DesignWare digital libraries. Performance analysis shows that the reconfigurable digital filter consumes 790 μW of core dynamic power with a clock frequency of 15.36 MHz, which includes the peak power consumption of the Star*Core SC110 DSP core per TDD frame. The DSP core is not only used for the filter, but for other components in the mobile transceiver, therefore, the area will be shared. The power consumption of a fixed length 49 tap filter yields 1.92 mW of power

consumption concluding that an average 59 percent power dissipation saving is available for both I and Q filters. The savings will be greater as the DSP power consumption is assumed at peak and not per instruction.

Chapter 6

Reconfigurable Pipelined Architecture

6.1 Introduction

This chapter exploits the findings in Chapters 4 and 5 and has led to the design of a reconfigurable-pipelined architecture (RPA) for the time division duplex (TDD) mode of universal mobile telephone service (UMTS) terrestrial radio access (UTRA). The architecture consists of an analog to digital converter (ADC) where its output is fed to the digital receiver root raised cosine (RRC) filters' (as described in previous chapters) input. The motivation for this design is that the ADC in the mobile receiver is also one of the major players that consume considerable amounts of battery power. The reconfigurable principle that applies to the filter also applies to the ADC, that is, the resolution of the ADC greatly depends on in-band and out-of-band signal powers.

The basic concept of the RPA is to only utilise the required filter adjacent channel selectivity (ACS) to meet the required bit-energy to interference ratio (Eb/No) and to

assign any remaining noise available in the system to quantisation noise of the ADC. The resolution or word length of the ADC is a function of dynamic range which depends greatly on quantisation noise (noise floor); therefore various quantisation noise values produce various word lengths of the ADC. The concept of the ADC is based similar on the concept of the filter and is illustrated in Figure 6.1. If adjacent channel interference (ACI) and intra-cell interference powers are low, the ACS of the filter can be reduced and the resolution of the ADC can be decreased to a level that satisfies the Eb/No, therefore saving battery power. Otherwise, if ACI and intra-cell interference powers have increased in strength, the ACS of the filter and the resolution provided by the ADC may have to increase to meet the Eb/No.

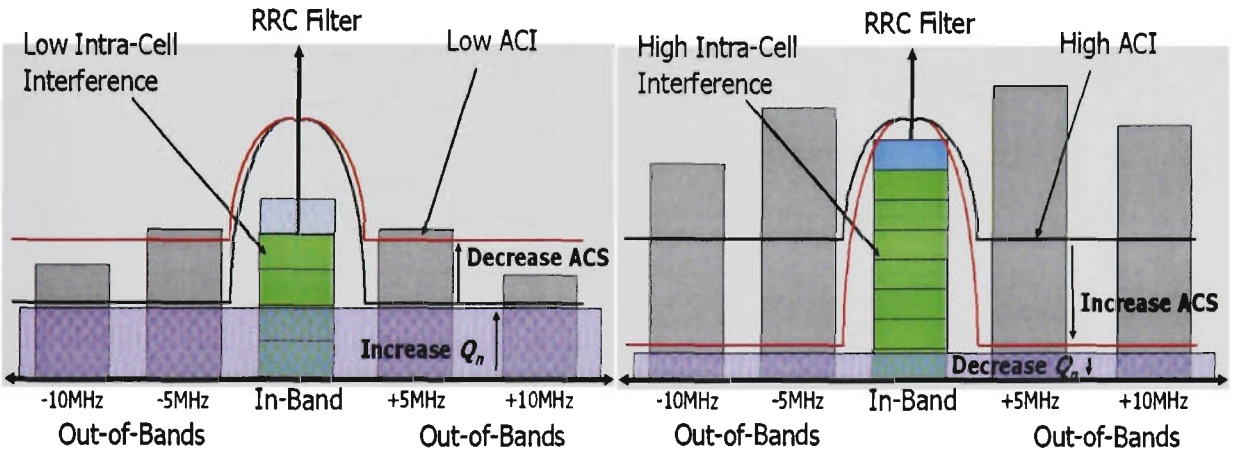


Figure 6.1 Spectrum analysis of operational concept of RPA

The chapter is prepared as follows: section 6.2 describes the RPA in detail that includes algorithm formulations as well as ADC considerations suitable for the RPA. A statistical analysis in a static simulation environment is presented in section 6.3 to evaluate the efficiency of the RPA. Conclusions are presented in section 6.4.

6.2 System Design

The RPA is described in this section. The architecture of the RPA is similar to the reconfigurable digital filter described in Chapter 4 with the addition of an ADC. Figure 6.2 presents the UTRA-TDD mobile receiver with the RPA. Firstly, the algorithm enabling the filter and ADC to exhibit variable lengths and resolutions is formulated and the corresponding system architecture is introduced. The subsequent sections give insight into considerations of the ADC and propose the structure suitable for the RPA.

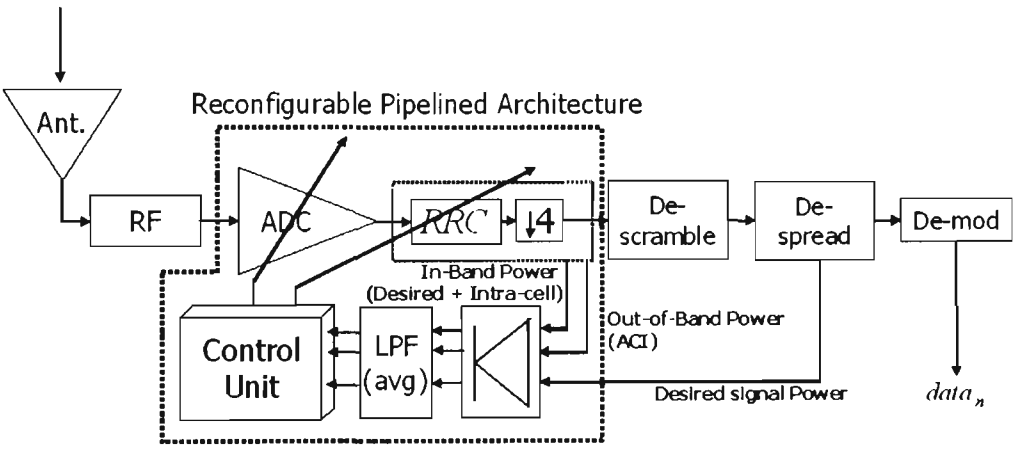


Figure 6.2 UTRA-TDD mobile receiver block diagram with RPA

6.2.1 Algorithm Formulation

The algorithm is formulated from the Eb/No model given in equation (3.2). ADC quantisation error, Q_n, is introduced as noise and the Eb/No is represented by:

$$Eb/No = \frac{P_{rx}^{\ i} pg}{(M-1)P_{rx}^{\ i} + \frac{I_{adj}^{\ i}}{ACP} + \eta + Q_n} \tag{6.1}$$

In the above model, there are two unknown variables (ACP and Q_n) as both require solving to determine the required adjacent channel protection (ACP) factor of the filter as well as the allowable quantisation noise of the ADC. One of the variables must be known to solve for the other, otherwise it is not possible. When solving for ACP, the quantisation noise is assigned as a function of ACI and ACP along with a gain factor, G_k, to scale the required ACP and allow room for quantisation noise. Therefore, Q_n is defined as follows when solving for ACP:

$$Q_n = G_k \bullet \left(\frac{I_{adj}{}^{i}}{ACP} \right) \tag{6.2}$$

Substituting equation (6.2) into (6.1) and solving for ACP yields:

$$ACP_{scaled}{}^{i} = (G_k + 1) \bullet \left(\frac{I_{adj}{}^{i}}{P_{rx}{}^{i}\left(1 + \frac{pg}{Eb/No}\right) - P_{rx}{}^{i} M - \eta} \right) \tag{6.3}$$

From equation (6.3) it is clear that the ACP factor will be scaled higher as the ACI is scaled by a factor of (G_k+1). Therefore, if the Eb/No is calculated, it will be higher than the target allowing the difference to be utilised as quantisation noise. To solve for quantisation noise, the calculated ACP factor from equation (6.3) is substituted in equation (6.1) and solved for Q_n listed below:

$$Q_n = P_{rx}{}^{i}\left(1 + \frac{pg}{Eb/No}\right) - P_{rx}{}^{i} M - \frac{I_{adj}{}^{i}}{ACP_{scaled}{}^{i}} - \eta \tag{6.4}$$

where ACP_{scaled} is the ACP factor calculated from equation (6.3) that is scaled by (G_k+1). The three signals; I_{adj}^{i} as the *out-of-band* signal, P_{rx}^{i} as the *desired* signal and $P_{rx}^{i}M$ as the *in-band* signal are identical to that described in Chapter 4. Based on the above formulations, the RPA is presented in Figure 6.3.

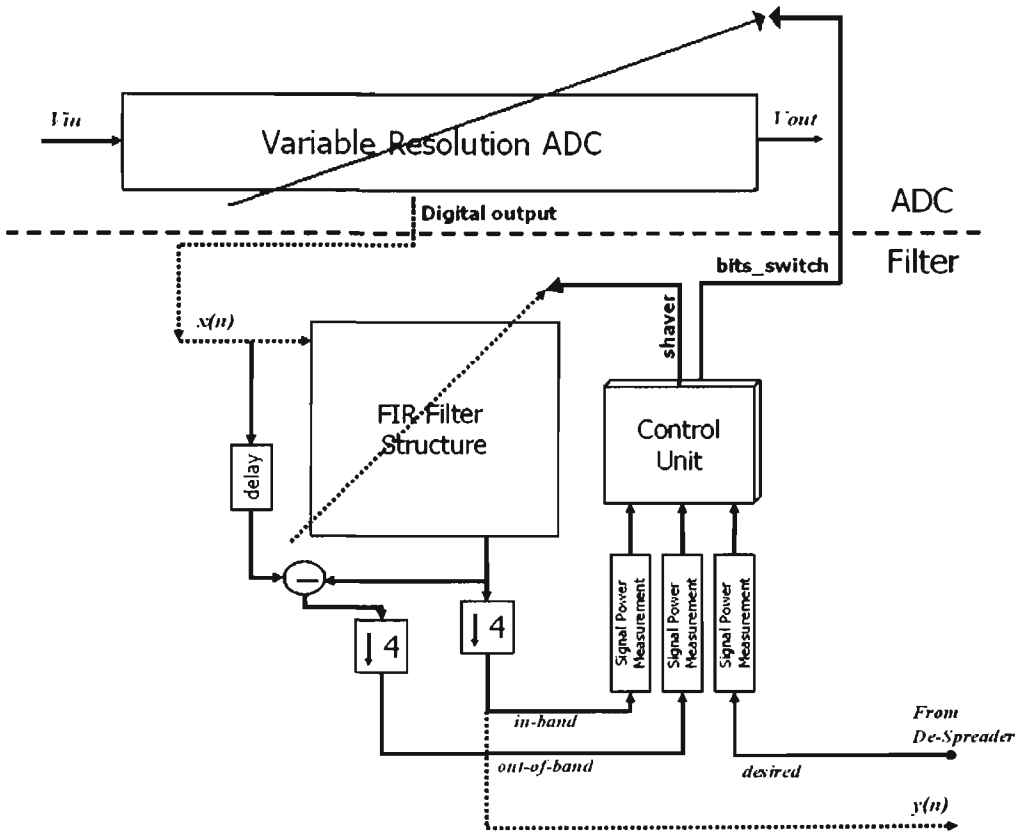


Figure 6.3 RPA block diagram

It consists of the reconfigurable digital filter identical to that presented in Chapter 4 and an ADC converter employing a variable resolution. Each of the ADC stages would output a certain number of bits, *n*, and are switched on or off depending on the dynamic range requirements which is controlled by the system control unit. The figure clearly demonstrates that the resolution of the ADC depends on the signal powers of the in-band, out-of-band and desired signals. The control unit is described in section 6.2.3 where the findings in this section are exploited.

6.2.2 Analog-to-Digital Converter Considerations

This section considers many aspects inherent to the design of the ADC for the RPA. It does not provide filter considerations as these have been discussed in the previous chapters. Two issues are discussed; firstly, an ADC structure that is suitable for the RPA and for wireless communications. Secondly, a dynamic range analysis is performed to determine the minimum resolution for the ADC that will not affect the noise performance of the receiver.

6.2.2.1 Suitable ADC Structure

ADCs are fundamental crossing points in mixed-signal systems. With the rapid growth in semiconductor technology and device scaling, digital integrated circuits (ICs) have achieved low power consumption and high speed. Today, more functions are performed on digital circuits rather than analog which impose problems to mixed-signal ICs. Firstly, the speed of the ADC boundary has to be scaled with the speed of the digital circuits in a system to truly take advantage of complex technologies. Secondly, the cost of ADCs is higher compared to digital circuits; therefore digital circuits are desirable to accomplish high levels of integration on a single chip [86 - 90]. Nevertheless, ADCs are crucial and complete necessities in digital wireless communications as signals require digitising for base band processing. Therefore, reducing the cost is desirable.

The pipeline ADC approach is suitable for wireless communications systems in which total harmonic distortion, spurious-free dynamic range, and other frequency domain specifications are relevant. The pipeline approach provides an advantageous balance of

size, speed, resolution and power dissipation making it more suitable for portable wireless devices and has become increasingly more appealing to data converter manufacturers and their designers [91 - 94]. A typical architecture of a pipeline ADC is illustrated in Figure 6.4 [93]. Each stage of a pipeline ADC encompasses a low-resolution quantiser and provides two outputs.

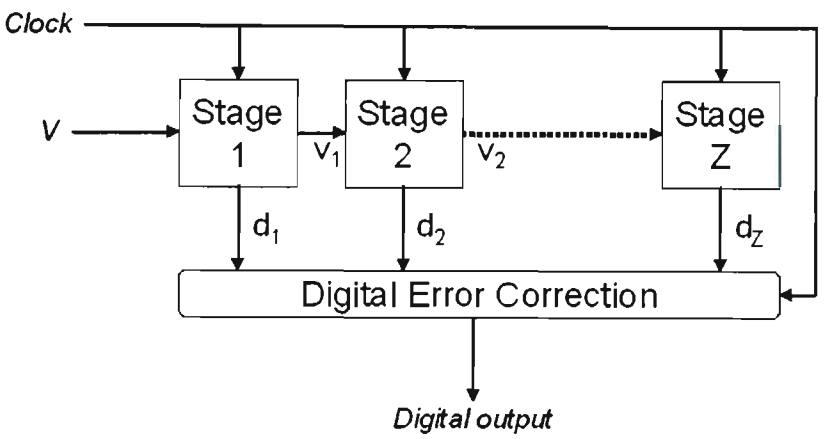


Figure 6.4 Typical pipeline ADC block diagram [93]

The first output, d_n, is a coarse resolution digital equivalent of the input voltage, and the second output is the residual voltage, v_n, which is achieved by measuring the difference between the input voltage and the voltage expected by d_n. The residual voltage is cascaded to the next stage in the chain and the digital output of each stage is processed by a digital error correction (DEC) circuit as it is a major design challenge to design an ADC with a specific resolution without calibration to combat transfer function errors. The consequent stages improve the final representation by quantising the residual voltage. All the digital outputs, d_n are composed in the DEC circuit to unite these coarse estimated values into a final higher resolution symbol of the input voltage V. The same clock signal clocks all of the stages in the pipeline chain. Formerly stage 1 produces v_1 and d_1, at this time stage 2 begins quantising v_1 while stage 1 is processing the next

input sample. This permanent dispensation of samples is the concept of '*pipelining*'. The capability of the pipeline topology makes it a high-quality candidate for high speed and low power conversions.

The details of each stage in the pipeline ADC architecture are presented in Figure 6.5 [94]. It consists of a sample and hold (S/H) amplifier, a low-resolution ADC, digital-to-analog converter (DAC), and a summing circuit with a gain amplifier. Each stage has a sub K_n bit ADC (such as a Flash ADC) to provide the digital output for that pipeline stage. A sub DAC with comparable resolution to the sub ADC is used to convert this digital output back to an analog voltage. This voltage is then subtracted from the initial sampled input, resulting in the voltage error that is scaled by the gain factor and cascaded to subsequent stages as v_n.

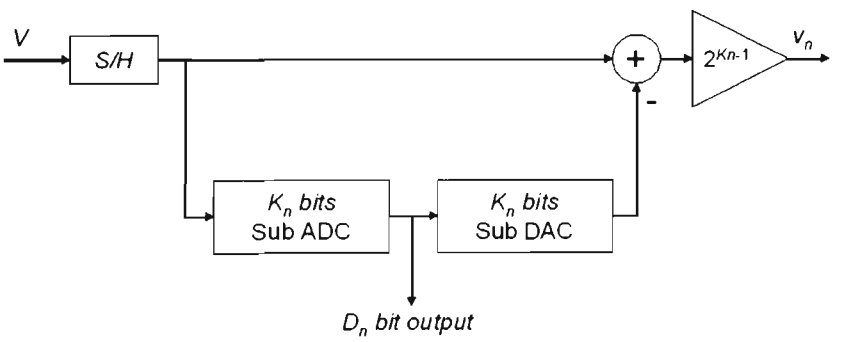


Figure 6.5 Single Pipeline ADC stage block diagram [94]

An improvement on the DEC method proposed in [95] is discussed here. Considering a 2-bit pipeline stage, a $-¼$ reference voltage (V_{REF}) offset is intentionally added to both the sub-ADC input and the sub-DAC output. With this modification, the ADC output will always be equal to or lower than the ideal output, but never above the ideal output. The error detection and correction process is similar to that in [95], except that the

correction circuit is simplified by avoiding the possibility of subtraction. A further improvement is achieved by eliminating the top comparator at ¾ V_{REF} in the sub-ADC. This takes advantage of the fact that the over ranging in the transfer function can be detected by the next stage. The final block diagram and the transfer characteristic are shown in Figure 6.6 [92]. The sub-ADC thresholds are now at ± ¼V_{REF} (note that only two comparators are required) and the sub-DAC levels are at −½V_{REF}, 0, and +½V_{REF}. Since the sub-ADC and sub-DAC only have three digital codes, this technique is often referred to as a 1.5 bit per stage converter. The overall resolution after digital error correction is performed is equal to 1 bit per stage.

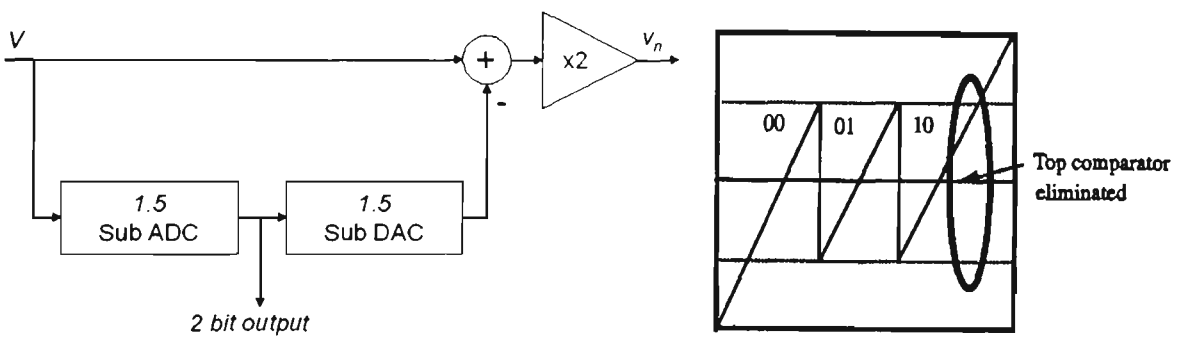


Figure 6.6 1.5 bit per stage architecture [92]
a) Modified sub-stage pipeline architecture, b) voltage transfer function

A 1.5 bit per stage, 4 bit pipeline ADC with DEC is presented in Figure 6.7 [92]. An increased number of delay stages, *D*, are necessary for the output bits that are generated early in the pipeline so that all outputs corresponding to a given input sample arrive at the DEC at the same time. The DEC then takes the outputs from the $(N+1)^{th}$ stage and adds them to the N^{th} stage outputs, with a one least significant bit (LSB) offset. If there is a carry bit, it potentially propagates all the way to the most significant bit (MSB).

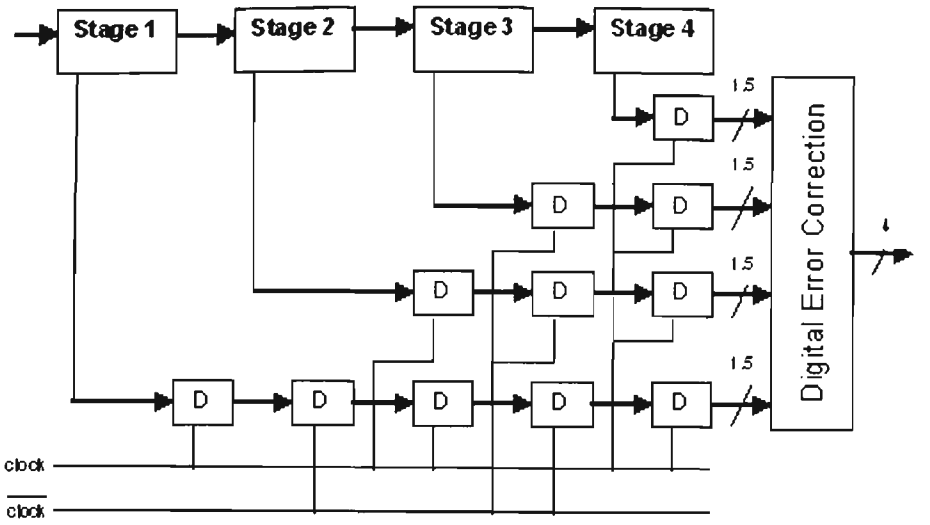


Figure 6.7 1.5 bit per stage 4 bit pipeline ADC architecture [92]

6.2.2.2 Dynamic Range Analysis

Further analysis was required to determine the minimum resolution of the ADC without affecting the noise performance of the receiver. This was achieved by performing a dynamic range analysis which describes the range of input signal levels that can be reliably measured concurrently. The relationship between the dynamic range, DR_{ADC} and the effective number of bits, N, has been investigated in [96] and is as follows:

$$DR_{ADC} = \mathbf{20} \bullet \log \mathbf{10}\left(\mathbf{2}^{N}\right) \tag{6.5}$$

Equation (6.5) yields 6.0201 decibels (dB) of dynamic range per bit, therefore is simplified to:

$$DR_{ADC} = \mathbf{6.0201} \bullet N \quad [dB] \tag{6.6}$$

To obtain the corresponding effective number of bits if the dynamic range is known, N corresponds to:

$$N = \frac{DR_{ADC}}{\mathbf{6.0201}} \tag{6.7}$$

Figure 6.8 illustrates the dynamic range analysis of the ADC with variable resolutions.

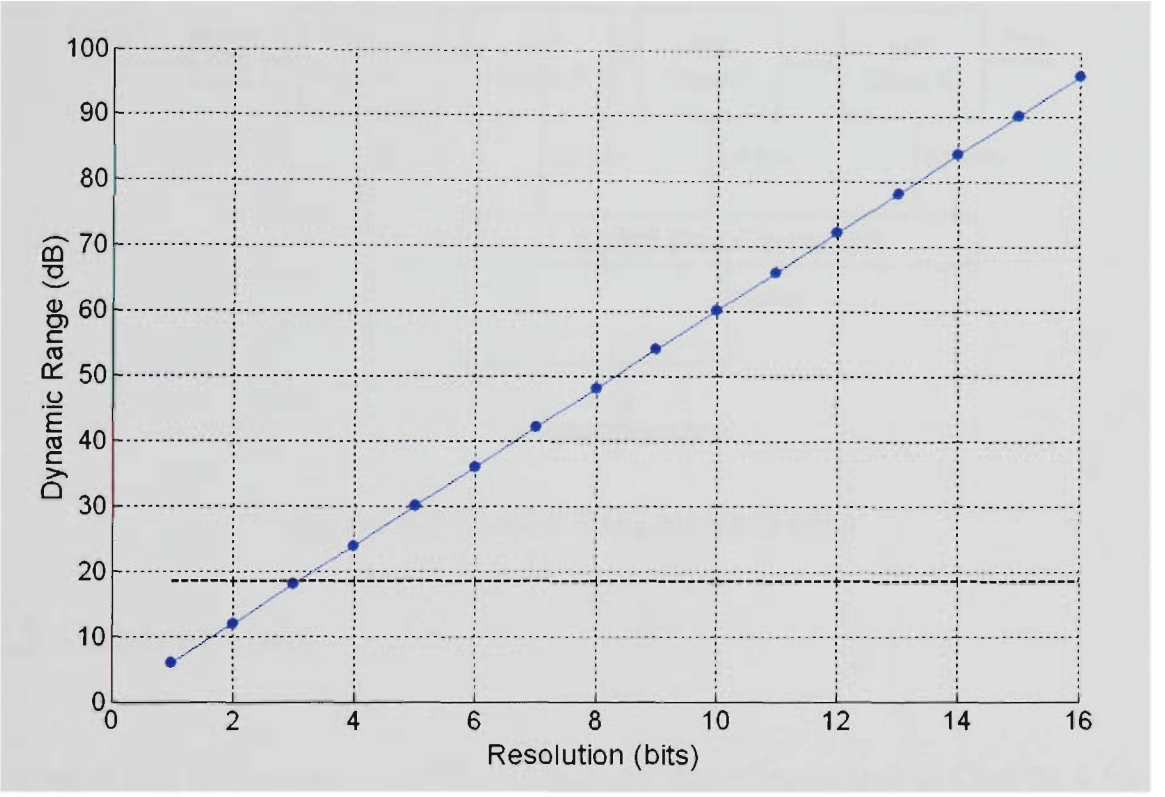


Figure 6.8 Dynamic range analysis of ADC

The dotted line corresponds to the quality of service (QoS) margin where acceptable resolutions are greater than it. The required symbol-energy to interference ratio (Es/No) of the UTRA-TDD system is twice the target Eb/No and corresponds to 6.5103 dB. An additional safety margin of 2 bits (12.0402 dB of dynamic range) to combat input noise spikes yields a QoS margin requirement of 18.5505 dB for the ADC. Therefore, acceptable resolutions are ≥ 4 bits. Figure 6.9 amends to Figure 6.3 where it illustrates the cascaded pipeline ADC, where the first stage outputs 4 bits and the consequent

pipeline ADC stages output 1 bit each (after DEC) corresponding to 16 bits maximum (thirteen ADC stages). A maximum resolution of 16 bits was chosen for extreme cases of ACI when higher resolutions might be required.

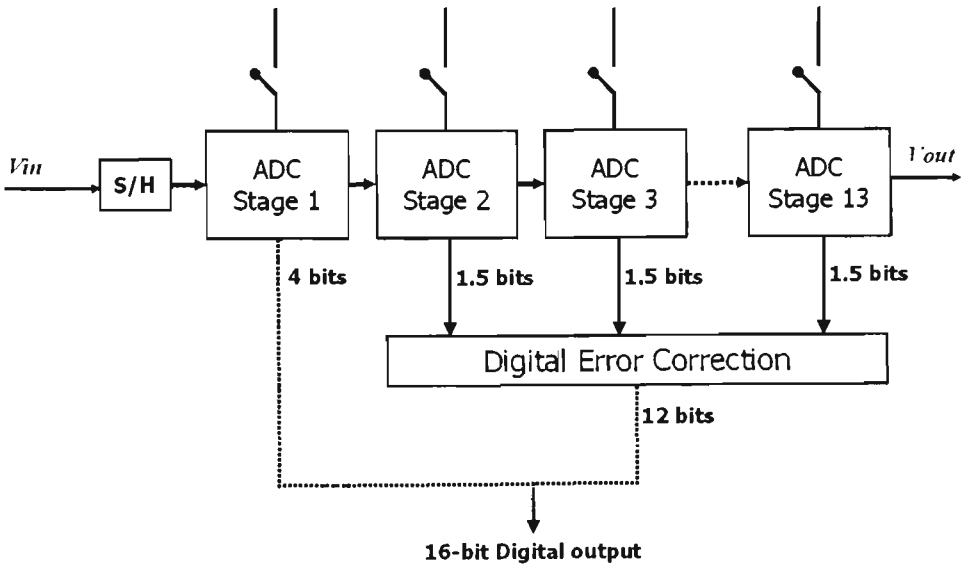


Figure 6.9 Pipeline ADC stages of RPA

6.2.3 Control Unit

The control unit is amended from the control unit design presented in Chapter 4 for the reconfigurable filter alone to allow reconfiguration of both filter and ADC simultaneously. The control unit design for the filter of the RPA is identical to that in Chapter 4 but for the exception that the ACP factor is scaled by a gain factor as derived in equation (6.3).

Once the quantisation noise, Q_n of the ADC is calculated from equation (6.4), the corresponding resolution can be derived by calculating the dynamic range. The dynamic range itself, *DR*, is the measure of the noise floor in comparison to the largest input voltage, but in this case, it is in comparison to the largest input wattage yielding:

$$DR = 10\log 10\left(\frac{Max_W}{Noise_W}\right)[dB] \tag{6.8}$$

where $Noise_W$ is the noise floor assigned to the quantisation noise derived in equation (6.4) and Max_W is the maximum input wattage defined as a sum of desired and out-of-band signal powers and is as follows:

$$Max_W = (P_{rx}^{\ i} + I_{adj}^{\ i})Dec_F \tag{6.9}$$

The summation of desired and out-of-band signal powers are scaled by the decimation factor of the filter, Dec_F as the signals have been decimated after filtering but the ADC digitises the signals while they are interpolated. The corresponding ADC resolution, N_{ADC}, is:

$$N_{ADC} = \frac{DR}{6.0201} \tag{6.10}$$

A look up table (LUT) is used to convert the calculated dynamic range from equation (6.8) to the corresponding switches to control the pipeline ADC resolution. Equation (6.10) can be used but will be inefficient as extra computational processing is required. It will not only give integer values for the required ADC resolution but floating point values as well. Therefore, LUT is still required to round the calculated resolution to an integer. The LUT to convert dynamic range to corresponding ADC switches is given in Table 6.1. The advantage of the LUT is that the ADC resolution calculations need not be calculated as the ADC switches can be found directly from the calculated dynamic range, therefore reducing the complexity. The dynamic range is given in dB units but in

implementation can be left linear for simplification, therefore disregarding the log complexity.

Table 6.1 Control Unit Look-Up Table for ADC

DR (dB)	*ADC Resolution (bits)*	*bits_switch*
$DR \leq 24.0804$	4	1000000000000
$24.0804 \leq DR \leq 30.1005$	5	1100000000000
$30.1005 \leq DR \leq 36.1206$	6	1110000000000
$36.1206 \leq DR \leq 42.1407$	7	1111000000000
$42.1407 \leq DR \leq 48.1608$	8	1111100000000
$48.1608 \leq DR \leq 54.1809$	9	1111110000000
$54.1809 \leq DR \leq 60.2010$	10	1111111000000
$60.2010 \leq DR \leq 66.2211$	11	1111111100000
$66.2211 \leq DR \leq 72.2412$	12	1111111110000
$72.2412 \leq DR \leq 78.2613$	13	1111111111000
$78.2613 \leq DR \leq 84.2814$	14	1111111111100
$84.2814 \leq DR \leq 90.3015$	15	1111111111110
$90.3015 \leq DR \leq 96.3216$	16	1111111111111

The logic in *bits_switch* correspond to the voltage source of the ADC and switches (applies voltage) a cascaded pipeline ADC stage on with a Logic '1' and vice versa with Logic '0'.

6.3 Statistical Analysis

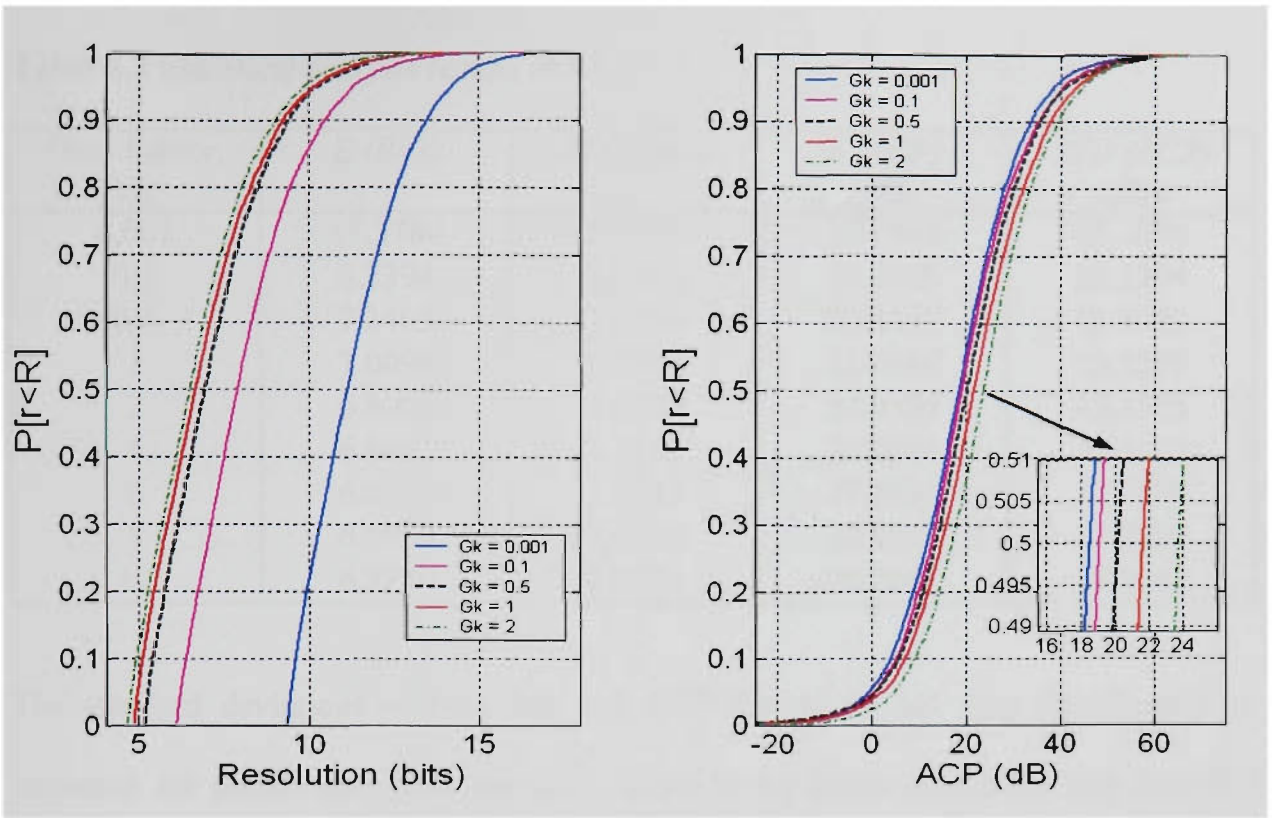
This section presents a statistical analysis of the RPA in a static simulation environment. The analysis is performed evaluate the performance of the RPA in an indoor UTRA-TDD environment whether efficient or not. The efficiency savings of the RPA can give an estimated power consumption savings in percentage compared to typical fixed structures when implemented. The simulation parameters are presented in

Table 6.2 which are similar to that in Table 3.1 for a multiple interfering cell environment.

Table 6.2 Simulation parameters for RPA analysis

Parameter	*Value*
Bit Rate	32 Kilo bits per second (Kbps)
# of users in COI	8
Max TX Power (dB milli watts (dBm))	Downlink: 10, Uplink: 4
Thermal Noise (dBm)	−102.85
Required Eb/No (dB)	3.5
Receiver Sensitivity (dBm)	−115.09
Standard deviation σ(dB)	12
Cell Radius, R (meters (m))	100
# of Interfering Adjacent Cells	7
# of users in each Interfering Adjacent Cell	8
Synchronisation factor α	Uniform random 0 to 1
Path loss exponent γ	3.0
Orthogonality Factor τ	1
Gain Factors, G_k	0.001, 0.1, 0.5, 1, 2, 4, 6, 8 and 10

Various G_k values are used to obtain a comparison between the means of ADC word lengths and filter ACP factors. A lognormal shadowing variable standard deviation of 12 dB is used as per statistical analysis of the reconfigurable filter presented in Chapter 5. Figure 6.10 illustrates the cumulative distribution functions (cdfs) of ADC word lengths and filter ACP factors by Monte Carlo simulations of equations (6.10) and (6.3) respectively. The results presented are for G_k values of 0.001 to 2. Figure 6.11 presents the results for G_k values of 4 to 8. Table 6.3 corresponds to the recorded results of the figures where the means and standard deviations are listed.



a) **b)**

Figure 6.10 Statistical analysis of RPA (G_k = 0.001 to 2)
a) ADC resolution, b) ACP Factor

A G_k of 0.001 presents the best case for the mean of ACP factors but the worst case for the mean of bits. Reason is that there is only minor quantisation noise for the ADC corresponding to a necessarily higher dynamic range. The mean of the ACP factor is lower as it has only been adjusted by a slight gain. A G_k of 10 presents the best case for the mean of the bits but the worst case for the mean of ACP factors. This case is simply the opposite as the ADC requires lower dynamic range but the filter requires a greater ACP factor to mitigate ACI. A G_k of 0.001 is not suitable as it makes the filter efficient but the ADC not efficient as the mean resolution is quite high and a reconfigurable approach has no benefit. A G_k of 10 is the opposite where the ADC benefits from the reconfigurable approach, as the mean resolution is low whereas the filter has no benefit.

Table 6.3 Statistical analysis results of RPA

Gain Factor, G_k	*E (Bits)*	*STD (Bits)*	*E (ACP)* (dB)	*STD (ACP)* (dB)
0.001	11.3780	1.5094	18.7144	12.2275
0.1	8.2394	1.6481	19.7445	12.2294
0.5	7.2403	1.6214	20.4441	12.6426
1	7.0099	1.6798	22.0846	12.7245
2	6.8000	1.6300	24.0559	12.1208
4	6.6401	1.6151	26.0641	12.1137
6	6.6120	1.6043	27.5431	12.3882
8	6.5980	1.6484	28.8137	12.2289
10	6.5280	1.6060	29.2661	12.1542

The standard deviations of both bits and ACP factors do not vary significantly as expected. *Gk* should only have dramatic effects in the means due to the fact the ACP factors are scaled by a gain. A 10 percent variation in the standard deviation of bits is recorded and 0.6108 dB variation for the ACP factors.

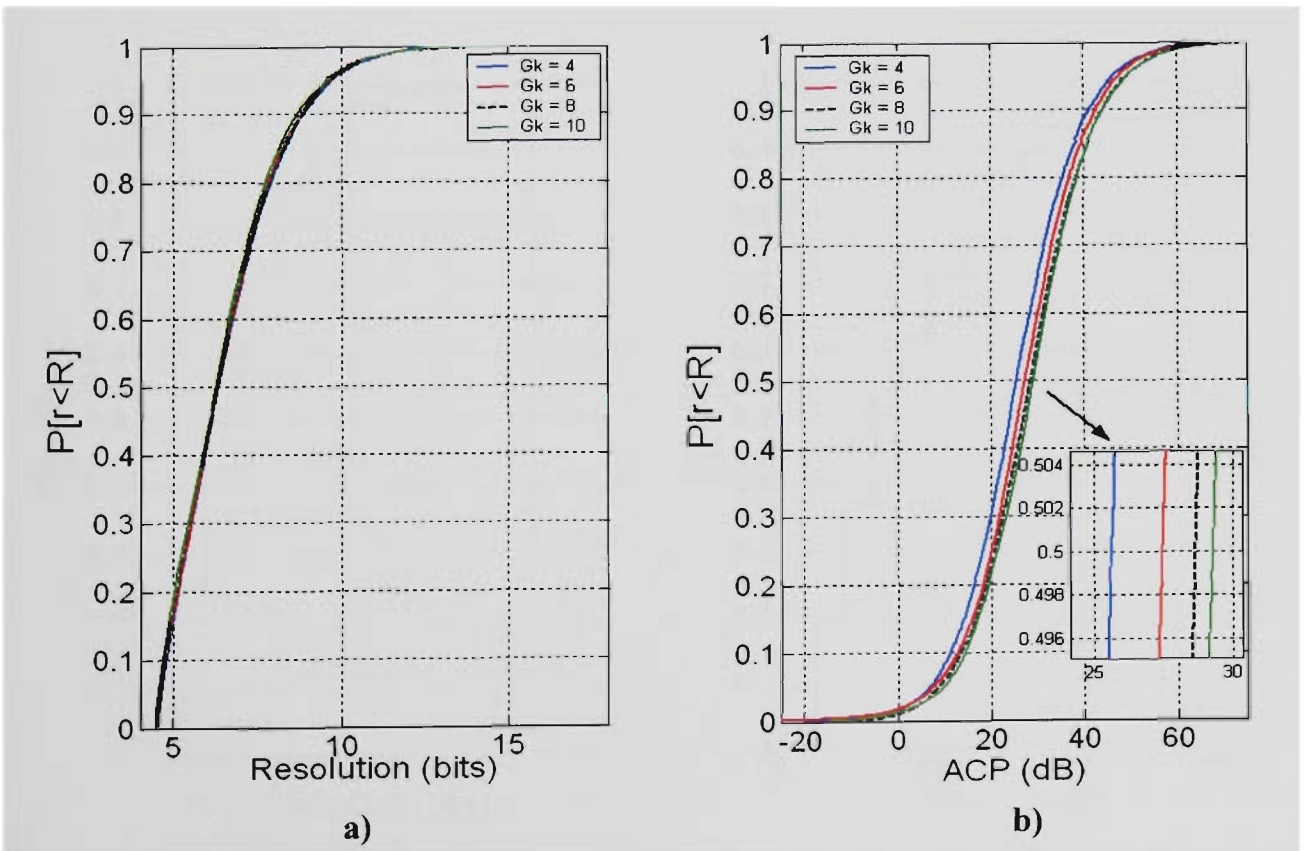


Figure 6.11 Statistical analysis of RPA (G_k = 4 to 10)
a) ADC Resolution, b) ACP Factor

A suitable G_k value is 2 as it provides a good trade off between the efficiency of the ADC and filter where the mean bits is 6.8 and the mean ACP factor is 12.1208 dB. It is also noticeable that G_k values between 0.001 and 2 improve (decrease) the mean of the ADC resolution dramatically by 40 percent whereas the mean only improves by 4 percent when increasing the G_k value from 2 to 10, therefore, there is no need to increase G_k beyond 2. It is also important to note that G_k values above 2 will result in the same mean for the bits when using the LUT in Table 6.1 and only unnecessarily decreasing the efficiency of the filter.

Figure 6.12 illustrates the statistical analysis of ADC resolution and filter lengths. The ADC resolutions were obtained using the LUT in Table 6.1 and the filter lengths were obtained using the LUT in Table 4.4. The following results are for a G_k of 2.

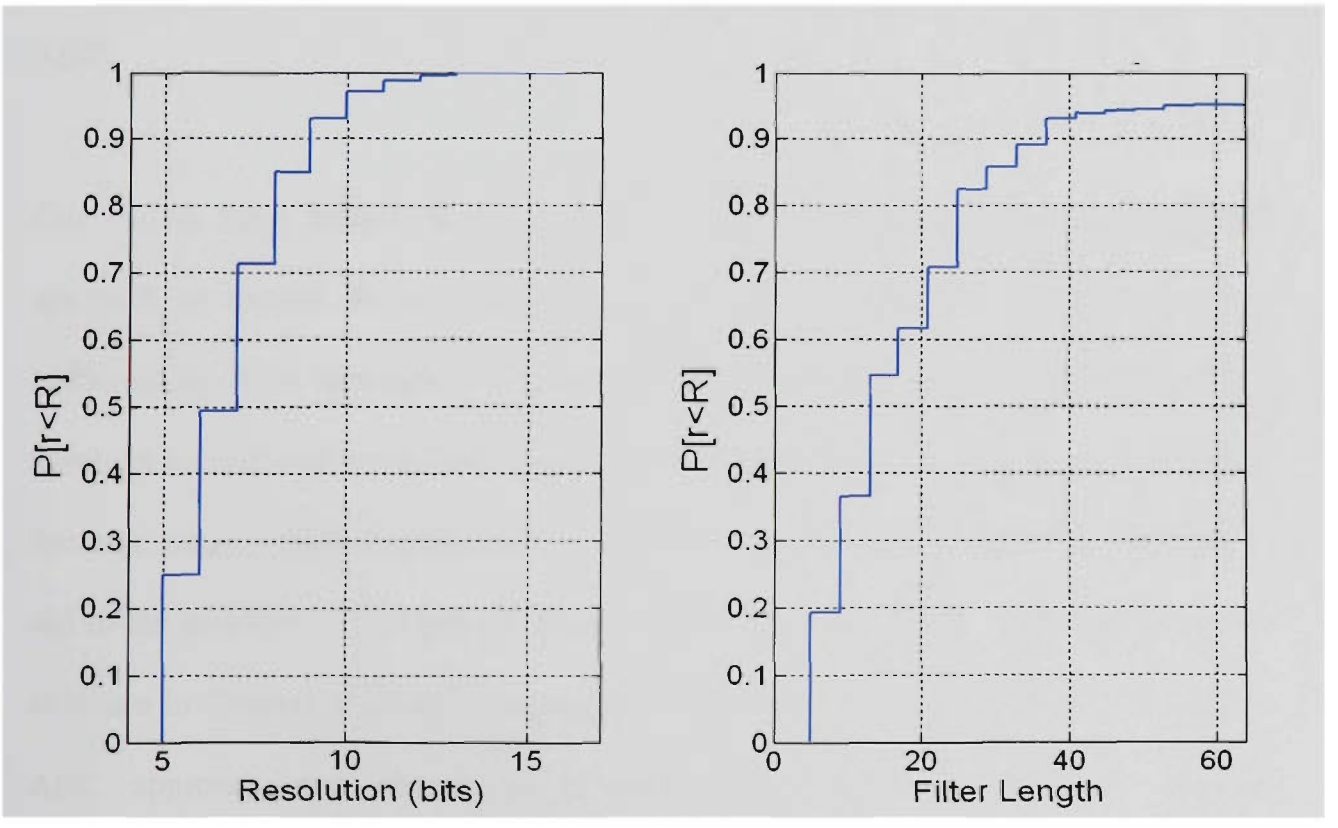


Figure 6.12 Statistical analysis of RPA
a) ADC Resolution, b) Filter Length

The average ADC resolution is 7 bits and the corresponding average filter length is 13. This corresponds to a 56 percent reduce in complexity for the ADC (when compared to a maximum ADC resolution of 16 bits) and a 73 percent reduce in complexity for the filter as compared with 3rd Generation Partnership Project (3GPP) specifications. The efficiency will correspond to major power consumption savings in both ADC and filter in the RPA.

6.4 Conclusions

This chapter has presented the design of a RPA inherent to the UTRA-TDD mobile terminal receiver. The design of the RPA is an extension of the reconfigurable digital filter presented and analysed in Chapter 4 and 5 to cater for power efficiency in the ADC.

Cost issues have further been resolved in the receiver filter by a reconfigurable approach to extend the battery life in the mobile terminal by minimising power consumption. This approach has been applied to the ADC converter where the RPA monitors in-band and out-of-band signal powers and intelligently calculates the required dynamic range, which corresponds to a certain resolution. The algorithm formulation led to the proposal of the system structure, which consists of the reconfigurable filter structure in Chapter 4 as well as a pipeline ADC with 13 cascaded stages. A pipeline ADC approach was chosen as it exhibits the right dynamics for wireless communications: high speed, low power and compactness. The first ADC stage provides a 4 bit resolution as investigated by the dynamic range analysis to calculate the

minimum word length without affecting the noise performance of the system. Consecutive ADC stages each provide 1 bit resolution totalling 16 bits. The control unit in the RPA calculates the required ACP factor for the filter and the corresponding dynamic range of the ADC and by employing LUTs it determines how many filter taps and ADC stages may need to be switched off or turned on to provide the required ACS and resolution respectively.

Trade off issues exist between the filter and ADC as various gain factors severely affect the efficiency performance of the two. A G_k of 2 was chosen as it provided the right balance of efficiency between the ADC and the filter where a statistical analysis resulted in an average ADC resolution of 7 and the average filter length of 13. This provides a 56 percent efficiency savings for the ADC and a 73 percent efficiency saving for the filter.

If the ADC implementation was available, the G_k factor can be further optimised. By relating the ADC size to power consumption and the filter size to power consumption, an optimum G_k can be selected to provide optimal minimisation in power consumption of the RPA. Currently, this cannot be achieved as the implementation of the ADC is required.

The results presented in this chapter were for a static simulated UTRA-TDD indoor environment without hysteresis protection in the control unit. Hysteresis protection as well as simulations in a dynamic environment will increase the recorded average filter length to approximately 20 (59 percent efficiency saving) following the trend of Chapter

5 between static and dynamic analysis. The average ADC word length should not be affected as the quantisation noise is calculated before the protection takes effect. Nevertheless, the RPA provides an efficient approach to tackle cost issues inherent to the UTRA-TDD mobile terminal receiver.

Chapter 7

Conclusions and Future Work

7.1 Introduction

This chapter concludes the thesis and presents the major findings of this work. It details how the work addresses the aims of Chapter 1 and presents the main conclusions that can be drawn from the findings. It also details limitations in the work in correspondence with a certain set of assumptions and outlines future research options.

7.2 Major Findings

The thesis has addressed a major design challenge of a mobile terminal receiver inherent to the time division duplex (TDD) mode of universal mobile telephone service (UMTS) terrestrial radio access (UTRA). Due to the increased interference powers in UTRA-TDD as adjacent channel interference (ACI) is experienced from both adjacent channel base stations (BS's) and mobile stations (MS's) depending on frame synchronisation and channel asymmetry, the design of root raised cosine (RRC) filters

for receiver processing has become quite costly. The reconfigurable digital filter has provided a low complex solution that both meets the specifications set by the 3rd Generation Partnership Project (3GPP) and is power efficient on the mobile battery. The reconfigurable-pipelined architecture (RPA) has further reduced the cost by applying the reconfigurable principle to the analog to digital converter (ADC) in the receiver. Reconfigurable is defined as the process of scaling the filter length and ADC resolution depending on in-band and out-of-band power ratios while satisfying the required bit-energy to interference ratio (Eb/No). The findings of this thesis; results and novel ideas have been reported in related publications in the *List of Publications* section of the thesis. Specifically, the major findings in the thesis have addressed the set aims in Chapter 1 and the following conclusions are drawn:

- ***Investigate the effects of interference in the UTRA-TDD system.***

The interference analysis was two fold. Firstly, a statistical analysis of ACI was investigated and secondly, an inter-symbol interference (ISI) analysis was performed. The analysis of ACI considered two interfering scenarios; single interfering cell and multiple interfering cells. Both scenarios demonstrated that the severity of ACI is greatly dependent on time synchronisation and channel asymmetry between adjacent cells. Non-synchronised cells for the single interfering scenario can cause between 2.1 to 2.9 times the ACI powers for various path loss lognormal shadowing variables, σ, as compared to synchronised cells. The severity is higher in the multiple interfering cells scenario yielding 2.63 to 3.65 times the ACI powers. This is dependent on cell cluster geometry and user distribution. Contrasting the ACI powers in both scenarios, the multiple interfering cells scenario can be 2.52 to 3.24 times more severe than the single interfering cell due to the addition of six interfering cells. Lognormal shadowing also

affected the severity of ACI powers. It was found that varying the standard deviation of the lognormal shadowing variable increased or decreased the mean and standard deviation of ACI powers. The single interfering cell scenario yielded mean and standard deviation variances of (1.07 decibels (dB) to 1.82 dB) and (0.22 dB to 0.85 dB) respectively for σ between 4 dB and 8 dB. Increasing σ from 8 dB to 16 dB further varies the mean and standard deviation of ACI powers by (3.84 dB to 4.68 dB) and (1.23 dB to 2.46 dB) respectively. The multiple interfering cells scenario yielded mean ACI power variations of (6.57 dB to 8.84 dB) and (0.42 dB to 1.248 dB) standard deviation variations for σ values of 4 dB to 16 dB. It is relatively apparent that the strength of ACI power is dependent on various dynamics. It is never constant and varies greatly. Therefore, it is inefficient to employ a standard fixed length receiver channel filter to mitigate ACI.

The ISI investigation revealed that decreasing the length of the receiver filter resulted in an increase of ISI. The received symbols on the constellation map showed a spread variance when the length of the filter was reduced. The spread variance tended to rise when the length of the filter was further reduced. The ISI investigation yielded acceptable filter lengths of 5, 11, 13 and $\geq$19 where the minimum is 5.

- ***Develop novel algorithms for / and design a reconfigurable channel filter for an UTRA-TDD mobile terminal receiver***

The intention of the reconfigurable filter is to provide a resolution to the cost issues associated with the TDD cellular system; primarily to increase the battery life of the mobile terminal by minimising power consumption. The architecture in real-time

observes in-band and out-of-band powers, and by employing intelligent functionality, calculates the required adjacent channel selectivity (ACS) and regulates the filter length accordingly. This reduces the power consumption as only the required multiplications and additions in the architecture will be used to process the convolution between input samples and coefficients.

Transmitter filter consideration concluded that an interpolation and decimation factor of 4 (sampling frequency of 15.36 Megahertz (MHz)) is suitable for over sampling and down sampling data. This was primarily due to the complexity tradeoffs with the transmitter filter and the analog reconstruction filter. The formulation of the algorithm for reconfigurable filtering concluded that three signals are required to determine the appropriate ACS that gives overall adjacent channel protection (ACP) factor performance. This led to the proposal of the system architecture. It consists of a number of components; finite impulse response (FIR) structure with tap switches managed by the control unit, a low complexity high pass filter (HPF) equivalent subtraction operation to obtain the ACI signal as well as signal power measurement components to provide clearly varying amplitudes of each of the three input signals to the control unit. The control unit calculates the appropriate ACP and by employing a look up table (LUT) as well as hysteresis protection and safety margins determines how many taps need be switched off or turned on to provide the required ACS.

- ***Analysis of the reconfigurable channel filter***

A static analysis of ACP factors, ACS and filter lengths was performed. The ACP factor analysis initially shows that the probability of high values is minor and that

synchronisation factors play a key role in the strength of ACP factors besides the strength of signal powers. The mean varies by a maximum of 3.535 dB when varying the synchronisation factors. The static ACS analysis employed random synchronisation factor values. The analysis revealed that the mean and standard deviation varies by a minor percentage compared with the corresponding ACP factors. The major difference between ACP and ACS is above 33 dB where the ACS powers tend to saturate due to leakage from adjacent channel in the in-band. This cannot be filtered and there is a 2.2 percent outage. The static filter length analysis concluded that the average filter length is 10.1 for UTRA-TDD, which corresponds to an 80 percent efficiency saving compared to a fixed filter length of 49 to meet 3GPP requirements.

The dynamic analysis showed that without hysteresis protection in the control unit of the system, the required Eb/No is never met and drastically reduces when the mobile velocity increases. With protection, the Eb/No is met as it ensures a higher ACP factor is used than the minimum. The dynamic analysis also revealed that the mean of ACP factors varies by 7.26 dB for with and without protection, therefore, the average filter length will increase correspondingly. The mean ACP factor recorded was 25.5 dB with hysteresis and safety margin protection. A 65 percent efficiency saving for each in-phase and quadrature filters is available compared to a fixed filter length of 49.

- ***Implementation and performance analysis of the reconfigurable filter***

The reconfigurable digital filter was hardware / software partitioned onto an application specific integrated circuit (ASIC) and digital signal processor (DSP) to achieve high performance and exhibit flexibility. Realisation considerations were discussed in terms

of resolution of the filter, number representation and coefficient quantisation effects. The ASIC was coded in Very High Speed Integrated Circuit Hardware Description Language (VHDL) – register transfer level (RTL) and synthesised in Synopsys Design Compiler using DesignWare digital libraries. Performance analysis shows that the reconfigurable digital filter consumes 790 micro watts (μW) of core dynamic power with a clock frequency of 15.36 MHz, which includes the peak power consumption of the StarCore SC110 DSP core per TDD frame. The power consumption of a fixed length 49 tap filter with yields 1.92 milli watts (mW) of power consumption concluding that an average 59 percent power and maximum 83 percent dissipation saving is available for both I and Q filters. The savings will be greater as the DSP power consumption is assumed at peak not per instruction.

- ***Design and analysis of a reconfigurable pipelined architecture***

The reconfigurable approach has been applied to the ADC converter where the RPA monitors in-band and out-of-band signal powers and intelligently calculates the required dynamic range, which corresponds to a certain resolution. The algorithm formulation led to the proposal of the system structure, which consists of the reconfigurable filter structure in Chapter 4 as well as a pipeline ADC with 13 cascaded stages. A pipeline ADC approach was chosen as it exhibits the right dynamics for wireless communications: high speed, low power and compactness. The first ADC stage provides a 4-bit resolution as investigated by the dynamic range analysis to calculate the minimum word length without affecting the noise performance of the system. Consecutive ADC stages each provide 1 bit resolution totalling 16 bits. The control unit in the RPA calculates the required ACP factor for the filter and the corresponding

dynamic range of the ADC and by employing LUTs it determines how many filter taps and ADC stages may need to be switched off or turned on to provide the required ACS and resolution respectively.

Trade off issues exist between the filter and ADC as various gain factors, G_k, severely affect the efficiency performance of the two. A G_k of 2 was chosen as it provided the right balance of efficiency between the ADC and the filter where a statistical analysis resulted in an average ADC resolution of 7 and the average filter length of 13. This provides an average 56 percent efficiency savings for the ADC and an average 73 percent efficiency saving for the filter in a static environment. If the ADC implementation was available, the G_k factor can be further optimised by relating the ADC size to power consumption and the filter size to power consumption.

7.3 Limitations and Assumptions

The results presented in this thesis are based on a series of mathematical models and computer simulations in MATLAB to provide statistical analyses. Therefore, they are question to certain limitations with a set of assumptions.

The ACI analysis was based on static simulations, which provided a good insight into the UTRA-TDD system with respect to the sensitivity and how certain system parameters affect the severity of ACI. It has, however, limitations with respect to user mobility and real time power control. It is also recognised that the performance of UTRA-TDD is greatly dependent on a certain set of parameters such as Eb/No targets,

cell structure and cluster geometry, processing gain and thermal noise. Varying these parameters will accordingly vary the results of the ACI investigation especially if the Eb/No is scaled. The power control algorithm exhibited in the investigation is 'ideal' or 'perfect'. Ideal power control in practice could not be achieved due to inaccuracies; therefore non-ideal power control algorithms will have some effect on results. Handover was also not assumed in the simulations as MS's were allocated to BS's based on minimum distance. Handover might reduce the severity of ACI, which will lead to lower filtering level requirements. In addition, the same bit rate for each user was assumed. In practice, a time slot can be fully loaded by one user with high data rate demands. This case might lead to lower filtering levels, as there is a reduced amount of intra-cell interference. All the ACI investigation was limited to one downlink time slot and only considered the +5 MHz adjacent channel. Considering other adjacent channels in the −5 MHz and ±10 MHz frequency bands will have an impact on the results.

It can be stated the results in the ACI investigation is on large specific to a certain scenario and absolute statements cannot be made that covers every scenario. Nevertheless, an excellent insight is provided. The above limitations and assumptions for the ACI interference analysis also are common to the statistical analysis (static and dynamic) of filter with respect to ACP, ACS and filter lengths as well as the static analysis of the RPA. The statistical analysis in the dynamic environment of the reconfigurable filter was based on an arbitrarily selected reconfiguration frequency of 10 ms (length of a TDD frame). Increasing the reconfiguration frequency may result in improved Eb/No (at a cost of increase power consumption), whereas lowering the reconfiguration frequency might result in poorer Eb/No where outage will be of

concern. The results would also vary if synchronisation was present between adjacent channel operators.

The implementation of the reconfigurable filter only considered the ASIC partition. The DSP partition was not implemented, as future work in section 7.4, is required with regards to power control considerations. Floor planning, layout and routing were not performed on the ASIC and the results recorded were at synthesis stage. The results do not include power consumption of input and output (I/O) pads, only the core circuitry. Including I/O pads will increase the power consumption of the filter proportionally. The power estimation of the DSP core partition assumes peak power consumption, not power consumption per instruction; therefore the power consumption is likely to decrease.

7.4 Future Work

Future work can involve system simulation with different parameters and including handover and non-ideal power control in the static ACI and filter ACP, ACS and length simulations. It will be interesting to analyse the results as they may improve. An extension to other modulation schemes such as frequency division duplex (FDD), Global Systems for Mobile communications (GSM) and even multiple-input multiple-output (MIMO) systems would be beneficial as the reconfigurable principle can be applied. The control unit algorithm and filter coefficient values will require modification according to the specifications for that system as well as the reconfiguration frequency will require adjustment to suffice the signal to noise ratio of

that system. Thus will minor amendments the reconfigurable filter can be applied to other standards or systems.

This thesis presented results for a dual ASIC and DSP implementation approach where the control unit was partitioned for a DSP. DSP's are well known for their vast flexibility as they are programmable through software and are well suited for communications applications due to their inbuilt arithmetic units such as multipliers and adders, therefore are suitable for the control unit of the reconfigurable filter. Another possible solution for the control unit would be implementation on a field programmable gate array (FPGA). Typically FPGA architectures contain LUT's and flip-flops where they are programmed to perform any function (depending on the limitations of the device) such as multiplications and additions. Nowadays, FPGA's have advanced and some vendor's produce them with embedded microcontrollers, multipliers and adders. These advanced FPGA's would be suitable for the control unit implementation as they provide better efficiency and implementation could be further investigated in future.

This thesis, given the complexity of the problem, was focused on downlink where uplink was not considered. Future work could also investigate the effect of the uplink subsystem in the base station. There are no advantages in terms of power consumption by employing this reconfigurable scheme in the base station receiver as power to the system is supplied by the mains. An advantage (subject to all the base band receiver processing is performed on a DSP) the reconfigurable filter would have in the base station would is it will reduce the instruction complexity, therefore, allowing other functions to utilise the free instructions on the DSP.

Other future work involves the full implementation of the reconfigurable digital filter and testing of the final chip. Before the full implementation can be fabricated, some further work and optimisation is required to improve the overall efficiency. The hysteresis protection used in the control unit was selected arbitrarily at 8 taps. Relating hysteresis factors with the corresponding measured Eb/No to average power dissipation of the filter would yield an optimum hysteresis factor. The filter structure may also require some optimisation in terms of decimation if the rake receiver, depending on the design, requires the signal data at the critical sampling rate. By decimating before filtering instead of decimating after filtering, the computational complexity can be reduced in the structure therefore saving power [34]. The multiplications and additions involving the filter coefficients will be performed at the critical sampling frequency instead of the over sampled frequency, thus, reducing the complexity by a factor of 4 (as the decimation factor is 4). The architecture is illustrated in Figure 7.1 [34].

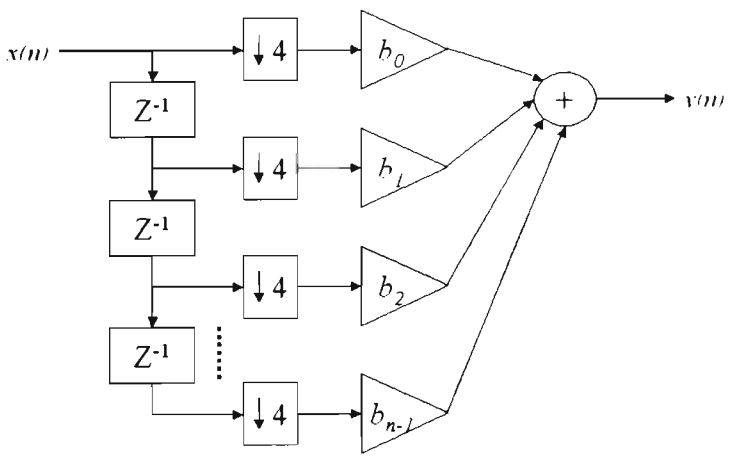


Figure 7.1 Computation efficient decimation filter [34]

Further optimisation in the control unit algorithm is required to consider downlink power control in the UTRA-TDD system. Transmit Power Control (TPC) is essential in

UTRA-TDD to bound interference levels within the system thus reducing ACI powers as well as power dissipation in the MS. Table 7.1 presents the downlink TPC characteristics. All OVSF codes within one time slot allocated to the same coded composite transport channel (CCTrCH) use identical transmission power, in case they employ identical spreading factors [97].

Table 7.1 Transmit Power Control characteristics [97]

Parameter	*Downlink TPC*
Power control rate	Variable: rate depending on slot allocation
Step Size (dB)	1, 2 or 3
Remarks	Within one time slot the powers of all active codes may be balanced to within a range of 20 dB

The downlink TPC is an inner loop signal to interference ratio (SIR) based power control method. The initial transmission power of the downlink dedicated physical channel (DPCH) is set by the network. After initial transmission the UTRA network (UTRAN) enables the TPC. The algorithm is as follows [97]:

$$\begin{aligned} &if && SIR_{measured} > SIR_{target} && TPC = "down" \\ &elseif && SIR_{measured} \leq SIR_{target} && TPC = "up" \end{aligned} \tag{7.1}$$

The SIR is measured periodically at the MS. If the measured SIR is greater than the target SIR, the MS responds to the UTRAN with the TPC command "down". When the measured SIR is less than or equal to the target SIR, the MS responds with the TPC command "up". The UTRAN may increase or decrease the transmit power of all downlink DPCHs of the radio link by a certain step size (1, 2 or 3 dB) depending on the TPC command. The transmission power is defined as the average power of the complex quadrature phase shift key (QPSK) symbols of a single DPCH before spreading. The

target SIR is set by a higher layer in the network. [97]. The SIR is identical as the Eb/No defined in equation (4.3).

Based on the downlink TPC method, a there is a conflict with the reconfigurable filter. When the UTRAN performs downlink TPC periodically, it might occur at the same time (every TDD frame) the reconfigurable filter scales the filter length. Therefore, the following two cases exist.

- If TPC = "down", the UTRAN decreases transmission power as interference may be low. The control unit of the reconfigurable filter will also decrease the filter length as interference is low but the filter length may not meet the target Eb/No as the desired transmission power will decrease by a certain step size. This is because the filter length was derived based on the transmission power before the UTRAN adjusted it by a certain step size.

- If TPC = "up", the UTRAN increases transmission power as interference may be high. The control unit of the reconfigurable filter will also increase the filter length to mitigate the interference and bring it below the ACS level but the filter length in this case may be higher than required to meet the Eb/No. This is because the UTRAN will increase the transmission power by a certain step size, which will result in unnecessary power consumption in the MS.

Future work will look at employing the downlink TPC method in the control unit of the architecture. The control unit will have the ability to calculate whether the UTRAN will

increase or decrease the desired transmission power by a certain step size in the DPCH and will ensure the calculated filter length complies with the increase or decrease in transmission power.

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Annex A

Spreading and Modulation by 3GPP

The information in this annex is directly taken from the specification document "3rd Generation Partnership Project, TSGRAN, 'Spreading and Modulation (TDD)' 3G TS 25.223, version 3.2.0, 2000".

A.1 General

In the following, a separation between the data modulation and the spreading modulation has been made. The data modulation is defined in clause A.2 and the spreading modulation in clause A.3.

Table A.1 Basic modulation parameters

Chip rate	chiprate: 3.84 Mchip/s	Low chiprate: 1.28 Mchip/s
Data modulation	QPSK	QPSK
Spreading characteristics	Orthogonal Q chips/symbol, where $Q = 2^p$, $0 <= p <= 4$	Orthogonal Q chips/symbol, where $Q = 2^p$, $0 <= p <= 4$

A.2 Data Modulation

The symbol duration T_S depends on the spreading factor Q and the chip duration T_C: $T_s = Q \times T_c$, where $T_c = \frac{1}{chiprate}$.

The data modulation is performed to the bits from the output of the physical channel mapping procedure and combines always 2 consecutive binary bits to a complex valued data symbol. Each user burst has two data carrying parts, termed data blocks:

$$\underline{\mathbf{d}}^{(k,i)} = (\underline{d}_1^{(k,i)}, \underline{d}_2^{(k,i)}, \ldots, \underline{d}_{N_k}^{(k,i)})^T \quad i = 1, 2; k = 1, \ldots, K. \tag{A.1}$$

N_k is the number of symbols per data field for the user k. Data block $\underline{\mathbf{d}}^{(k,1)}$ is transmitted before the midamble and data block $\underline{\mathbf{d}}^{(k,2)}$ after the midamble. Each of the N_k data symbols $\underline{d}_n^{(k,i)}$; i=1, 2; k=1,...,K; n=1,...,N_k; of equation 1 has the symbol duration $T_s^{(k)} = Q_k . T_c$ as already given.

The data modulation is quadrature phase shift keying (QPSK), thus the data symbols $\underline{d}_n^{(k,i)}$ are generated from two consecutive data bits from the output of the physical channel mapping procedure:

$$b_{l,n}^{(k,i)} \in \{0,1\} \qquad l = 1,2; k = 1,\ldots K; \; n = 1,\ldots, N_k; i = 1,2 \tag{A.2}$$

using the following mapping to complex symbols:

Table A.2 QPSK mapping

consecutive binary bit pattern	*complex symbol*
$b_{1,n}^{(k,i)}$ $b_{2,n}^{(k,i)}$	$\underline{d}_n^{(k,i)}$
00	+j
01	+1
10	-1
11	-j

The mapping corresponds to a QPSK modulation of the interleaved and encoded data bits $b_{l,n}^{(k,i)}$ of equation (A.1).

In case of physical random access channel (PRACH) burst type, the above definitions apply with a modified number of symbols in the second data block. For the PRACH burst type, the number of symbols in the second data block $\underline{\mathbf{d}}^{(k,2)}$ is decreased by $\frac{96}{Q_k}$ symbols.

A.3 Spreading Modulation

Spreading of data consists of two operations: Channelisation and Scrambling. Firstly, each complex valued data symbol $\underline{d}_n^{(k,i)}$ of equation (A.1) is spread with a real valued channelisation code $\mathbf{c}^{(k)}$ of length $Q_k \in \{1,2,4,8,16\}$. The resulting sequence is then scrambled by a complex sequence $\underline{\mathbf{v}}$ of length 16.

The elements $c_q^{(k)}$; k=1,...,K; q=1,...,Q_k; of the real valued channelisation codes

$$\mathbf{c}^{(k)}=(c_1^{(k)},c_2^{(k)},...,c_{Q_k}^{(k)})\ ;\ k=1,...,K;$$

shall be taken from the set.

$$V_c = \{1, -1\} \tag{A.3}$$

The $\mathbf{c}_{Q_k}^{(k)}$ are orthogonal variable spreading factor (OVSF) codes, allowing to mix in the same timeslot channels with different spreading factors while preserving the orthogonality. The OVSF codes can be defined using the code tree of Figure A.1.

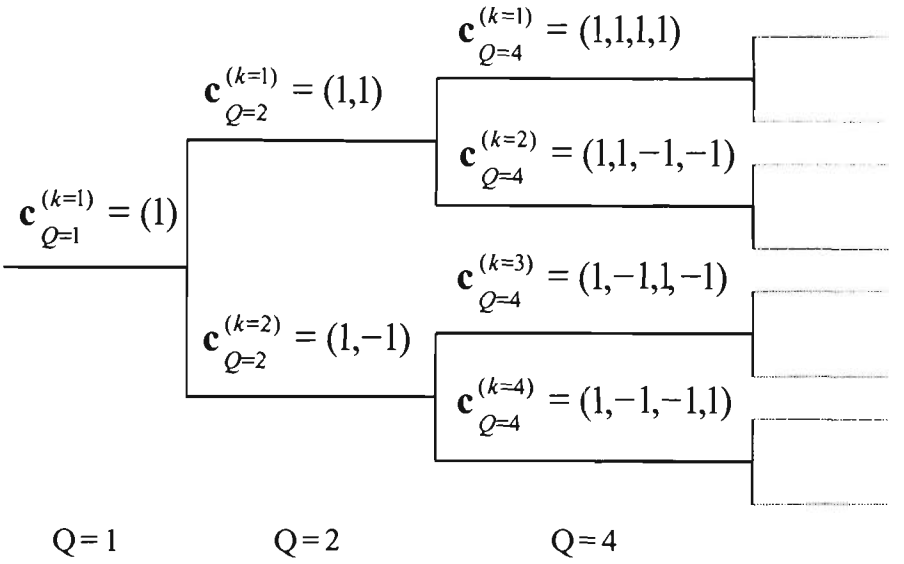

Figure A.1 Code-tree for generation of OVSF codes for Channelisation Operation

Each level in the code tree defines a spreading factor indicated by the value of Q in the figure. All codes within the code tree cannot be used simultaneously in a given timeslot. A code can be used in a timeslot if and only if no other code on the path from the specific code to the root of the tree or in the sub-tree below the specific code is used in this timeslot. This means that the number of available codes in a slot is not fixed but depends on the rate and spreading factor of each physical channel. The spreading factor goes up to Q_{MAX}=16.

The spreading of data by a real valued channelisation code $\mathbf{c}^{(k)}$ of length Q_k is followed by a cell specific complex scrambling sequence $\underline{\mathbf{v}} = (\underline{v}_1, \underline{v}_2, \ldots, \underline{v}_{16})$. The elements $\underline{v}_i; i = 1,\ldots,16$ of the complex valued scrambling codes shall be taken from the complex set

$$\underline{V}_{\underline{v}} = \{1, j, -1, -j\} \tag{A.4}$$

In equation (A.4) the letter j denotes the imaginary unit. A complex scrambling code $\underline{\mathbf{v}}$ is generated from the binary scrambling codes $\mathbf{v} = (v_1, v_2, \ldots, v_{16})$ of length 16 shown in Annex A. The relation between the elements $\underline{\mathbf{v}}$ and $\mathbf{v}$ is given by:

$$\underline{v}_i = (j)^i \cdot v_i \qquad v_i \in \{1, -1\},\ i = 1,\ldots,16 \tag{A.5}$$

Hence, the elements $\underline{v}_i$ of the complex scrambling code $\underline{\mathbf{v}}$ are alternating real and imaginary. The length matching is obtained by concatenating Q_{MAX}/Q_k spread words before the scrambling. The scheme is illustrated in Figure A.2.

The combination of the user specific channelisation and cell specific scrambling codes can be seen as a user and cell specific spreading code $\mathbf{s}^{(k)} = (s_p^{(k)})$ with

$$s_p^{(k)} = c^{(k)}_{1+[(p-1) \bmod Q_k]} \cdot \underline{v}_{1+[(p-1) \bmod Q_{MAX}]}, \quad k=1,\ldots,K,\ p=1,\ldots,N_k Q_k.$$

With the root raised cosine chip impulse filter $Cr_0(t)$ the transmitted signal belonging to the data block $\underline{\mathbf{d}}^{(k,1)}$ of equation 1 transmitted before the midamble is

$$\underline{d}^{(k,1)}(t) = \sum_{n=1}^{N_k} \underline{d}_n^{(k,1)} \sum_{q=1}^{Q_k} s_{(n-1)Q_k+q}^{(k)} \cdot Cr_o(t-(q-1)T_c-(n-1)Q_kT_c) \qquad \text{(A.6)}$$

and for the data block $\underline{\mathbf{d}}^{(k,2)}$ of equation 1 transmitted after the midamble

$$\underline{d}^{(k,2)}(t) = \sum_{n=1}^{N_k} \underline{d}_n^{(k,2)} \sum_{q=1}^{Q_k} s_{(n-1)Q_k+q}^{(k)} \cdot Cr_0(t-(q-1)T_C-(n-1)Q_kT_c-N_kQ_kT_c-L_mT_c). \qquad \text{(A.7)}$$

where L_m is the number of midamble chips.

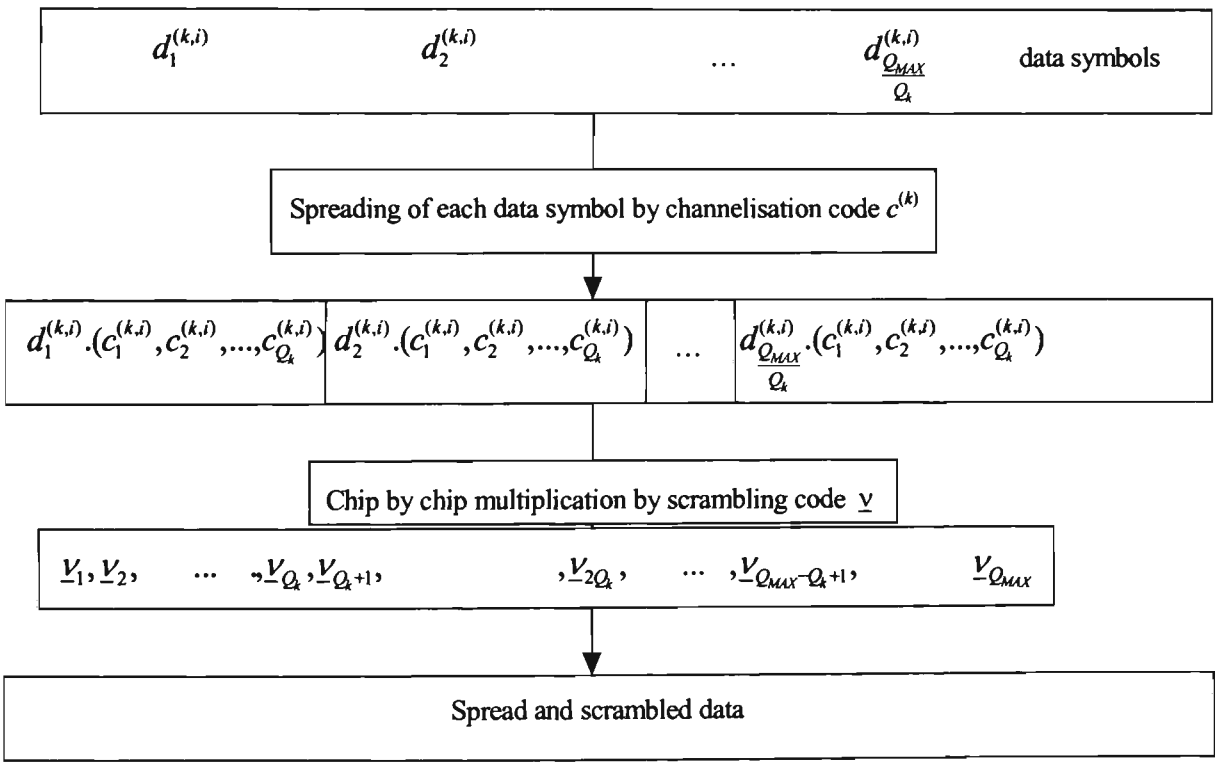

Figure A.2 Spreading of data symbols

The complex-valued chip sequence is QPSK modulated as shown in Figure A.3 below.

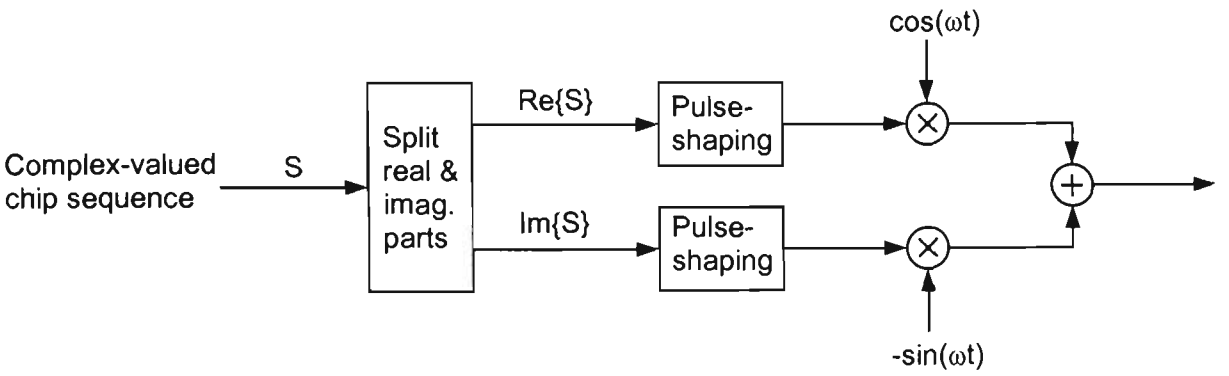

Figure A.3: Modulation of complex valued chip sequences

Annex B

Rayleigh Flat Fading Channel Model

The Rayleigh flat fading channel model used in this work is based on Clarke's model for flat fading [98]. The model describes that the statistical characteristics of the electromagnetic fields of the received signal at a mobile are derived from scattering [99]. His model assumes a fixed transmitter with a vertically polarised antenna. The mobile antenna is assumed to receive N azimuthal plane waves with random carrier phases. All of these incoming components are assumed to have an arbitrary distributed angle of arrival and equal average amplitude.

Another assumption is line of sight between the transmitter and the receiver does not exist, so that all multi path components should experience the same average attenuation. Clarke also assumed that all multi path components arrive at the same time. That is, every N arriving signal undergoes a Doppler frequency shift only. Clarke's model on flat fading has verified that the received signal at a mobile is attenuated by a Rayleigh distribution, $p(r)$, given by [99]:

$$p(r) = \begin{cases} \frac{r}{\sigma^2} e^{\left(-\frac{r^2}{2\sigma^2}\right)} & 0 \le r \le \infty \\ 0 & r < 0 \end{cases} \tag{B.1}$$

where r is the random received signal envelope, and σ^2 is defined as [99]:

$$\sigma^2 = E_0^2 / 2 \tag{B.2}$$

where E_0 is the real amplitude of the local average E-field [99]. Gans [100] derived a spectrum analysis from Clarke's work where the total received power, P_r, can be expressed as [99]:

$$P_r = \int_0^{2\pi} AG(\theta)p(\theta)d\theta \tag{B.3}$$

where $p(\theta)$ denotes the fraction of the total incoming power within $d\theta$ of the angle θ. The average received power with respect to an isotropic antenna is denoted by A and $G(\alpha)$ ia the azimuthal gain pattern of the mobile antenna as a function of the angel of arrival [99]. If the scattered signal is of carrier frequency f_c, then the instantaneous frequency, $f(\theta)$, of the received signal at angle θ is [99]:

$$\begin{aligned} f(\theta) = f &= \frac{\upsilon}{\lambda}\cos(\theta) + f_c \\ &= f_m \cos\theta + f_c \end{aligned} \tag{B.4}$$

where υ is the mobile velocity, λ is the wavelength where f_m is the maximum Doppler frequency shift. The output spectrum, $S_{E_z}(f)$, is given by [99]:

$$S_{E_z}(f) = \frac{1.5}{\pi f_m \sqrt{1 - \left(\frac{f - f_c}{f_m}\right)^2}} \tag{B.5}$$

Now that the spectrum density of the received signal can be found using equation (B.5), a simulation model can be used to determine the impact of an applied signal. The concept is based on in-phase (I) and quadrature (Q) modulation paths to produce a simulated signal with spectral and temporal characteristics [99]. Two independent Gaussian noise sources are used to produce I and Q fading branches. Using a spectral filter defined in equation (B.5) to shape the Gaussian signals in the frequency domain can accurately produce time domain waveforms of Doppler fading by using an inverse fast Fourier transform (IFFT) [99]. The following steps are used to implement the simulator [99]:

- Specify number of frequency domain points, N, to represent the maximum Doppler frequency shift and $\sqrt{S_{E_z}(f)}$.
- Compute the frequency spacing between adjacent spectral lines.
- Generate complex Gaussian random variables for each $N/2$ frequency components of the noise source.
- Construct negative frequency components of the noise source.
- Multiply the I and Q noise sources by $\sqrt{S_{E_z}(f)}$.
- Perform an IFFT to obtain time domain of length n for each I and Q signal then add the squares of each point in time.
- Finally, take the square root of the sum obtained.

Figure B.1 [99] illustrates the simulator block diagram.

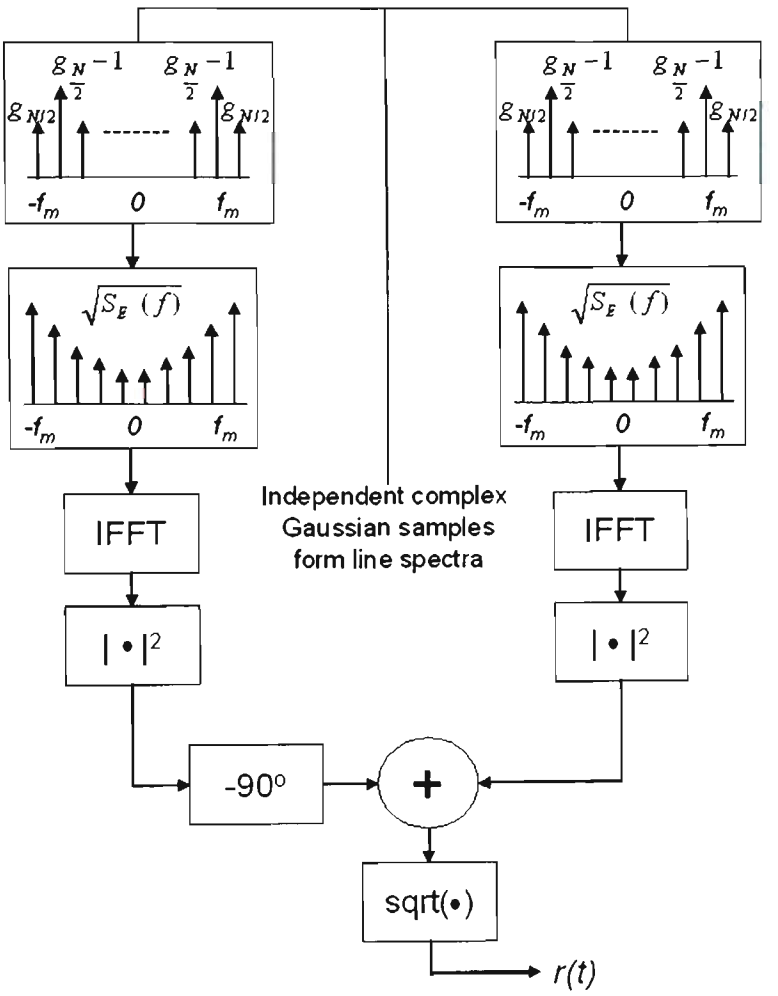

Figure B.1 Frequency domain implementation of a Rayleigh flat fading baseband simulator [99]

To apply the fading effect to a signal *x(t)*, one needs to multiply it by the generated *r(t)* derived from the simulator in Figure B.1. Figure B.2 illustrates an example of applying the fading effects on one downlink timeslot of a time division duplex (TDD) frame. The Rayleigh flat fading generator is sampled at 10 milliseconds with a Doppler frequency shift of 12.75 Hertz (Hz) (mobile velocity of 2 meters per second). The carrier frequency is set to 1912.5 Megahertz (MHz).

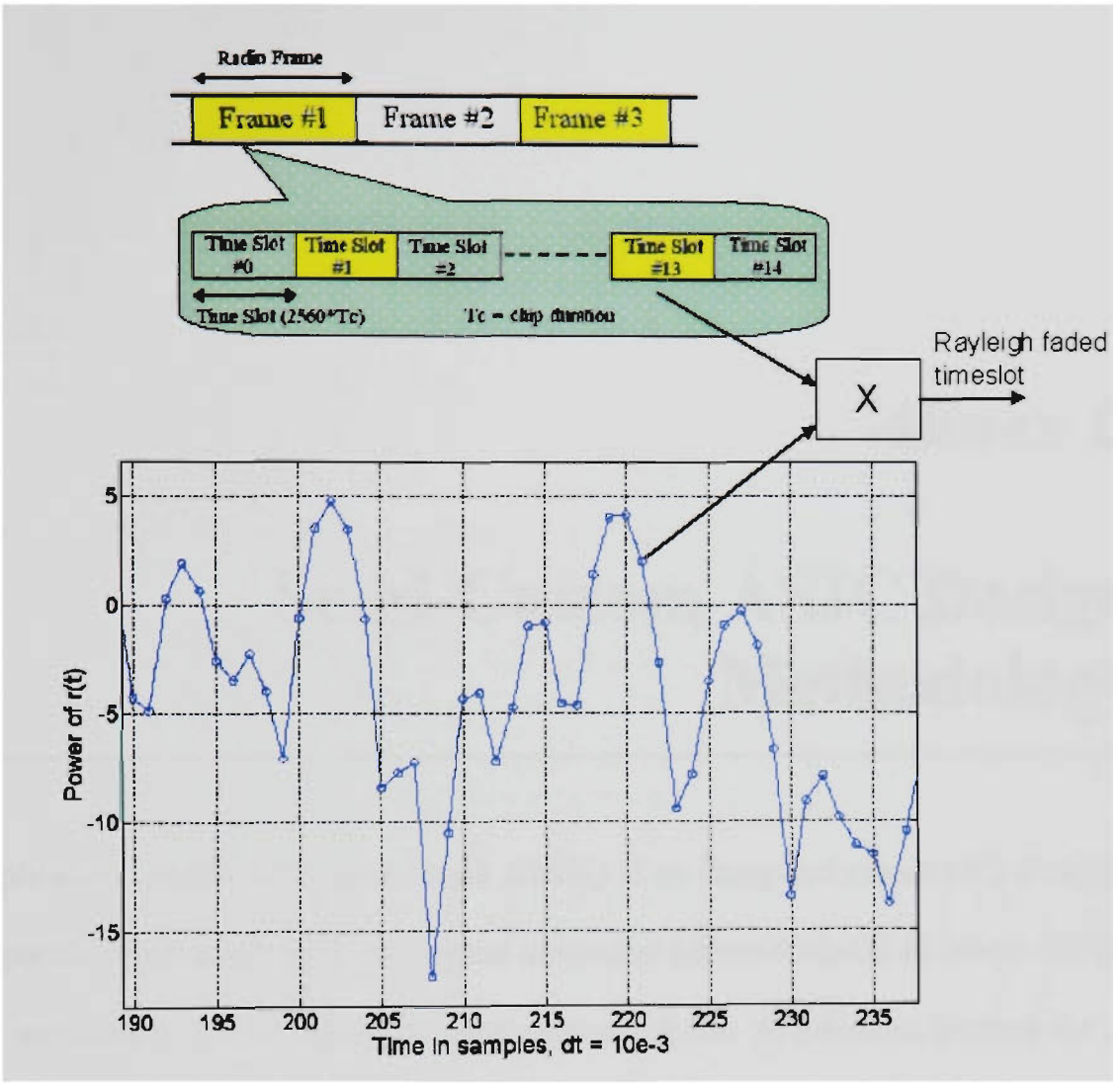

Figure B.2 Applying the effects of flat fading to a downlink time slot in a TDD frame

Annex C

Semi-Custom ASIC Design Methodology

An application specific integrated circuit (ASIC) is an integrated circuit (IC) designed for a specific application, such as wireless devices or personal digital assistants (PDA). ASICs are used in a vast variety of applications and can be pre-manufactured for an application or can be custom manufactured for a particular customer application. An semi-custom ASIC typically uses components from a "building block" library of general components such as combinational logic, custom ICs, dynamic random-access memory (DRAM) and static random-access memory (SRAM). Full custom ASICs offer higher performance and smaller die size but with the downside of increased design time, complexity and design expense whereas semi-custom ASICs provide a faster time to market.

The semi-custom ASIC design methodology used in the thesis for the implementation approach is presented in Figure C.1 [101].

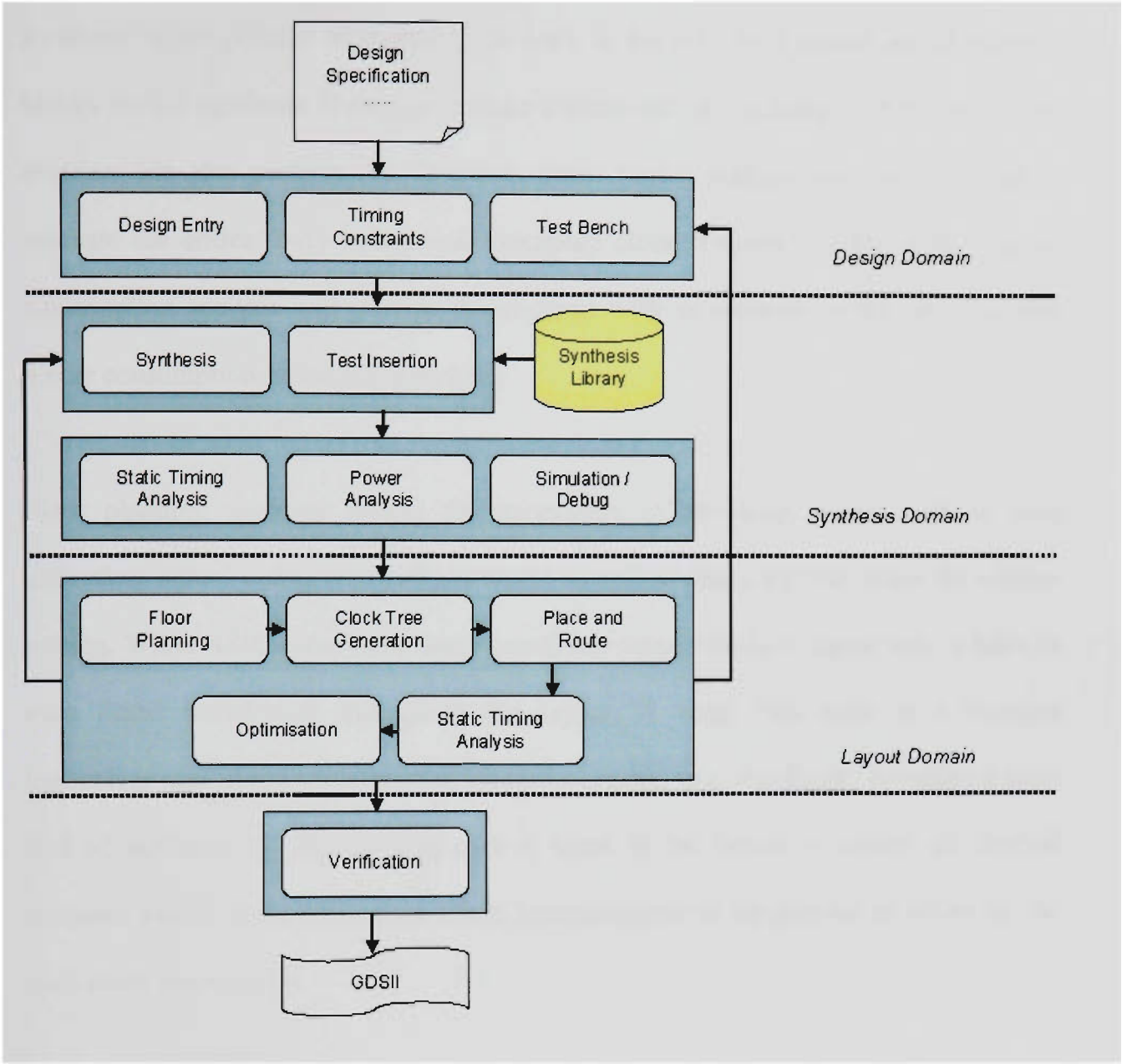

Figure C.1 Semi-custom ASIC design methodology [101]

The semi-custom ASIC design flow is as follows: Firstly, the engineer obtains a set of design specifications for the ASIC and performs the design entry. The design entry is typically register transfer level (RTL) - hardware description language (HDL) such as Very High Speed Integrated Circuit HDL (VHDL) or Verilog. A certain set of timing constraints is considered in the design and the design is simulated with a certain test bench.

Synthesis is the process of mapping the logic in the RTL to a certain set of building blocks from a synthesis library to produce a schematic of the design. At this point, the engineer can also perform test insertion. Static timing analysis can be performed to estimate the critical path delays and maximum clock frequency of the ASIC. Power consumption analysis will provide the engineer with an estimate of the core circuitry power consumption (static and dynamic).

Floor planning involves setting the parameters of the chip layout such as core utilisation, input / output (IO) pad placement as well as allocating chip space for voltage routing. When ASIC complexity (gate count) increases, the clock signal may require an even timed distribution throughout the layout. A large chip such as a wireless transceiver may contain hundreds of clocked elements (e.g. flip-flops), therefore a great deal of buffering is required and care is taken in the layout to ensure all clocked elements switch at the same time. Clock tree generation is the process of achieving the even clock distribution.

Place and route involves placing all components of the design (combinational logic, gates, memories, etc) in the core provided by the floor planning and then routing all the connections between components. Timing extraction is performed to allow the engineer to perform static timing analysis to verify if timing constraints are met. At this stage design rule checking (DRC) and layout versus schematic (LVS) is carried out to verify the design. The final stage in the design flow is the tape out where the engineer generates a file (GDSII) to send to the manufacturer foundry for fabrication.