# A Reconfigurable Analog-to-Digital Converter for a Mobile Receiver

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**Submitted in Fulfillment of the Requirements for the Degree of Doctor of Philosophy**


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*My work is dedicated to the two most important people in my life to date.*

*My wife* ***Klementina Stojcevski****, whose encouragement, support and endless love has made me the man I am today.*

*The other is my new born son* ***Stefan Stojcevski****, whose entrance on the 14th of May 2003, in this huge world has given me another reason to live.*

# TABLE OF CONTENTS

# *Declaration of Originality*

I declare that, to the best of my knowledge, the research described herein is the result of my own work, except where otherwise stated in the text. It is submitted in fulfillment of the candidature for the degree of Doctor of Philosophy in Engineering at Victoria University, Melbourne, Australia. No part of this work has been submitted for any other degree.

Aleksandar Stojcevski

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# *List of Figures*

# *List of Tables*

# *List of Abbreviations*

| | |
|---|---|
| 1GS | First Generation System |
| 2GS | Second Generation System |
| 3G | Third Generation |
| 3GS | Third Generation System |
| 3GPP | Third Generation Partnership Project |
| fF | femto-Fared |
| nV | Nano-Volts |
| μV | Micro-Volt |
| Σ – Δ | Sigma – Delta |
| ACI | Adjacent Channel Interference |
| ADC | Analog-to-Digital Converter |
| ACP | Adjacent Channel Protection |
| ASIC | Application Specific Integrated Circuit |
| ACLR | Adjacent Channel Leakage Ratio |
| AF | Averaging Filter |
| ACS | Adjacent Channel Selectivity |
| BiCMOS | Bipolar Complementary Metal Oxide Semiconductor |
| BS | Base Station |

| | |
|---|---|
| BSs | Base Stations |
| CDF | Cumulative Distribution Function |
| CDMA | Code Division Multiple Access |
| CRA | Combined Reconfigurable Architecture |
| CCI | Co-Channel Interference |
| CMOS | Complementary Metal Oxide Semiconductor |
| CCD | Charged-Coupled Devices |
| COI | Cell of Interest |
| CM | Common Mode |
| CMRR | Common Mode Rejection Ratio |
| dB | Decibels |
| DSP | Digital Signal Processing |
| DAC | Digital-to-Analog Converter |
| DNL | Differential Non-Linearity |
| DR | Dynamic Range |
| EVM | Error Vector Magnitude |
| EDA | Electronic Design Automation |
| ENOB | Effective Number of Bits |
| Eb/No | Bit Energy to Interference Ratio |
| FDD | Frequency Division Duplex |
| FFT | Fast Fourier Transform |
| FWR | Full Wave Rectifier |
| GSM | Global System for Mobile Communications |
| GHz | Giga-Hertz |
| INL | Integral Non-Linearity |

| | |
|---|---|
| ISI | Inter Symbol Interference |
| ICs | Integrated Circuits |
| IOS | Input Offset Storage |
| LSB | Least Significant Bit |
| LNA | Low Noise Amplifier |
| LPF | Low Pass Filter |
| LUT | Look Up Table |
| MSB | Most Significant Bit |
| MS | Mobile Station |
| MSs | Mobile Stations |
| MSPS | Mega-Sample per Second |
| MHz | Mega-Hertz |
| MAC | Multiply-Accumulate |
| MIMO | Multiple Input Multiple Output |
| NMOS | Negative-Channel Metal Oxide Semiconductor |
| $N_f$ | Nyquist Frequency |
| OOS | Output Offset Storage |
| OSVF | Orthogonal Variable Spreading Factor |
| PCS | Personal Communications System |
| PDC | Personal Digital Communications |
| PSRR | Power Supply Rejection Ratio |
| PMOS | Positive-Channel Metal Oxide Semiconductor |
| $Q_n$ | Quantisation Noise |
| QPSK | Quadrature Phase Shift Key |
| RRC | Root Raised Cosine |

| | |
|---|---|
| RF | Radio Frequency |
| rms | Root Mean Square |
| SNDR | Signal-to-Noise plus Distortion Ratio |
| SNR | Signal-to-Noise Ratio |
| SAR | Successive-Approximation Register |
| S/H | Sample-and-Hold |
| SFDR | Spurious Free Dynamic Range |
| SDD | Space Division Duplex |
| SoC | System on a Chip |
| TDD | Time Division Duplex |
| THD | Total Harmonic Distortion |
| TDMA | Time Division Multiple Access |
| UMTS | Universal Mobile Telecommunication System |
| UTRA | UMTS Terrestrial Radio Access |
| VLSI | Very Large Scale Integration |
| WCDMA | Wideband Code Division Multiple Access |

# *List of Publications*

**Journal Publications**

[1] A. Stojcevski, H. P. Le, J. Singh, A. Zayegh, "Flash ADC Architecture", IEE Journal, Electronic Letters, Vol. 39, No. 6, pp. 501-502, 2003.

[2] A. Stojcevski, R. Veljanovski, J. Singh, M. Faulkner, A. Zayegh, "A Low Cost Reconfigurable Architecture for UMTS Receiver" Accepted for publication in IEICE Transactions on Communications, Special Issue, 2003.

[3] A. Stojcevski, J. Singh, A. Zayegh, "An Efficient ADC for an UTRA-TDD System", Accepted for publication in Advances in Modeling & Simulation, AMSE Journal, 2003.

[4] A. Stojcevski, J. Singh, A. Zayegh, "Low Power, High Speed, 4-Stage Pipeline Analog-to-Digital Converter", Accepted for publication in Advances in Modeling & Simulation, AMSE Best-of-Book Journal, 2002.

[5] A. Stojcevski, R. Veljanovski, J. Singh, A. Zayegh, M. Faulkner, "Reconfigurable Architecture for UTRA-TDD System", IEE Journal, Electronic Letters, Vol. 38, No. 25, pp. 1732-1733, 2002.

[6] A. Stojcevski, J. Singh, A. Zayegh, "Design Implication of the Building Block Components of Pipeline Analog-to-Digital Converters", Accepted for publication in Advances in Modeling & Simulation, AMSE Journal, 2002.

## Conference Publications

[1] A. Stojcevski, R. Veljanovski, J. Singh, A. Zayegh, "Highly Efficient Reconfigurable Architecture of UTRA-TDD Mobile Terminal Receiver", Proceeding of IEEE, International Symposium on Circuits and Systems, ISCAS'03, Bangkok, Thailand, pp. II-45 – II-48, 2003

[2] A. Stojcevski, R. Veljanovski, J. Singh, A. Zayegh, "A Real-Time Reconfigurable Pipelined Architecture with Advanced Power management for UTRA-FDD", Proceeding of IEEE, PIMRC, 2003.

[3] A. Stojcevski, H. P. Le, J. Singh, A. Zayegh, "Low Cost Flash Architecture for Pipeline ADC", Proceeding of IEEE, 10th International Conference on Mixed Design of Integrated Circuits and Systems, MIXDES, Poland, 2003.

[4] A. Stojcevski, J. Singh, A. Zayegh, "Scalable Pipeline Analog-to-Digital Converter for UTRA-TDD Mobile Station Receiver", Proceeding of IEEE, International Conference on Semiconductor Electronics", ICSE'02, Penang, Malaysia, pp. 370-374, 2002.

[5] A. Stojcevski, J. Singh, A. Zayegh, "Modified Flash ADC Architecture with Reduced Power and Complexity", Proceedings of the 4th International Conference on Modeling and Simulation, MS'02, Melbourne, Australia, pp. 169-173, 2002.

[6] A. Stojcevski, J. Singh, A. Zayegh, "A Reconfigurable Analog-to-Digital Converter for UTRA-TDD Mobile Terminal Receiver", Proceeding of IEEE, Midwest Symposium on Circuits and Systems, MWSCAS, Tulsa, Oklahoma, USA, pp. II-613 – II616, 2002.

[7] A. Stojcevski, J. Singh, A. Zayegh, "Quantisation Error Analysis for an ADC used in UTRA-TDD Mobile Station Receiver", Proceedings of the 2nd ATCRC Telecommunications and Networking Conference, Fremantle, Australia, pp. 2002. (*Best Paper Award*).

[8] A. Stojcevski, J. Singh, A. Zayegh, "Performance Analysis of a CMOS Analog to Digital Converter for Wireless Telecommunications," Proceedings of IEEE, ISIC-2001, Devices & Systems, Marina Mandarin, Singapore, pp. 59-62, 2001.

# *Abstract*

The evolution of new telecommunication standards is increasingly leaning towards higher data transmission rates. The boundaries between digital and analog signal processing is impending closer to the antenna, therefore aiming for a software-defined radio solution. In terms of analog-to-digital converters (ADCs) of mobile terminal receivers, this indicates higher sample rate, lower power consumption and higher resolution. With comparison to other ADCs, the pipelined ADC architecture has most successfully covered the wide resolution limits and data rate requirements of these terminal receiver architectures. However, even though fix word-length pipeline ADC architecture could be a suitable device for the mobile receiver, it still has a distinct disadvantage when it comes to power consumption. ADC optimisation techniques could lower power consumption but will not reduce it to its most efficient level.

A solution in theory is to use minimum resolution, and still meet the performance requirements of the Universal Mobile Telephone Service (UMTS) Terrestrial Radio Access (UTRA) – Time Division Duplex (TDD) receiver specified by the 3rd

Generation Partnership Project (3GPP). To achieve this, in-band and out-of-band signal powers need to be measured. The ADC then intelligently chooses the amount of resolution required to ensure the out-of-band signal is below a certain tolerance level and the Signal-to-Noise Ratio (SNR) is met. This scheme will reduce power consumption, as it only utilises the required resolution as compared to traditional fixed complexity architectures. To solve this, a more complex receiver ADC design and implementation is required, which will have a significant impact on battery life in the mobile terminal. Taking advantage of the software-defined radio theory, a solution can be achieved using digital signal processing and application specific integrated circuit (ASIC) technologies that can meet the performance and system needs of high speed and low cost devices. A DSP can interface with an ASIC and control the ADC resolution dependant on in-band and out-of-band power ratios, making the design a reconfigurable solution. This could be embedded on a single chip to provide System-on-a-Chip (SoC) solution.

In this thesis, the requirements of ADC of the mobile receiver architecture are studied and analysed using the system specifications of the 3$^{rd}$ Generation (3G) Wideband Code Division Multiple Access (WCDMA) standard. From the standard and limited performance of the building blocks, constraints at circuit design level and block level, within the design of the pipeline ADCs are drawn. At the circuit level, topologies for the most important components of the pipeline ADC have been developed and analysed. These include a sample-and-hold (S/H) circuit and a dynamic comparator.

The emphasis of the thesis is based on the reconfigurable properties of the pipeline ADC, to be used within the mobile receiver. A reconfigurable 4-bit to 16-bit, 15.36-MS/s embedded CMOS pipeline ADC, optimised for low-power direct conversion receiver has been designed. The research was further extended by making the Root Raised Cosine (RRC) filter, also part of the mobile receiver, scalable, in order to observe what effect this would have on the reconfigurable ADC. The final results indicate and justify the design of a reconfigurable architecture as compared to a fixed topology.

**Keywords:** analog integrated circuit, analog-to-digital conversion, reconfigurable architecture, direct conversion receiver, pipelined analog-to-digital converter, mixed-signal circuits.

# Chapter 1

# *Introduction*

## 1.1 Foreword

With the explosive growth of wireless communication system and portable devices, the power reduction of integrated circuits has become a major problem. In applications, such as personal communication system (PCS), cellular phone, camcorders and portable storage devices, low power dissipation, hence longer battery lifetime is a must. An example for low power application is a wireless communication system. With the rapid growth of internet and information-on-demand, handheld wireless terminals are becoming increasingly popular. (eg. UPS and FeDex handheld pad for package delivery.) With limited energy in a reasonable size battery, minimum power dissipation in integrated circuits is necessary. Many of the communication systems today utilise digital signal processing (DSP) to resolve the transmitted information. Therefore, between the received analog signal and DSP system, an analog-to-digital converter (ADC) interface is necessary. This interface achieves the digitisation of received

waveform subject to a sampling rate requirement of the system. Being a part of communication system, the ADC also needs to adhere to the low power constraint.

## 1.2 Motivation for the Thesis

Wireless communication standards, like the Universal Mobile Telecommunication System (UMTS), is evolving towards higher data rates, therefore permitting more services to be provided. High data rates imply wide bandwidths, while a continuously growing complexity of the modulation schemes. The desire for more efficient terminal receivers push the boundary between analog and digital signal processing closer to the antenna, thus aiming for a software defined radio. These two trends set the specifications of the ADC in a radio receiver, the ultimate goal being a receiver with an ADC directly sampling signals at the radio frequency (RF). However, this would require an ADC with a sampling rate in the order of the RF input frequencies, which can rise to numerous giga-hertz (GHz), and a dynamic range capable of handling signals with nano-volt (nV) amplitudes in the presence of strong interferers. To accomplish higher levels of integration, the direct conversion receiver is used, as shown in Figure 1.1.

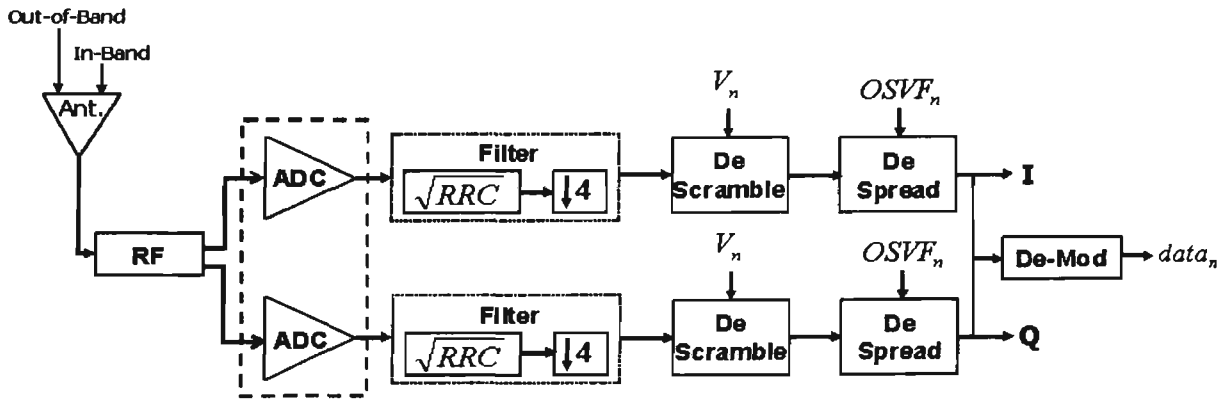



Figure 1.1: Direct conversion receiver architecture.

In the direct conversion receivers, analog channel selection filtering and variable gain amplifiers relax the dynamic range requirement, and thus the resolution, of the ADCs. The desired channel is also around zero frequency, which indicates a small sampling linearity requirement and low sample rate. As the direct conversion receiver architecture is almost exclusively used in the mobile terminal, the power dissipation is a significant design constraint. Depending on the receiver architecture, analog filtering and gain control range, for ADCs of such receiver, a resolution of 4-16 bits is required. Furthermore, the ADC can be incorporated with either analog or digital parts of a receiver, which states the technology of the ADC.

The most capable wide-band ADC architecture, covering a good combination of wide resolution and sample rate range that can be applied in radio receivers is the pipeline architecture. Pipeline architecture can contain numerous low-resolution stages operating concurrently on different samples. Any number of stages can be cascaded to give the required resolution. Pipeline ADCs can operate with supply voltages beneath 1-V, have a great prospective for low power, and can be fabricated with Complementary Metal Oxide Semiconductor (CMOS), bipolar Complementary Metal Oxide Semiconductor (BiCMOS) or bipolar processes.

## 1.3 Objectives of this Research

The specific objectives of this research are listed below.

- Review of different ADC architectures
- Design and simulation of the most critical components of the pipeline ADC
    - Sample-and-Hold circuit

- Comparator circuit

- Design, implementation and analysis of the sub-ADC (modified-flash ADC) used within the pipeline ADC.
- Development of algorithms for the reconfigurable ADC in UMTS terrestrial radio access (UTRA) – time division duplex (TDD) system.
- Design, implementation and analysis of the reconfigurable ADC architecture with fixed RRC filter length.
- Analysis of the reconfigurable ADC architecture with a scalable RRC filter.

## 1.4 Design Methodologies & Techniques

The primary limitations or disciplines, which one needs to research in order to develop a successful reconfigurable ADC are Microelectronic Circuits and Mixed Signal Design. Knowledge of these disciplines is required in order to analyse and develop algorithms capable of extracting information about the complexity, dynamic range and power efficiency of the ADC. CMOS technology has been chosen to design this ADC. The main advantage of CMOS over NMOS and bipolar technology is the much lower power dissipation.

Unlike the negative-channel metal oxide semiconductor (NMOS) or bipolar circuits, a CMOS circuit has very little static power dissipation. Power is only dissipated in case the circuit actually switches on. This allows integrating many more CMOS gates on an integrated circuit (IC) than in NMOS or bipolar technology, resulting in much better performance.

The proposed methodology and techniques to accomplish the aims of this research are:

- *Design and Implementation of analog-to-digital converter architectures:* Two different types of analog-to-digital converters were designed and simulated. The two converter circuits include a modified-flash conversion method, and pipeline converter circuits. The modified-flash ADC was used as a sub-ADC within the pipeline topology. The pipeline ADC was chosen over various other existing architectures, due to the fact that it offers a great combination of high speed, low power consumption, and low complexity, which is extremely suitable for the design of this ADC. Design and simulation was performed using Electronic Design Automation (EDA) tools. Performance was measured on complexity, dynamic range, and power consumption.

- *Statistical Analysis of the UMTS system:* Algorithms for the reconfigurable ADC in UTRA-TDD were developed. The algorithm intelligently calculates the required word lengths depending on the desired and interference signal powers and ensures that the specified system signal-to-noise ratio (SNR) of 3.5 dB is met.

- *Design and Implementation of the reconfigurable ADC architecture with fixed filter length:* The designed pipeline ADC architecture was modified to be made reconfigurable. A control-switching unit was also designed and implemented to switch between different stages of the pipeline topology.

- *Effect of a scalable RRC filter on the Reconfigurable ADC:* The reconfigurable ADC was further researched with the RRC filter within the terminal receiver this

time being scalable. The effect on the ADC with this scalable filter was statistically analysed.

## 1.5 Originality of the Thesis

The objective of this research is to design and implement a low power, reduced complexity, reconfigurable ADC for a mobile terminal receiver. The word length (bits) of the reconfigurable ADC depends on the amount of interference experienced at certain times. When adjacent channel interference (ACI) is low, the required number of word length (bits) are reduced, which leads to lower power consumption.

A control unit is responsible for the decision making property depending on the ACI level. This is desirable in battery-powered terminals to increase talk and standby times. Figure 1.2 shows the alterations made to the standard mobile receiver to accommodate this reconfigurable philosophy. A UTRA system was chosen to demonstrate the power saving capabilities of this architecture.

UMTS includes two duplex modes, frequency division duplex (FDD) and TDD. In UTRA-FDD, the uplink and downlink transmissions use two separated radio frequency bands. In UTRA-TDD, uplink and downlink transmissions are carried over same radio frequency by using synchronised time intervals. Time slots in the physical channel are divided into transmission and reception part. Information on uplink and downlink are transmitted reciprocally.

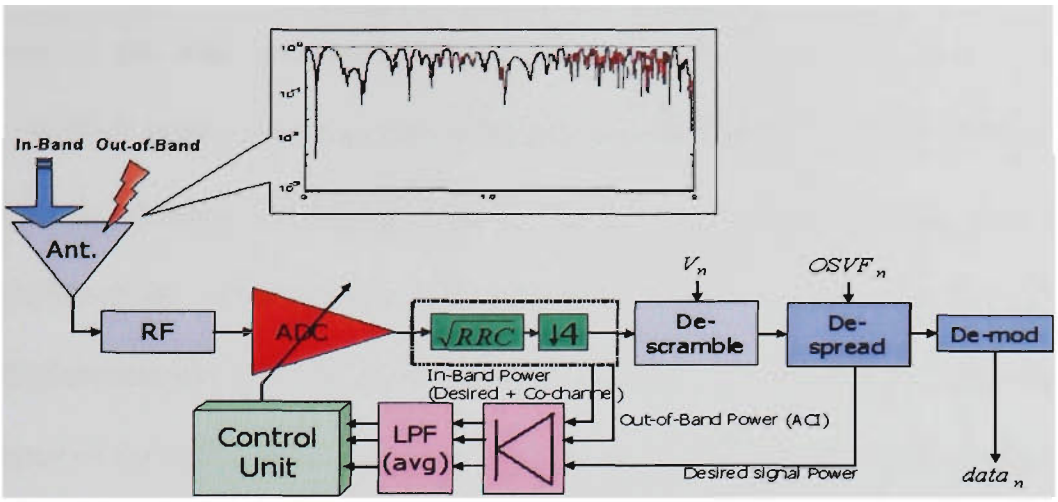



Figure 1.2: Mobile Terminal Receiver with Reconfigurable Properties

Requirements and optimisation of the pipeline ADCs, at the schematic and layout levels, have been tackled to meet the uneven specifications of this application. Although the reconfigurable architecture has been designed according to the specifications of the UTRA-TDD application, it can be applied to various mobile standards by altering the word length values and the controlling code of the ADC.

## 1.6 Thesis Organisation

The thesis is organised into seven chapters. Following the thesis overview, chapter 2 is split into two parts, where the first part reviews the different ADC topologies and their applications with a greater emphasis dedicated to the pipeline ADC. A survey of state-of-the-art ADCs is given in terms of the physical limitations of power consumption, sample rate, and accuracy. Due to the fact that the designed reconfigurable ADC will be applied to the UTRA-TDD mode, therefore the second part of this chapter presents an overview of this duplex. Chapter 3 presents design techniques of the building block components of the pipeline ADC architecture used in the reconfigurable topology with its most essential parameters. The proposed design topologies for these essential

components are also presented and analysed. Design of the sub-ADC, which is a modified-flash architecture together with noise and probability analysis of this design, is presented in chapter 4. Chapter 5 firstly looks at the system design and algorithm formulation of the reconfigurable ADC with a fixed filter length, followed by the design and implementation of this novel ADC. A statistical analysis to demonstrate the efficiency of the ADC, which in effect justifies the design of the reconfigurable ADC, is also presented in this chapter. Emphasis is on the minimisation of power consumption. The chapter is concluded with the design of the control unit, which is the key component for the reconfigurable ADC architecture. The effect of the scalable RRC filter on the reconfigurable ADC is presented in chapter 6. This chapter also presents some characteristics of the scalable RRC filter. The thesis conclusions with future work are presented in chapter .7.

# Chapter 2

# *Literature Review*

## PART I

### 2.1 Analog-to-Digital Converters

ADCs are vital crossing points in mixed-signal systems. With the fast growth in semiconductor technology and scaling of devices, digital circuits have achieved both low power consumption and high speed. This inclination has numerous blows on the mixed-signal integrated circuits (ICs). First, ever more operations are performed by digital circuits rather than by analog. Second, the speed of the ADC boundary needs to scale with the speed of the digital circuits in order to fully exploit the advantages of the complex technologies. Third, the performance and cost make it desirable to accomplish the high levels of integration on a single chip.

#### 2.1.1 Introduction

Most published literature about ADCs, which come close to the specifications and constrains mentioned in section 2.1 of this chapter are bipolar integrated circuits [1-6].

The high speed and wide dynamic range of these circuits owes to the use of open-loop precise building blocks, including low offset comparators. CMOS ADCs, by contrast tend to use closed-loop auto zeroed comparators in quantisers resolving 4-bits or more. Due to these reasons, it is difficult for these circuits to manage the speed of a bipolar ADC. In one basic way, it can be stated that the ADC is the entrance bridge to the digital domain. ADCs generally succumb into groups that essentially classify their basic modes of operation.

This literature review is divided into two parts. Part I compares key characteristics of the five most popular ADCs, and demonstrates their limitations in speed and accuracy. Higher level of emphasis is directed towards the characteristics and design of the pipeline ADC. Part II of the literature review describes the application of the pipeline ADC, for the UTRA-TDD environment.

## 2.1.2 Direct Conversion ADCs

Out of the five techniques, which will be analysed, one of the fastest is direct conversion, better known as "flash" conversion ADC, shown in Figure 2.1. ADCs based on this architecture are particularly fast and perform their conversion directly. The disadvantage of this design is that it requires complex analog design to handle the large number of devices involved [7]. The operation of this topology is as follows:

The resistor network sets the reference levels for the conversion. The outputs of the comparators will be in one state when the input voltage is below the reference and in the other state when the input voltage is above the reference. A change of input voltage usually causes a change of state in more than one comparator output. These output

changes are combined in an encoder logic unit that produces a parallel N-bit output from the converter.

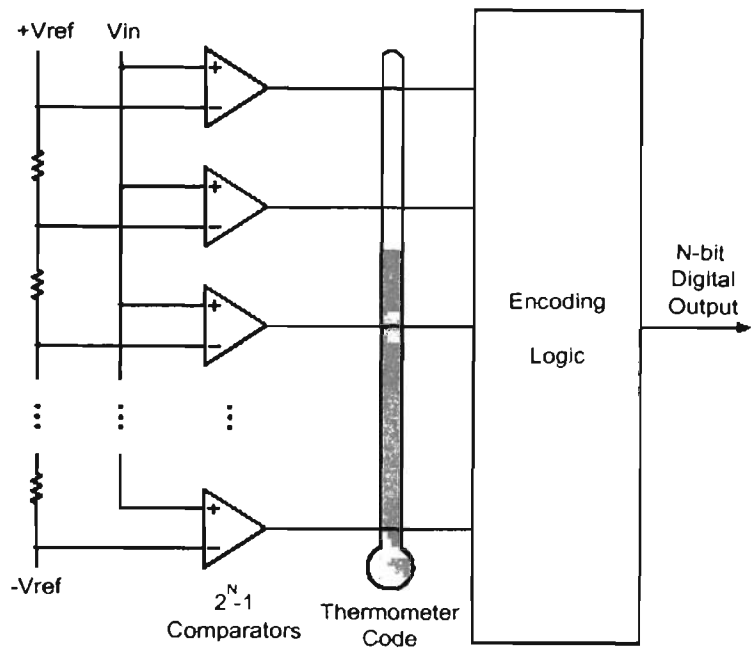



Figure 2.1: ADCs based on the direct-conversion architecture [7].

Even though flash converters are the fastest types available, their resolution is constrained by the available die size and by the large number of comparators used. Their cyclic structure demands accurate matching between the parallel comparator sections, due to the fact that any inequality can cause static inaccuracy such as a magnified input offset voltage. Flash ADCs also come up with sporadic and erratic outputs known as "sparkle codes". Sparkle codes have two major sources [8]:

- Metastability in the $(2^N - 1)$ comparators.
- Thermometer-code bubbles.

Incompatible comparator delays can revolve logic 1 into logic 0 or logic 0 into logic 1, causing the emergence of so-called "bubbles". Due to the fact that the ADC's encoder

cannot sense this error, it generates an out-of-sequence code that also appears as an output "spark". Another concern with flash ADCs is the area of the die, which is nearly seven times larger for a 6-bit flash converter than for an equivalent pipelined analog to digital converter. In further contrast to the pipeline design, the flash converter's input capacitance can be six times higher and its power dissipation twice as high [9].

### 2.1.3 Successive-Approximation ADCs

The successive-approximation register (SAR) conversion, also known as bit-weighing conversion, utilises a comparator to weigh the functional input voltage with the output of an N-bit digital-to-analog converter (DAC). Using the DAC output as a reference, this process approaches the final result as a sum of N weighing steps, in which each step is a single-bit conversion [10]. The first step stores the DAC's most significant bit (MSB) in the SAR, and then compares that value with the input. The comparator output is supplied to the DAC as a correction before the next comparison is performed, as shown in Figure 2.2. Clocked by logic control circuit, the SAR continues this weighing and shifting method until it completes the least significant bit (LSB).

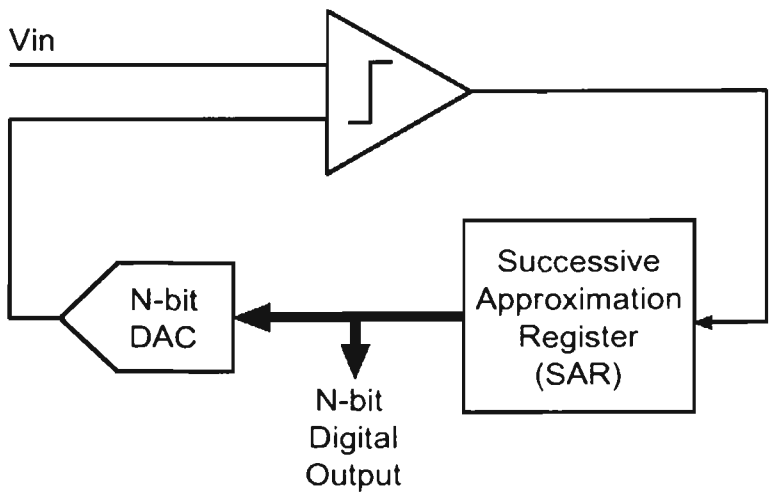



Figure 2.2: Typical successive approximation ADC [8].

As each bit is established, it is latched into the SAR as part of the ADC's output. SAR converters consist of a comparator circuit, a DAC circuit, a SAR, and a logic controller. This type of conversion methods can sample at low data rates of only up to 1 Mega-Samples-Per-Second (MSPS), use low supply current in the order of a few micro amps, low power consumption of approximately 2mW and offer the lowest production cost in the range of AUD$15 to AUD$600. The disadvantage of these designs is that their analog design is demanding and time consuming.

## 2.1.4 Integrating ADCs

Integrating ADC technique, also known as dual-slope or multi-slope data converter, is amongst the most popular converter types available. The standard dual-slope converter, shown in Figure 2.3 [8, 11, 12], has two main sectors, which include a circuit that attains and digitises the input, producing a time-domain interval, and a counter that converts the result into a digital output code.

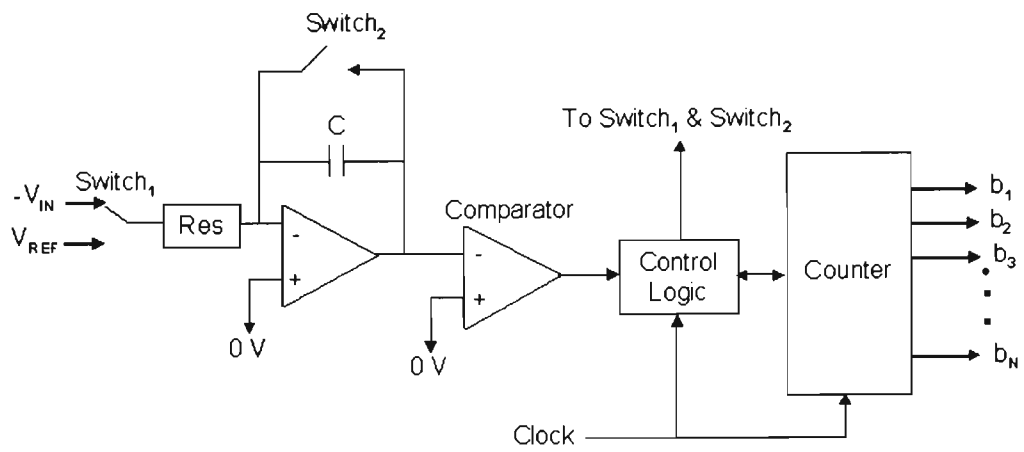



Figure 2.3: Dual-Slope Integrating ADC [8]

The dual-slope converter utilises an analog integrator with switched inputs, a comparator, and a counter. The input voltage is integrated for a fixed time interval ($T_{CHARGE}$) that commonly corresponds to the maximum count of the internal counter, as shown in Figure 2.4. At the conclusion of this interval, the device resets its counter and applies an opposite-polarity to the integrator input. With this opposite-polarity signal functional, the integrator "de-integrates" until its output accomplishes zero. At this stage, the counter is stopped and the integrator is reset. Charge that has been achieved by the capacitor within the integrator during the first integrating/charging interval $\left(\frac{T_{CHARGE}}{|V_{REF}|}\right)$ must equal that lost during the second, de-integrating/discharging interval $\left(\frac{T_{CHARGE}}{|V_{REF}|}\right)$. Under this condition the binary output is proportional to the ratio of these time intervals.

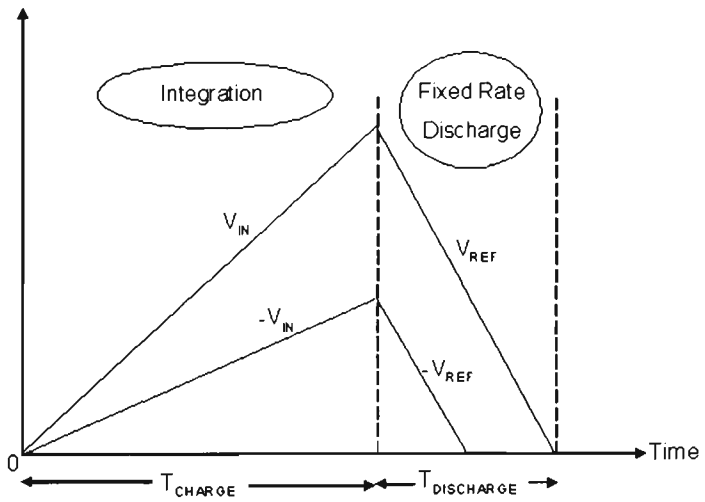



Figure 2.4: Timing relationships for a dual-slope integrating ADC [8].

Integrating ADCs are particularly slow devices with low input bandwidth. However, their ability to reject high frequency noise and fixed low frequencies, for example 60Hz, makes these converters very useful in noisy environments [12].

## 2.1.5 Sigma-Delta (Σ-Δ) ADCs

Sigma-delta (Σ-Δ) converters, also known as over-sampling converters have a reasonably plain arrangement. They consist of a sigma-delta modulator, which is then connected to a digital decimation filter, as shown in Figure 2.5 [14]. The modulator, whose architecture is similar to that of a dual-slope ADC, includes an integrator and a comparator with a feedback loop that contains a 1-bit DAC [13-15]. This internal DAC is basically a switch that connects the comparator input to a reference voltage. The Σ-Δ analog-to-digital converter also contains a clock that provides appropriate timing for the modulator and digital filter [16, 17].

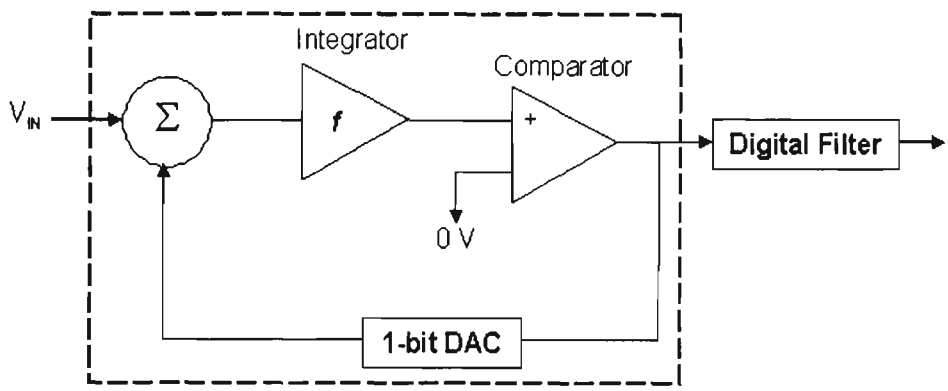



Figure 2.5: Sigma-delta converter [14].

Low-bandwidth signals applied to the input of a Σ-Δ ADC are quantised with very low resolution (1-bit), but require sampling frequencies greater than 2 MHz. Combined with digital post-filtering, this over-sampling reduces the sampling rate to about 8 kHz and increases the ADC's resolution to 16 bits or higher. Even though this type of ADC is slower than the other described above, the standard of this converter has urbanised a sturdy position in the ADC market.

The Σ-Δ ADC offers three main advantages:

- Low-cost, high-performance conversion
- Integrated digital filter
- Digital Signal Processor (DSP) compatibility for system integration [14].

### 2.1.6 Pipeline ADCs

Due to the fact that pipeline ADCs provide an optimum balance of size, speed, resolution, power dissipation, these ADCs topologies have become progressively more eye-catching to data converter manufacturers and their designers [18-21]. Also known as sub-ranging quantisers, pipeline ADCs consist of several consecutive stages, each containing a sample-and-hold (S/H) amplifier, a low-resolution ADC, DAC, and a summing circuit that includes an amplifier to provide gain.

Applications for pipeline ADCs include communication systems, in which total harmonic distortion (THD), spurious-free dynamic range (SFDR), and other frequency domain specifications are relevant [8, 22-24]. Another application of the pipeline ADC is charged-coupled devices (CCD) based imaging systems, in which favorable time-domain specifications for noise, bandwidth, and fast transient response promising quick settling. Pipeline ADCs are also used in data-acquisition systems, in which time and frequency domain characteristics (i.e., low spurs and high input bandwidth) are both important [25, 26].

### 2.1.6.1 Standard Architecture of Pipeline ADC

A standard architecture of a pipeline ADC is shown in Figure 2.6 and is discussed in [27-33]. Each stage in the ADC comprises of a low-resolution quantiser. The $n^{th}$ stage provides 2 outputs, the first output being $d_i$, which is a coarse resolution digital representation of its input voltage. The variable $d_i$ is an integer value which varies from 0 to $(2^{Kn} - 1)$, where $K_n$ is the resolution of the $n^{th}$ stage.

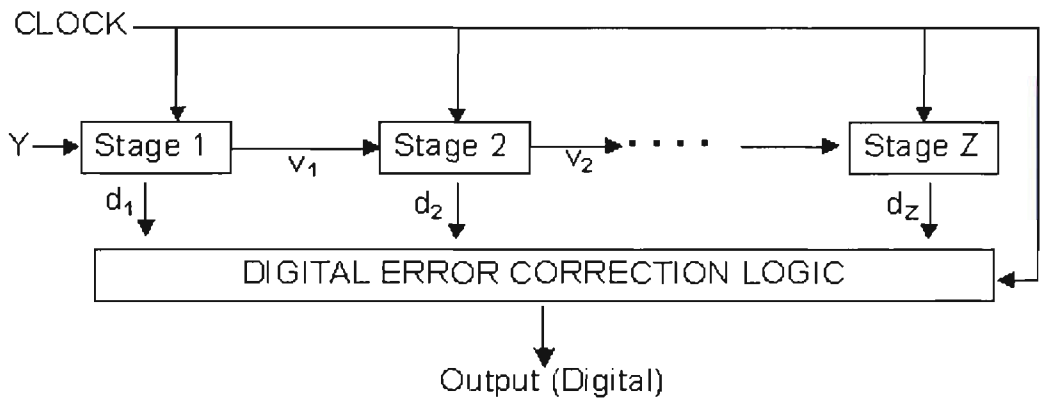



Figure 2.6: Standard Pipeline ADC block diagram [33].

The second output is the residual voltage, $v_n$, obtained by measuring the difference between the input and the voltage expected by $d_n$. This residual voltage is passed onto the next stage in the pipeline chain and $d_n$ is sent to the digital correction logic circuit. Consequent stages try to improve the final representation by quantising the residual voltage. All the $d_n$'s are composed in the digital correction logic, which is used to unite these coarse estimated values into a final higher resolution symbol of $Y$. The same clock signal clocks all of the stages in the pipeline chain. Formerly stage 1 produces $v_1$ and $d_1$, at this time stage 2 begins quantising $v_1$ while stage 1 is processing the next input sample. This permanent dispensation of samples is the concept of 'pipelining'. The competence of the pipeline topology makes it a high-quality candidate for high speed

and low power conversions. A one stage pipeline ADC block diagram is illustrated in Figure 2.7 and is discussed in several papers [34-37]. A S/H amplifier is employed at the input of each pipeline block. Each stage has a sub $K_n$-bit ADC to provide the digital output for that exact stage. A sub-DAC with comparable resolution to the sub-ADC is utilised to convert the digital output back to an analog signal.

The analog signal is then subtracted from the initial sampled input, resulting in the voltage error, $f_n$. The consequential residual error $f_n$ is balanced by a gain factor and sent to the following stage as $v_n$. The gain usually has a value of $(2^{Kn}-1)$, which depends on the resolution of that particular stage. The gain factor is applied to scale the residual to the full operating scale for the next stage. Choosing the gain as a power of two extensively abridges the digital correction logic. Contravening the high-resolution conversion into stages with low resolution has advantages and disadvantages. An important advantage is a high conversion rate. Using pipeline block stages also saves significant area, resulting in cost savings on silicon. If area is not a concern, more stages can be added to acquire higher resolution.

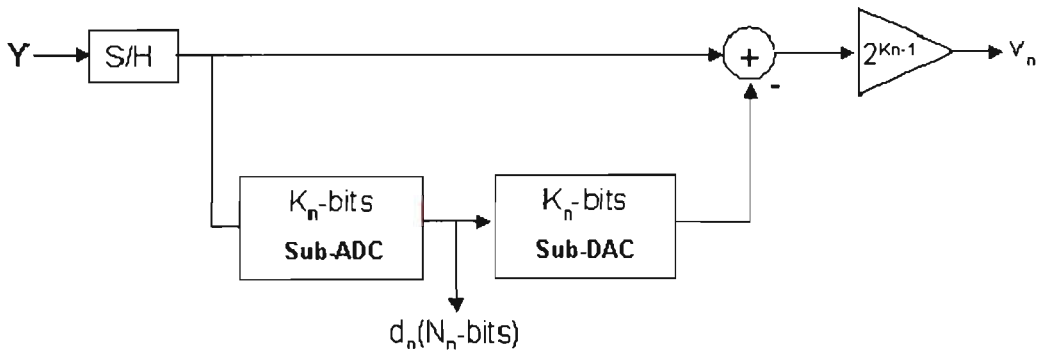



Figure 2.7: Single Pipeline stage block diagram [37].

## 2.1.6.2 Two-Stage Pipeline ADC Structure

To construct a two-stage pipeline ADC, two low-resolution ADCs could be used. Figure 2.8 shows an $A$-bit converter with an input $Y$ and outputs $d$ and $f$. The digital output representation of the ADC converter is provided by $d$, where $f$ represents the residual error of the conversion.

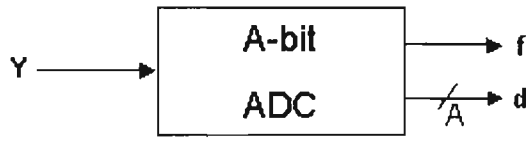



Figure 2.8: $A$-bit ADC [38].

The input range is assumed to be limited to $|Y| \leq R_V$, so that the quantisation period ($E_Q$) for this $A$-bit ADC is $E_Q = \frac{2R_V}{2^A}$, where $R_V$ is reference voltage. The digital output $d$ ranges from 0 to ($2^A$ – 1). For a mid-step ADC, the average input voltage, that can produce an output $d$, is given by $E_Q\left(d - \left(2^{A-1} - 1\right)\right)$. The input voltage $Y$ can be represented here by [38]:

$$Y = \left[d - \left(2^{A-1} - 1\right)\right] \cdot \left[\frac{2R_V}{2^A}\right] + f \tag{2.1}$$

where $|Y| \leq R_V$.

Since the $A$-bit converter is of a mid-step design the residual error $f$ can be kept small. For an ideal ADC, the error is restricted to $|f| \leq \frac{E_Q}{2}$. Due to design and course of action limitations, in practice the error will surpass these boundaries, and a more practical

assumption would be $|f| \leq E_Q$. If $f$ is available, a second ADC can be used to recover the output by quantising this error.

A $B$-bit converter is connected at the output of the $A$-bit converter, as in Figure 2.9.

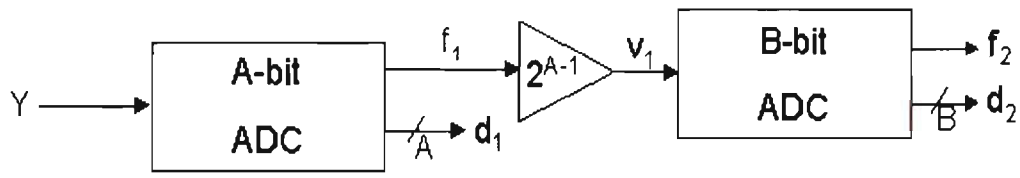



Figure 2.9: Two-stage Pipeline ADC [38]

A gain factor is selected to make $|v_1| < R_V$. Equation 2.1 can be written for the $B$-bit converter as,

$$v_1 = \left[d_2 - \left(2^{B-1} - 1\right)\right] \cdot \left(\frac{2R_V}{2^B}\right) + f_2 \tag{2.2}$$

where $|f_2| < E_B = \frac{2R_V}{2^B}$.

However, since $v_1 = 2^{A-1} \cdot f_1$, therefore,

$$f_1 = \left[d_2 - \left(2^{B-1} - 1\right)\right] \cdot \left(\frac{2R_V}{2^{B+A-1}}\right) + \left(\frac{f_2}{2^{A-1}}\right) \tag{2.3}$$

Using Equation 2.1, the $A$-bit converter output can be represented by [38]:

$$Out = \left[d_1 - \left(2^{A-1} - 1\right)\right] \cdot \left(\frac{2R_V}{2^A}\right) + f_1 = \left(d_1 2^{B-1} - \left(2^{B+A-2} - 2^{B-1}\right)\right) \cdot \left(\frac{2R_V}{2^{B+A-1}}\right) + f_1 \tag{2.4}$$

By merging Equations 2.3 and 2.4, a term for the input $Y$ and the quantised outputs can be attained as [38]:

$$Out = \left[d_1 2^{B-1} + f_2 - \left(2^{B+A-2} - 1\right)\right] \cdot \left(\frac{2R_V}{2^{A+B-1}}\right) + \frac{f_2}{2^{A-1}} \tag{2.5}$$

The expression for $Y$ in Equation 2.5 is in effect Equation 2.1, except it is written for a single ($B$+$A$-1)-bit converter. By combining the two ADCs, a higher resolution approximation of the input is obtained. The preferred digital output from Equation 2.5 is given by $d = d_1 \cdot 2^{B-1} + d_2$. The output $d$ computation is carried out in the digital correction logic of the topology. The quantisation period of the combined converter is $E_{Q(B+A-1)} = \frac{2R_V}{2^{B+A-1}}$. While $|f_2| \le \frac{2R_V}{2^A}$, the maximum error for the combined result is restricted by $\left|\frac{f_2}{2^{A-1}}\right| \le \frac{2R_V}{2^B \cdot 2^{A-1}} = E_{Q(B+A-1)}$. The operation of the digital correction is to calculate the final $d$ for each sample by adding up all the stage outputs, $d_n$. From the $A$-bit and $B$-bit representation, the concluding $d$ is specified by $d_1 2^{B-1} + d_2$. The $2^{B-1}$ is a binary shift to line up the bits before transferring them to a binary addition. The outputs are repositioned according to the resolution that each stage contributes to the final estimate. Assuming $d_1$ and $d_2$ are divided into binary bits, Figure 2.10 shows the configuration of these bits before the addition.

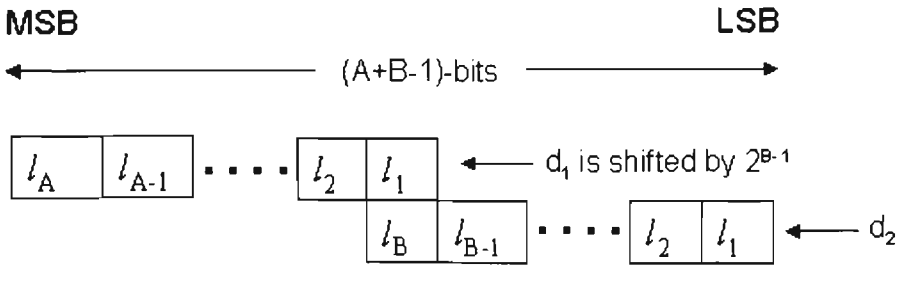



Figure 2.10: Digital correction for ($B$ +$A$ - 1)-bit ADC [38, 39].

Notice that in Figure 2.10, $l_1$ is the LSB and $l_A$ or $l_B$ is MSB of the consequent outputs. The procedure of the ADC for input voltages $\geq R_V$ needs meticulous consideration. Analysis of the error correction logic shows that erroneous results are produced for both $d_1 = (2^A - 1)$ and $d_2 = (2^B - 1)$. This conversion stipulation creates an arithmetic overflow and cannot present a valid ADC output state. To resolve this setback, the range of valid outputs for the $A$-bit converter is regularly limited.

Valid outputs vary from 0 to $(2^A - 2)$, thus this device will in no way create the challenging output state $(2^A - 1)$. In view of the fact that a mid-step design is practical here, eliminating this output state will not degrade the performance of the converter. The residual $v_n$ will still satisfy the boundary $|v_n| < R_V$ provided that the input is restricted by $|Y| < R_V$. This will guarantee that the sample is predicted correctly and no data is lost. The last stage of the pipeline ADC is only allowed to produce its diffusion state $d_2 = 2^B - 1$. This relationship corrects the saturation behavior of the converter, and reduces the hardware required to implement all intermediate pipeline stages.

The number of stages in a pipeline ADC can differ. In the instance described previously, the $A$-bit and $B$-bit converters can be regarded as the 2 stages in $(B+A-1)$-bit ADC. As the resolution of a stage declines, the number of comparators needed for the entire system also declines. An $A$-bit stage can have up to $(2^A - 1)$ comparators to achieve a resolution of $A$-bits. Multiple stage pipeline ADC is what this research is concerned about. By using this multiple stage philosophy, a reconfigurable pipeline ADC could be constructed.

## 2.1.6.3 Pipeline ADC with 1.5-bit/Stage

The requirements on the sub-ADC of a 1.5-bits/stage design are inhabited, hence proficient high-speed designs can be structured. The 1.5-bits/stage only has three valid quantisation periods, which are '00', '01'and '10'. In order to avoid overflowing in the digital correction, the state '11' is not valid output, unless it comes from the last stage in the pipeline string. To get $A$-bits of resolution, $(A - 1)$ stages are required. Using this characteristic architecture, the gain factor is set to a constant of 2 between the stages [40, 41]. A typical single stage structure of the 1.5-bits/stage architecture is illustrated in Figure 2.11 and is described in several papers [42-45].

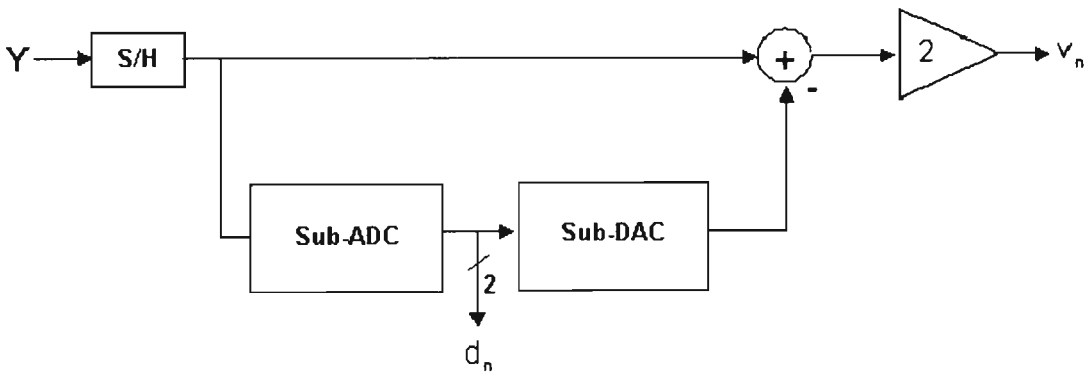



Figure 2.11: Single stage, 1.5-bit/stage pipeline ADC [45].

Supposing that the input has a range of $|Y| \leq R_V$, the quantisation period is $\frac{R_V}{2}$. The sub-ADC should have thresholds of $\frac{R_V}{4}$ and $-\frac{R_V}{4}$. In practice, the definite ADC thresholds will be different from these 'nominal' values. The ADC thresholds are illustrated in Figure 2.12 [38, 39]. Figure 2.12 also illustrates the corresponding digital outputs of the sub-ADC and the analog voltages, which are produced by the sub-DAC. The digital word-length is propelled to the digital correction logic of the ADC to be

amalgamated with all the other outputs from the other stages. The digital output delivers the input to the sub-DAC. This sub-DAC is designed to produce one of three possible output voltages. For the 1.5-bits/stage architecture these voltages are set to $\frac{R_V}{2}$, 0, and $-\frac{R_V}{2}$ for sub-ADC outputs codes '00', '01' and '10' respectively. The sub-DAC output is deducted from the input and the residual voltage is amplified by a gain factor of 2. If the sub-DAC outputs are accurate, this gain factor will level the residual error to $\pm R_V$, provided the sub-ADC quantisation thresholds are within $\frac{R_V}{4}$ of their nominal values. The subsequent stage will then quantise the residual error from this stage.

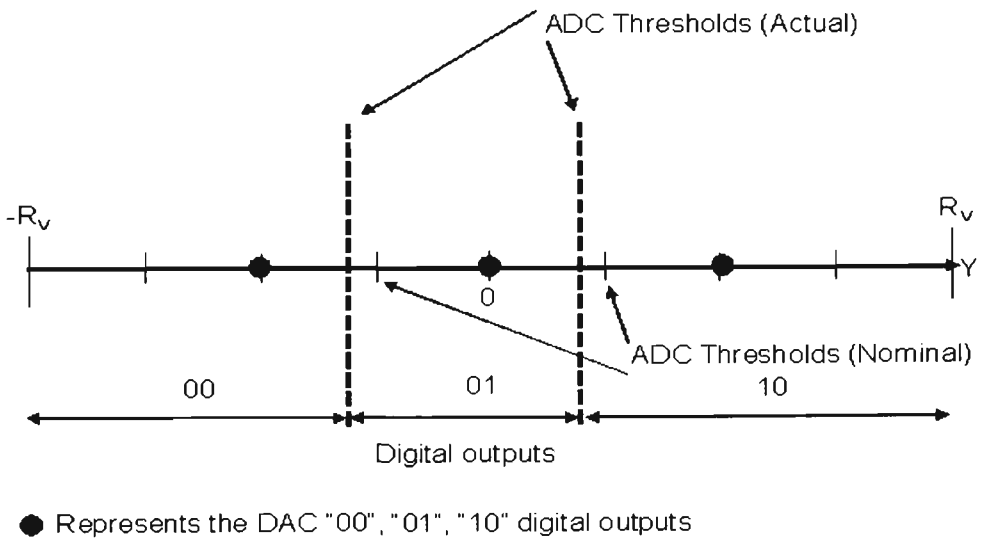



Figure 2.12: Sub-DAC outputs, 1.5-bit/stage pipeline ADC [38].

Digital error correction for a 1.5-bits/stage pipeline ADC is simple. Tentatively, the first stage in a pipeline presents the MSB for the final output and the last stage presents the LSB. Figure 2.13 [46] illustrates how the bits from each stage are joined together.

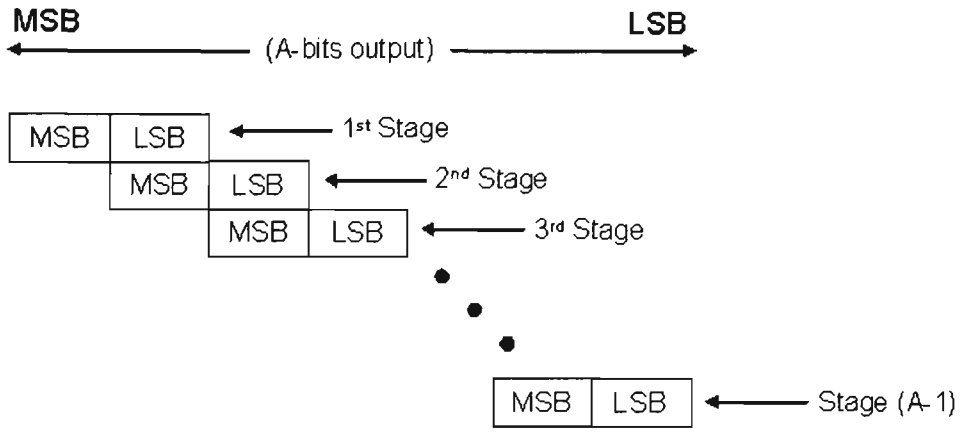



Figure 2.13: Digital error correction for 1.5-bit/stage pipeline ADC [46].

Table 2.1 is a merit summary of the five types of ADCs analysed.

Table 2.1: Summary of the five ADCs analysed

| ADC | Resolution | Speed | Advantages (+) Disadvantages (-) |
|---|---|---|---|
| Flash | 8 bits | 250Msps – 1Gsps | + Extremely fast<br>+ High input bandwidth<br>- Highest power consumption<br>- Large die size<br>- High input capacitance<br>- Expensive |
| S-AR | 10 bits – 16 bits | 76 ksps – 250 ksps | + High resolution & accuracy<br>+ Low power consumption<br>+ Few external components<br>- Low input bandwidth<br>- Limited sampling rates |
| Integrating | > 18 bits | < 50 ksps | + High resolution<br>+ Low supply current<br>+ Excellent noise rejection<br>- Low speed |
| Sigma - Delta | > 16 bits | > 100 ksps | + High resolution<br>+ High input bandwidth<br>+ Digital on-chip filtering<br>- External T/H<br>- Limited sampling rate |
| Pipeline | 12 bits – 16 bits | 1Msps – 80 Msps | + High throughput rate<br>+ Low power consumption<br>+ Digital error correction and on chip self-calibration<br>+ Good for communication applications<br>- Requires minimum clock frequency |

Literature on existing reconfigurable ADCs clearly differs from the work presented in this thesis. The work performed in [47], is one of these existing literatures. The design performed in [47] takes an approach where the user defines the resolution, and then depending on the selected resolution a particular ADC structure is selected, such as Sigma-Delta ADC or a pipeline ADC. Also the work performed in [47] is only on the architecture of the ADCs, not particularly selected for an application. However, one of the most important aspects of the difference between the work presented in this thesis and the design in [47] is that the design in [47] is not a real-time reconfiguration. The proposed reconfigurable architecture in this thesis is fully real-time reconfigurable design, where depending on the interference occurring from adjacent base and mobile stations, the ADC, in real-time, by using an intelligent control unit, reconfigures it self to meet the required specification.

# PART II

## 2.2 Wideband Code Division Multiple Access

Second generation systems (2G) such as personal digital communications (PDC), global system for mobile communications (GSM), cdmaOne (IS-95) and US–time division multiple access (TDMA) (IS-136) have enabled voice communication to switch to wireless. Also known as digital systems, they offer services such as text messaging and access to data networks. Prior to this second generation of systems, the analog cellular systems referred to as the first generation systems (1G) were in use. Lacking quality for multimedia communications (person to person communication) and access to information and services on public and private networks of the 1G and 2G, the third generation systems (3G) were designed. With the continuous evolution of the 2G and the design of the 3G, new business opportunities for the manufacturer and the provider using these networks have been created. Wideband code division multiple access (WCDMA) technology has been surfaced as the most extensively accepted third

generation air interface. The joint standardisation bodies from Japan, China, Europe, USA, and Korea have created the specification for WCDMA in the third generation partnership project (3GPP). Within this partnership project, WCDMA is referred to as the Universal Terrestrial Radio Access (UTRA). WCDMA is characterised by two duplex modes: Frequency Division Duplex (FDD) and Time Division Duplex (TDD) [48]. Figure 2.14 [48, 49] illustrates the peculiarity between the two duplex modes. The space division duplex (SDD) method is not considered here because this method is used in fixed-point transmission where directive antennas can be used. This method is not used in mobile terminals.

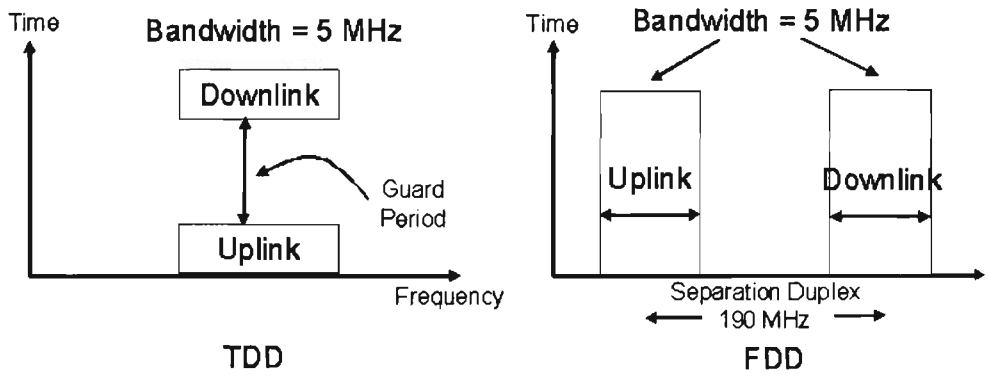



Figure 2.14: UTRA duplex modes [48, 49].

In the UTRA-FDD mode, the uplink and downlink transmissions use paired radio frequency bands whereas in UTRA-TDD, uplink and downlink transmissions are carried over same radio frequency using synchronised time intervals. Time slots in the physical channel are divided into transmission and reception part [50-52]. Information on uplink and downlink are transmitted reciprocally [53]. This makes TDD mode susceptible to adjacent channel interference (ACI) as nearby mobile stations (MS) and base stations (BS) cause interference to each other depending on frame synchronisation

and channel asymmetry. Table 2.2 [54] compares the key parameters of the UTRA-TDD and FDD physical layer.

Table 2.2: Parameters comparison of UTRA-TDD and FDD

| | **UTRA-TDD** | **UTRA-FDD** |
|---|---|---|
| Duplex Method | TDD | FDD |
| Multiple Access Method | TDMA, CDMA, FDMA | CDMA (inherent FDMA) |
| Channel Spacing | 5 MHz (nominal) | |
| Carrier Chip Rate | 3.84 Mcps | |
| Timeslot Structure | 15 slots/frame | |
| Frame Length | 10 ms | |
| Modulation | QPSK | |
| Multirate Concept | Multicode | Multicode and OVSF |
| Intra-Frequency Handover | Hard Handover | Soft Handover |
| Inter-Frequency Handover | Hard Handover | |
| Spreading factors | 1 ... 16 | 4 ... 512 |

The reconfigurable pipeline ADC is designed to be used on the downlink UTRA-TDD mode due to its near far problem. The near far problem along with the interference issues is described in section 2.2.2.3 of this chapter. Under this condition, the UTRA-TDD mode is described in greater detail in the following section.

## 2.2.1 UTRA-TDD Mode

There are distinct advantages of the UTRA-TDD system in comparison to the FDD system. The key advantage is that the TDD system can be implemented on an unpaired frequency band, while the FDD system requires a pair of bands. This characteristic solves some frequency band allocation issues resulting in effective and efficient use of the spectrum [54, 55]. Services such as mobile Internet, multimedia applications and file transfers may have different capacity requirements for uplink and downlink transmission. UTRA-TDD offers the advantages of flexibility in resource allocation, as

the frequency band is not fixed between uplink and downlink [54, 55]. Other advantages of the TDD system are listed in [56] and include the following:

- Adaptive support of asymmetric data rates
- High speed data services for indoor or low-mobility operating environments
- Large channel capacity (equivalent to FDD mode)
- Small sized mobile terminal
- Low complexity transceivers

### 2.2.2.1 Transmitter Architecture

The UTRA-TDD transmitter released by the 3GPP is presented in Figure 2.15 [57]. The figure presents the modulation for only one time slot containing sixteen users, which is one of fifteen time slots [58, 59]. Appendix A presents greater detail of the spreading and modulation of the TDD mode. The first block in the transmission chain is the data mapping. The data mapping of raw bits is executed using Quadrature Phase Shift Key (QPSK), where two successive binary bits are united and converted to a complex valued data symbol. The complex valued data symbols are spread by two operations. First, the symbols are spread with real valued channelisation codes $C_i$. The channelisation codes are orthogonal OSVF codes, allowing amalgamation of the same time slot with different spreading factors whilst maintaining orthogonality. The resulting sequence is scrambled by a complex cell specific scrambling code $v$. The complex-valued chip sequence is split into in-phase (I) and quadrature (Q) signals. The signals are subsequently pulse-shaped by two low pass pulse-shaping filters.

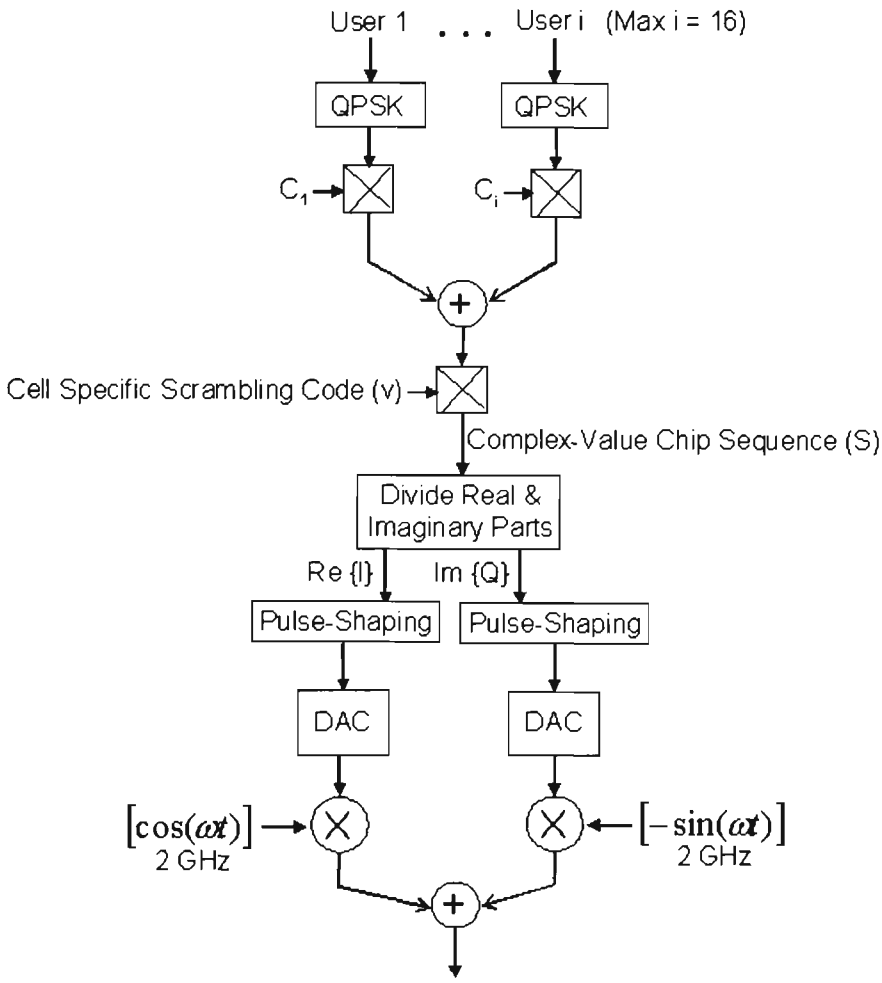



Figure 2.15: UTRA-TDD Base band Transmitter (one time slot) [57]

The two DACs after the pulse-shaping filters, convert the digital signals to analog signals. The signals are afterwards quadrature modulated to characterise the signal in RF format at the 2 GHz carrier frequency. The whole information is enclosed in the complex envelope and in the phase of the RF signal.

## 2.2.2.2 Receiver Architecture

Figure 2.16 [57] illustrates the standard block diagram of a direct conversion UTRA-TDD receiver. A RF signal is received by the antenna and then processed by the RF filter and the low noise amplifier (LNA). The quadrature demodulator produces a

complex valued chip sequence, both I and Q. The anti-aliasing filter removes aliasing in the spectrum from both I and Q then the ADC converts the signal from analog to digital. The RRC filter has a pulse-shape impulse response that attenuates out-of-band signals from the I and Q channels before the in-band signal is brought to the other base band signal processing blocks. The end user of the mobile terminal will experience a great deal of interference noise if the out-of-band signals were not filtered. Once filtering is completed, the signals are de-scrambled with a cell specific scrambling code $V_n$, de-spread with channelisation code, and finally de-modulated (de-QPSK) to obtain the users' raw data bits.

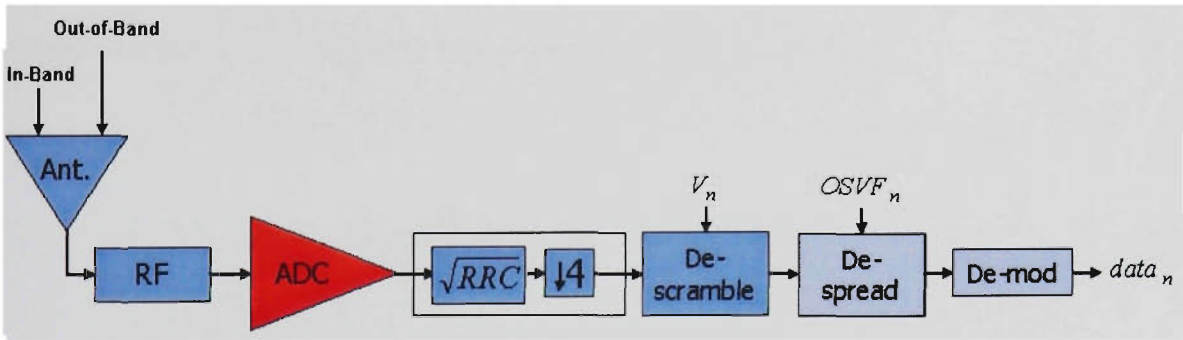



Figure 2.16: UTRA-TDD Receiver architecture for one time slot [57]

## 2.2.2.3 Interference Issues (Downlink Analysis)

This section describes the adjacent channel interference (ACI) experienced at the mobile terminal, where the signals arrive from the base stations, also known as downlink analysis. Due to the fact that the Analog-to-Digital Converter is within the mobile receiver (Ms), and the signals are sent from the BS to MS, it is appropriate to analyse and review the downlink propagation of the signals arriving at the MS. Two interference instances exist in this scenario, mobile station to mobile station (MS→MS) and base station to mobile station (BS→MS) interference.

#### 2.2.2.3.1 Propagation Model

The path loss is modelled in accordance to the COST 231 indoor propagation environment with no wall and floor losses [60-62]:

$$\kappa = 37 + \gamma 10\log(d) + \xi \text{ [dB]} \tag{2.6}$$

where $\gamma$ is the path loss exponent and $d$ is the separation between transmitter and receiver. Lognormal shadowing is modelled by $\xi$ [60] with a mean of zero and a standard deviation of $\sigma$. The receiver sensitivity is modelled as:

$$Rs = \frac{Eb}{No} + \eta - pg + I_{margin} \text{ [dB]} \tag{2.7}$$

where *Eb/No* is the required bit-energy to interference ratio, $\eta$ is the thermal noise, *pg* is the processing gain and $I_{margin}$ is an additional interference margin from the presence of other users in the same cell. $I_{margin}$ is modelled as:

$$I_{margin} = \frac{1}{1 - \frac{M-1}{\frac{pg}{Eb/No}}} \tag{2.8}$$

where $M$ is the number of users in the cell of interest (COI). Transmission power (*Ptx*) is derived from the receiver sensitivity *Rs* and the path loss model $\kappa$ and is as follows:

$$Ptx = Rs + \kappa \text{ [dB]} \tag{2.9}$$

#### 2.2.2.3.2 Downlink Interference Model

The extent of this work was restricted to downlink analysis. As noted earlier, MSs experience ACI from two sources, adjacent BSs and adjacent MSs dependant on the synchronisation factor $\alpha$. To gain an understanding of how this affects the amount of ACI experienced from BSs and MSs, we need to examine $t_{off}$. A small $t_{off}$ results in a high BS→MS interference and a low MS→MS interference. It is vice versa for a large $t_{off}$. It cannot be assumed that synchronised frames in a fully flexible system, therefore the computer simulations take into consideration misaligned frames and different asymmetry. To explore the effect of ACI in the downlink with no adjacent channel protection (ACP) factor present, it would give the raw adjacent channel interference power. These raw adjacent interference power measurements are needed to determine, depending on location in the COI, how much ACP is needed to satisfy the required bit energy to interference ratio *(Eb/No)*.

To determine the interference power from a single adjacent channel BS at a MS in the COI, we need to first determine the adjacent channel BS transmission power and the path loss between this BS and the MS in the COI. The ACI is then the BS transmission power multiplied by how many users are being served in this adjacent channel cell, over the path loss and is as follows:

$$I_{BS} = \frac{Ptx_{bs} \bullet M}{\kappa_{bs}} \tag{2.10}$$

where $I_{BS}$ is the interference experienced from the adjacent base stations, $Ptx_{bs}$ is the adjacent channel BS transmission power, $M$ is the number of users served by this BS, and $K_{bs}$ is the path loss between the adjacent channel BS and the MS in the COI. Based on this model, the total raw BS→MS ACI can be calculated with many adjacent channel interferers. Hence, raw BS→MS adjacent channel interference including a synchronisation factor is modelled by [62]:

$$I_B = \sum_{j=1}^{H} (1-\alpha) \frac{Ptx^j M^j}{\kappa^j{}_{B_m}} \tag{2.11}$$

where $I_B$ is the raw adjacent channel interference experienced from MS → BS, $\kappa^j{}_{B_m}$ is the path loss between the $j^{th}$ adjacent channel BS causing interference and the mobile located at $m$ in the COI. $M^j$ is the number of users served by the $j^{th}$ BS. $Ptx^j$ is the $j^{th}$ adjacent BS transmission power. The user facing the greatest attenuation in an adjacent channel cell determines the transmission power of that adjacent channel BS. This results in high or low BS transmission powers.

To investigate the interference power from a single MS in one adjacent channel cell at a MS in the COI, the transmission power of the MS in the adjacent channel cell needs to be calculated. The path loss from the adjacent channel MS to the MS in the COI also need be determined. The ACI results in:

$$I_{MS} = \frac{Ptx_{ms}}{\kappa_{ms}} \tag{2.12}$$

where $I_{MS}$ is the interference experienced from the adjacent mobile stations, $Ptx_{ms}$ is the adjacent channel MS transmission power and $\kappa_{ms}$ is the path loss between the adjacent channel MS and the MS in the COI. To investigate the raw MS→MS ACI caused by many MSs in many adjacent channel cells incorporating a synchronisation factor, the interference results in [62]:

$$I_M = \sum_{j=1}^{H} \sum_{i=1}^{M} \alpha \frac{P^j tx_i}{\kappa^j{}_{M_i M_m}} \tag{2.13}$$

where $I_M$ is the raw adjacent channel interference experienced from MS → MS, $\kappa^j{}_{M_i M_m}$ is the path loss between the $i^{th}$ MS in the $j^{th}$ adjacent channel cell causing interference and the mobile $m$ in the COI. $P^j tx_i$ is the MS transmission power. It can clearly be seen that when $\alpha = 0$, all ACI is sourced from the adjacent BSs. If $\alpha = 0.01$, this would mean that ninety nine percent of ACI is from adjacent channel BSs and one percent from adjacent channel MSs. The total ACI is a linear sum of both sources of interference. Therefore, the total downlink raw ACI power a mobile experiences at point $m$ is:

$$I_{total} = I_B + I_M \tag{2.14}$$

## 2.3 Conclusion

There are distinct advantages of using the pipeline ADC topology as compared with other topologies such as Flash ADCs, SAR ADCs, Sigma-Delta ADCs and Integrating ADCs. While the flash ADC architecture can reach very high speed, it consumes a lot of

power due to the high circuit complexity and large device count. The other ADC architectures consume little power, but they operate at very low speeds, which are not appropriate for the UTRA-TDD application, where the 3G specification of 15.36 MSPS needs to be met. However, even though fix word-length pipeline ADC architecture could be a suitable device for the mobile receiver, it still has a distinct disadvantage when it comes to power consumption. In many cases a fixed word-length ADC is used, say 12-bits, when the receiver requires and uses a converter of only 8-bits. During this time the whole 12-bit device is powered up, which uses a lot more power than it is supposed to. To achieve this, a more complex receiver ADC design and implementation is required, which will have a significant impact on battery life in the mobile terminal.

ADC optimisation techniques could lower power consumption but will not reduce it to its most efficient level. A solution in theory is to use minimum resolution, and still meet the performance requirements of the UTRA-TDD receiver specified by the 3GPP. To achieve this, in-band and out-of-band signal powers need to be measured. Then the ADC intelligently chooses the amount of resolution required to ensure the out-of-band signal is below a certain tolerance level and the SNR is met. This scheme will reduce power consumption, as it only utilises the required resolution as compared to traditional fixed complexity architectures.

To translate theory into reality, the solution has to take advantage of the software radio concept and technologies [54]. An exact definition for a software radio does not yet exist, but there are many definitions to help gain an understanding [55, 56].

Taking advantage of the software radio theory, a solution can be achieved using DSP and application specific integrated circuit (ASIC) technologies that can meet the performance and system needs of high speed and low cost devices. A DSP can interface with an ASIC and control the ADC resolution dependant on in-band and out-of-band power ratios, making the design a reconfigurable solution. This could be embedded on a single chip to provide a System on a Chip (SoC) solution.

# Chapter 3

# *Circuit Techniques for Pipeline ADC*

## 3.1 Introduction

The design of high performance ADCs for high-speed and low power applications requires investigation of the building block components of this ADC. This chapter presents a review of the most commonly used circuits suitable for low power pipeline ADCs and their characteristics. The designs covered here include, sample-and-hold circuits, comparator circuits and operational amplifier circuits. The proposed sample-and-hold circuit and the comparator circuit used within the reconfigurable pipeline ADC are also presented and analysed.

## 3.2 Sample & Hold Circuits

A high performance sample-and-hold circuit for pipeline ADCs should provide the following characteristics: must achieve high linearity, high speed, high drive capacity, large voltage swings, and simultaneously low power consumption. Performance characteristics of sample-and-hold circuits in Bipolar and CMOS technology are described in the following sections.

### 3.2.1 Techniques for Sampling

Sampling techniques can be classified as parallel sampling and series sampling. The circuit of Figure 3.1, named *"Parallel Sampling"*, shows a sampling capacitor $C_1$ in parallel with the signal. In the circuit of Figure 3.2, named *"Series Sampling"* the sampling capacitor $C_{hold}$ is in series with the signal, therefore the common-mode levels of the input and output are isolated.

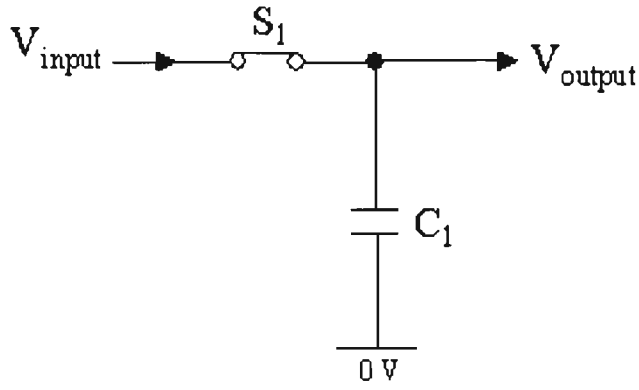



Figure 3.1: Parallel Sampling

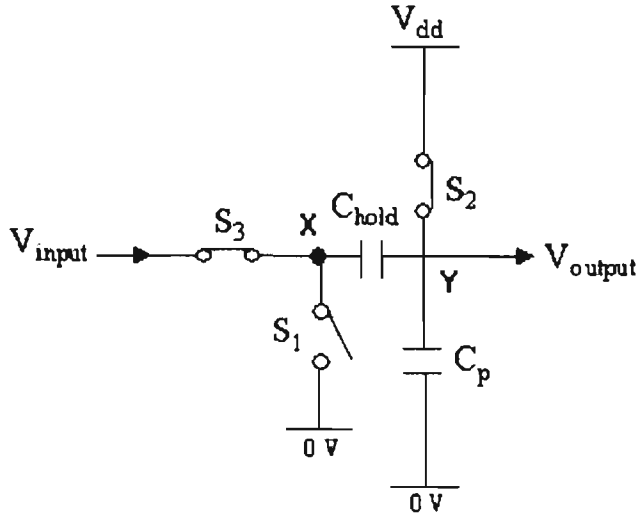



Figure 3.2: Series Sampling

In Figure 3.2, while the acquisition stage, switches $S_2$ and $S_3$ are on and in the transition to the hold mode, first node Y is released from $V_{dd}$ and subsequently node X is shorted to ground, producing a voltage charge at the output equal to the value of the input. The "*Series Sampling*" technique has a great advantage over the "*Parallel Sampling*" technique. Whilst parallel sampling endures from input dependent charge injection of $S_1$, series sampling doesn't demonstrate such behavior due to the fact that $S_3$ turns off after $S_2$, therefore injecting a constant charge onto node Y.

The "*Series Sampling*" technique has two disadvantages compared to the "*Parallel Sampling*" technique. The non-linearity of the parasitic capacitance $C_P$ at point Y introduces distortion in the sampled value, consenting that the value of $C_{hold}$ be adequately larger than that of $C_P$. Also, the hold settling time in series sampling is a lot longer than in parallel sampling.

This is due to the fact that in the past the output voltage ($V_{output}$), must always begin from a reset value while in the concluding stage, $V_{output}$ begins from a level close to its finishing value. Sampling techniques could be implemented with various types of switches. One of these types is by using MOS transistors, as shown in Figure 3.3.

MOS transistors need low complexity and trouble-free circuitry but they reveal two sources of dynamic errors, totaling to the channel charge injection and clock feed-through. First, as shown in Figure 3.4, the finite transition time of the sampling clock consequences in an input dependent sampling instant [63].

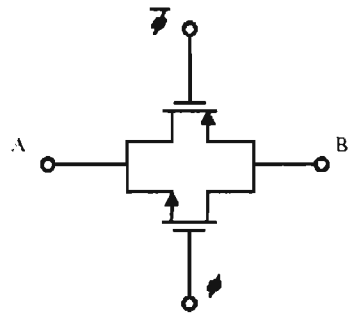



Figure 3.3: A typical CMOS switch [63]

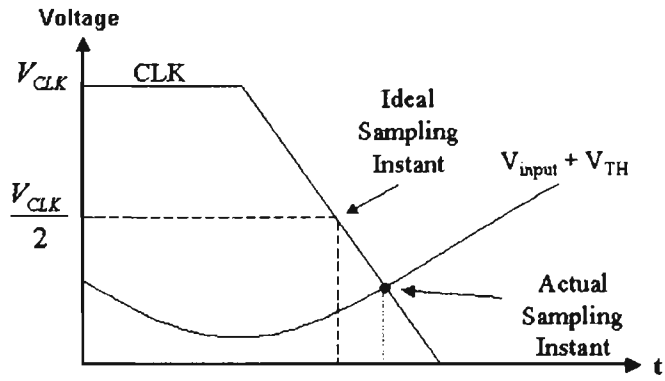



Figure 3.4: Input dependent sampling stage [63].

Second, as illustrated in Figure 3.5, the disparity of the switch on-resistance with the input level institutes distortion.

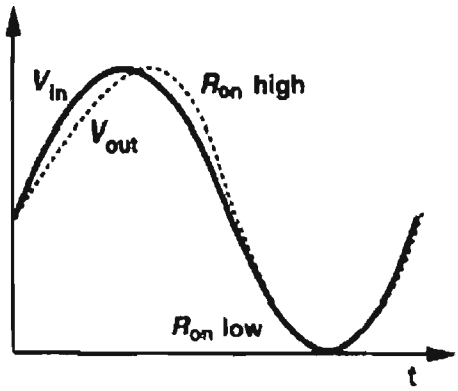



Figure 3.5: Distortion due to disparity of switch on-resistance [69].

Another issue that must be considered when designing in low voltage applications is the high on-resistance of the actual MOS devices, in particular when the source/drain

common mode level is approximately $\frac{1}{2}V_{dd}$ [69]. The design of low-voltage analog and mixed signal circuits often imposes severe speed and precision limitations upon signal processing systems. In multi-step ADC, such as the pipeline topology for example, the front-end sample-and-hold amplifier must achieve high speed and high linearity with low power consumption while the limited voltage headroom contains its dynamic range. It is recommended that in pipeline ADC, series sampling to be used instead of parallel sampling. This is because the parallel sampling suffers from input dependent charge injection, where as series sampling does not illustrate such behavior.

### 3.2.2 Sample & Hold Circuits in Bipolar technology

In bipolar technology the simplified sampling bridge of Figure 3.6 is used [63]. Achieving a high speed, the circuit nevertheless provides little dynamic range with a 3-volt supply. Alternatively, the bridge can be modified as illustrated in Figure 3.7, where the top two diodes are removed, the input diode is replaced with an emitter follower, and the bottom current source is converted to a single-ended form, saving some voltage headroom.

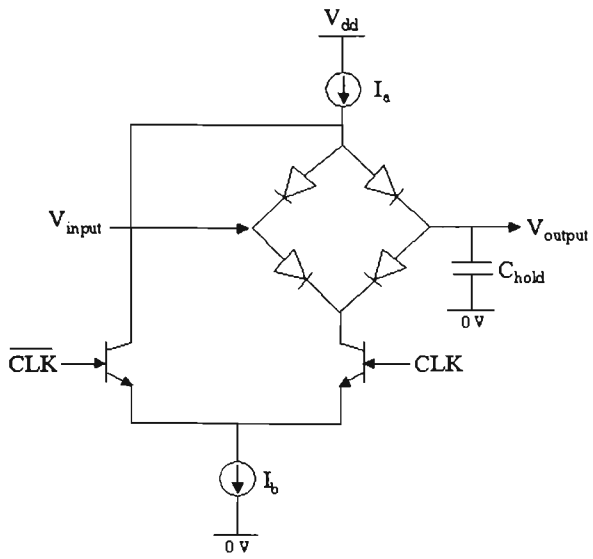



Figure 3.6: Simplified diode bridge [63].

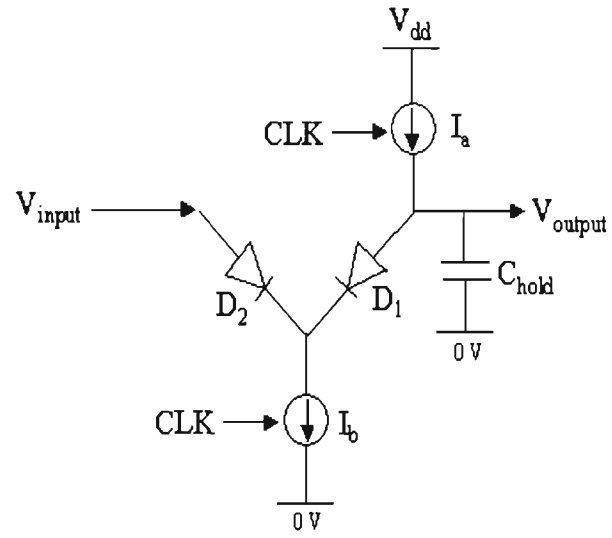



Figure 3.7: Bridge with top diodes removed [63].

The low-voltage BiCMOS sampling switch of Figure 3.8 [63] can be used in a sample-and-hold circuit to achieve a relatively high speed. One characteristics that results from the simplified diode bridge of Figure 3.6 is that the minimum supply voltage could be calculated, where it is assumed that $V_D \approx 0.8$ V, $V_{CE,min} \approx 0.5$ V, and the minimum voltage across $I_a$ and $I_b$ is 0.5 V. Therefore, $V_{CC,min} \approx 3.1$ V.

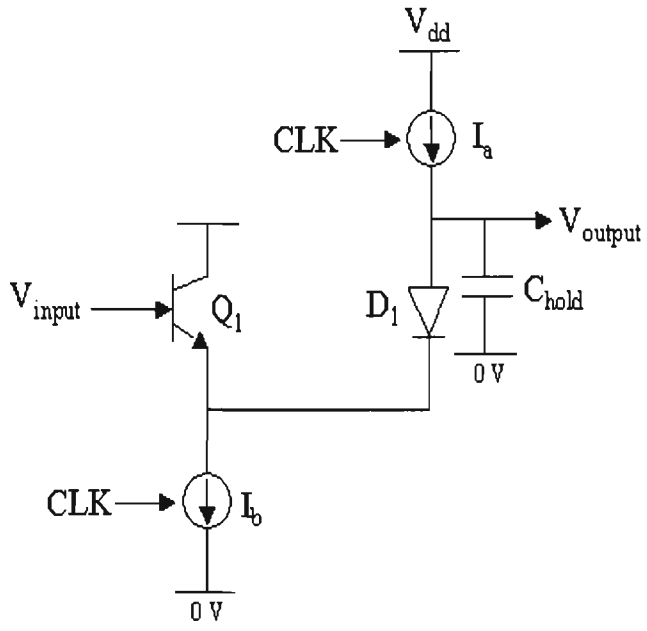



Figure 3.8: Bridge with input follower [63].

### 3.2.3 Sample & Hold Circuits in CMOS technology

Sample-and-hold (S/H) circuits' architecture that is popular in CMOS technology is shown in Figure 3.9. The design here is based on the series sampling technique, shown in Figure 3.10. The approach illustrated in Figure 3.9 utilises a virtual ground to perform a precise previous function. Since at the end of the acquisition mode, $S_1$ and $S_2$ turn 'off' after $S_3$ and $S_4$, the charge injected by the former two is equal, distributing only the output Common Mode (CM) level. The difficult task however here is in the design of the operational amplifier used in this technique.

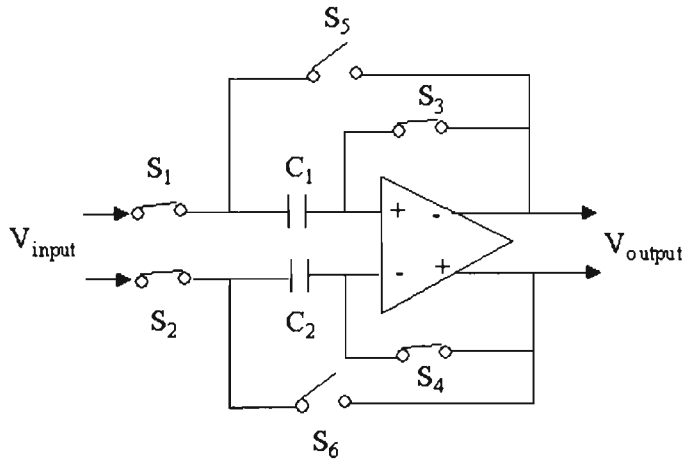



Figure 3.9: Unity gain sampling [64]

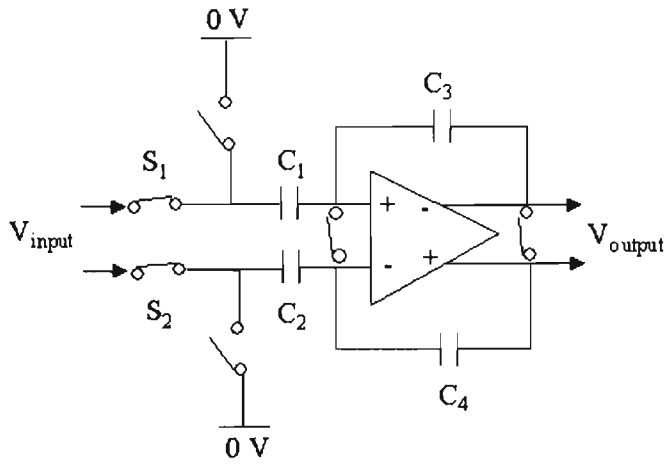



Figure 3.10: Series sampling technique [64]

More specifically:

- As the supply voltage of the op-amp is reduced, the op-amp suffers from various trade-offs in dynamic range, speed, and linearity.
- The op-amp needs an input/output common-mode level approximately equal to half the supply voltage, therefore limiting the gate-source overdrive voltage of $S_3 - S_6$ and degrading the settling behavior.

The circuit of Figure 3.9 only produces a maximum sampling frequency of 25 MHz [64]. This can be partly attributed to the large device widths required in the op-amp so as to achieve adequate voltage swings. Due to this reason, the architecture shown in Figure 3.10 is suitable in a way that it allows independent choice of the input and output common mode (CM) levels. Figure 3.11 illustrates a S/H circuit architecture proposed in [65].

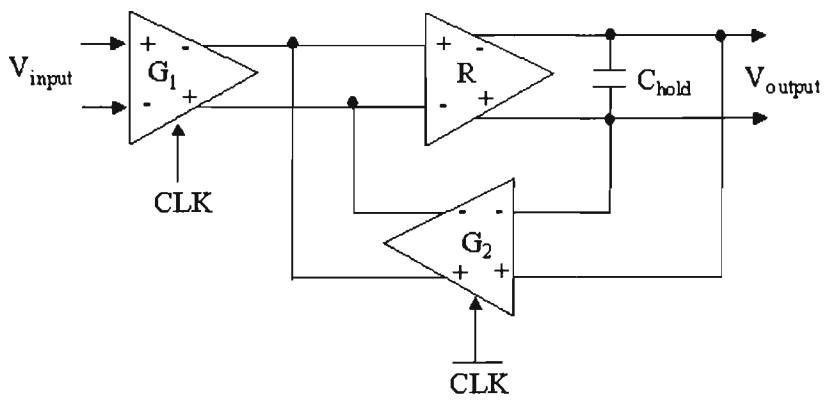



Figure 3.11: S/H architecture with transconductance and transresistance stages [65].

The circuit employs a transresistance stage $R$ and two transconductance stages, $G_1$ and $G_2$, where $G_1R=G_2R = 1$. When the circuit is in the acquisition period, the combination of $G_1$ and $R$ operate as a unity amplifier in which the output voltage $V_{output}$ is allowed to

track the input voltage $V_{input}$. When the circuit is in the hold period, the transconductance $G_2$ is enabled, $G_1$ is disabled, and $G_2$ and $R$ are configured as a unity gain amplifier in which the sampled value of $V_{input}$ retained across capacitor $C_{hold}$.

Another S/H circuit architecture similar in operation to the topology of Figure 3.11 with is the recycling S/H circuit illustrated in Figure 3.12 [66].

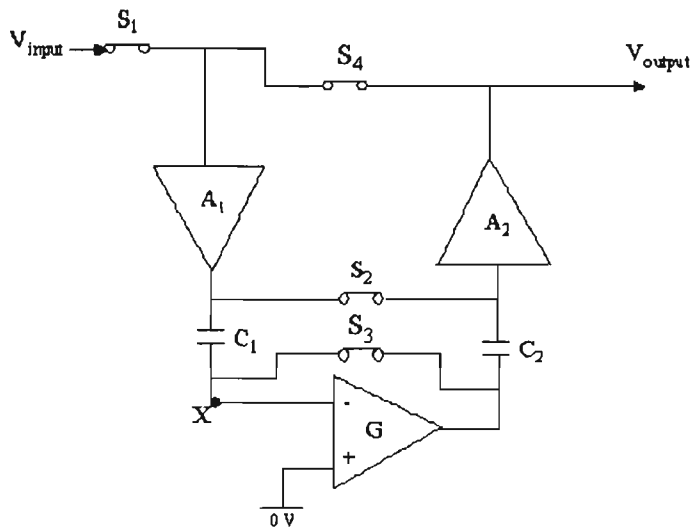



Figure 3.12: Recycling S/H circuit architecture [66].

During the sample stage of the operation, $S_1$, $S_2$ and $S_3$ are switched on and the $G$ stage creates an implicit ground at point X. While the transition from sample to hold mode takes place, $S_3$ turns off first, concurrently $S_1$ and $S_2$ turn off, and $S_4$ turns on. Therefore, $A_1$, $A_2$ and $G$ make up a unity gain feedback loop, which would hold the sampling level on $C_1$.

### 3.2.3.1 Switched Capacitor Sample & Hold Circuits

Switched capacitor circuits are pervasive in highly integrated, mixed signal applications. The sample-and-hold is the most basic and ubiquitous switched-capacitor building block. Before a signal is processed by a discrete-time system, such as an ADC, it must

be sampled and stored. This often greatly relaxes the bandwidth requirements of following circuitry, which now can work with a DC voltage.

Due to the fact that the S/H is often the first block in the signal processing chain, the accuracy and speed of entire application cannot exceed that of the S/H.

#### 3.2.3.1.1 Top Plate Sample-and-Hold Circuits

In CMOS technology, the simplest S/H consists of a MOS switch and a capacitor as shown in Figure 3.13 [67]. When $V_g$ is high the NMOS transistor acts like a linear resistor, allowing the output Vo to track the input signal $V_i$. When $V_g$ transitions low, the transistor cuts off isolating the input from the output, and the signal is held on the capacitor at $V_o$.

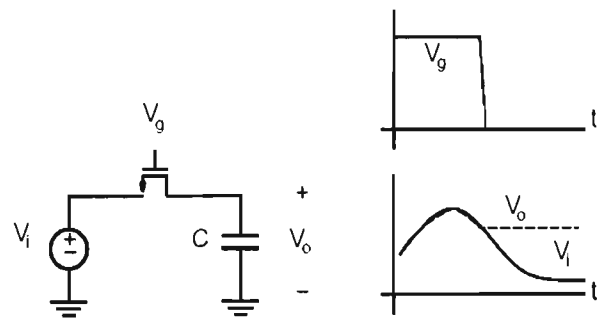



Figure 3.13: MOS Sample-and-Hold [67]

There are several practical limitations to this circuit. Because the RC network has finite bandwidth, the output cannot instantaneously track the input when the switch is enabled. Therefore, a short acquisition period must be allocated for this (exponentially decaying) step response.

After the S/H has acquired the signal, there will be a tracking error due to the non-zero phase lag and attenuation of the sampling network. The latter linear, low-pass filtering does not introduce distortion and is usually benign for most applications.

### 3.2.3.1.2 Bottom Plate Sample-and-Hold Circuits

A technique called bottom-plate sampling to first order eliminates some of the errors in the top-plate S/H circuit. Figure 3.14 shows the bottom-plate sampling configuration. While clocks $\phi'$ and $\phi$ are high, $V_o$ tracks the input voltage $V_i$. When clock $\phi'$ transitions from high to low, switch $M_2$ turns off, and the charge on node X is trapped. The charge on capacitor $C$ is now fixed $q=CV_i$. This is the defined sampling instant. When $\phi$ clock transitions from high to low, switch $M_1$ is turned off and the output is isolated from the input [67, 68].

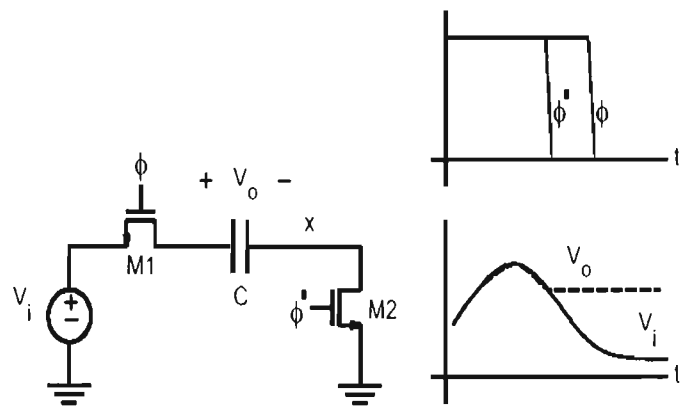



Figure 3.14: Bottom plate sample-and-hold circuit [67]

When $M_2$ turns 'off', the voltage at node $X$ is perturbed due to clock feed through and charge injection. In this case, the charge injection is signal-independent because drain and source see a fixed potential (ground). This condition eliminates signal-dependent charge injection distortion.

The charge injection from $M_1$ does not alter the charge stored on capacitor $C$ due to charge conservation.

### 3.2.4 Methods of using S/H circuits in ADCs

Using a front-end sample-and-hold circuit in ADC architecture is highly valuable in some cases, but very much unnecessary in other cases. Some common applications are considered below.

#### 3.2.4.1 One-Stage & Multi-Stage ADCs

The need of front-end sample-and-hold circuits in ADCs is highly beneficial. This is due to the fact that one-stage ADCs, such as folding and flash topologies use a distribution of samples in the cache of comparators. On the other hand, some not so ideal timing issues in these architectures restrain the effective number of bits at high input frequencies. A lot of apparatus report for this squalor [63]. Firstly, as illustrated in Figure 3.15, the non-linearity noticed on the input capacitance, which occurs from a large number of comparator circuits together with the source impedance resulting in a harmonic distortion.

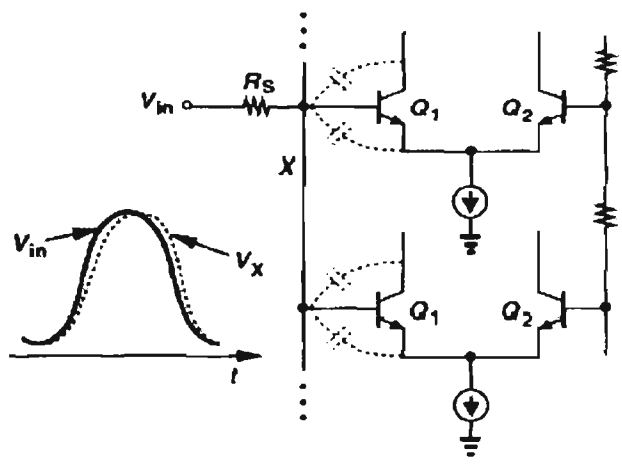



Figure 3.15: Non-linearity of input capacitance in Flash ADC [63]

Secondly, as depicted in Figure 3.16, an input dependent offset from each comparator circuit is introduced by the capacitive feedback from the input signal to the ladder of resistors disturbing the reference stage voltages.

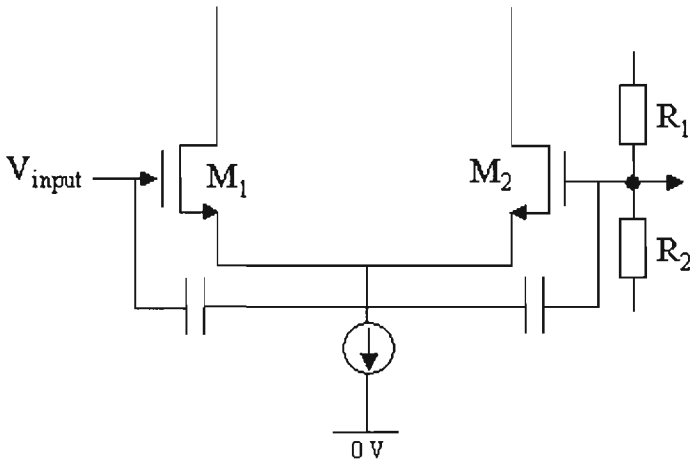



Figure 3.16: Feedback of input signal to resistance ladder [63]

Thirdly, as shown in Figure 3.17, sparks appear in the thermometer code of a flash ADC due to mismatches between different sampling instants of neighboring comparator circuits.

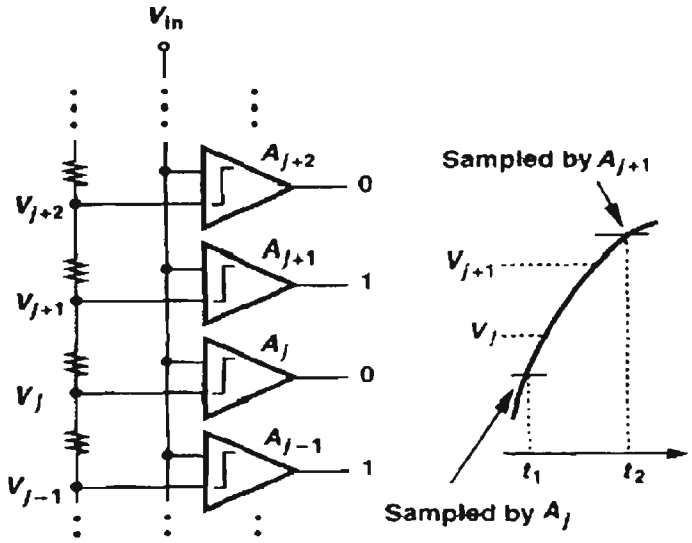



Figure 3.17: Bubbles (sparks) appearing from timing disparity [63].

## 3.3 Comparator Circuits

The design of fast precision comparators require careful trade-offs among parameters such as speed, resolution, power consumption, and input capacitance. The speed of a comparator is often limited by its preamplifier override recovery, while the resolution is constrained by the input offset of its latch. A CMOS comparator utilising offset cancellation technique has been introduced in this section. To achieve a small residual offset, this technique combines a preamplifier and a regenerative latch, both with an offset cancellation. Also in this section a design and simulated results have been presented of a CMOS comparator used in an interleaved pipeline ADC that performs analog processing only by means of open-loop circuits to achieve high conversion rate. To achieve the correct residual output from one-stage pipeline ADC, an amplifier circuit is employed to amplify the output, so it is equal to the original input. This amplification factor is $2^N$, when $N$ is the number of bits required. This section introduces a number of comparator design techniques for use in ADC that are implemented in CMOS very large scale integration (VLSI) technologies, in particular attention is paid to offset cancellation techniques. The suggested techniques are intended to provide improved speed and resolution while maintaining low power consumption and low complexity.

### 3.3.1 Offset Cancellation Techniques

#### 3.3.1.1 Circuit Topologies

Of the various offset cancellation techniques, two of the most common approaches, based on input offset storage (IOS) and output offset storage (OOS) are illustrated in Figure 3.18 and 3.19. The two approaches are design to be functional to a fully

differential comparator. A preamplifier, a latch, and offset storage capacitors are present in both of these topologies.

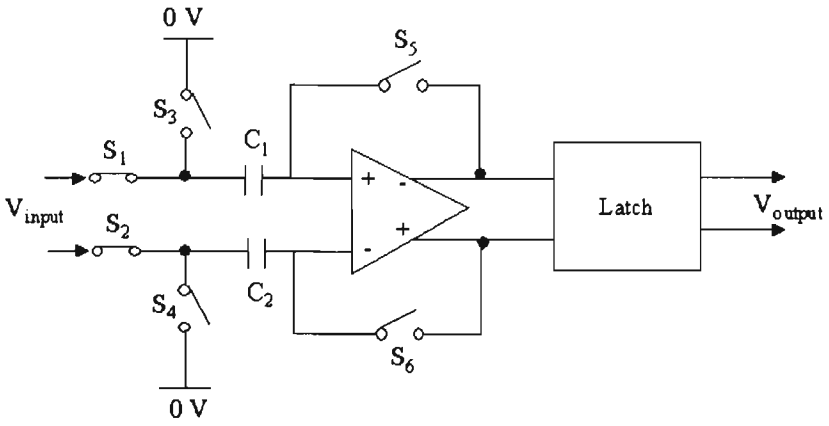



Figure 3.18: Comparator offset cancellation techniques (input offset storage) [70].

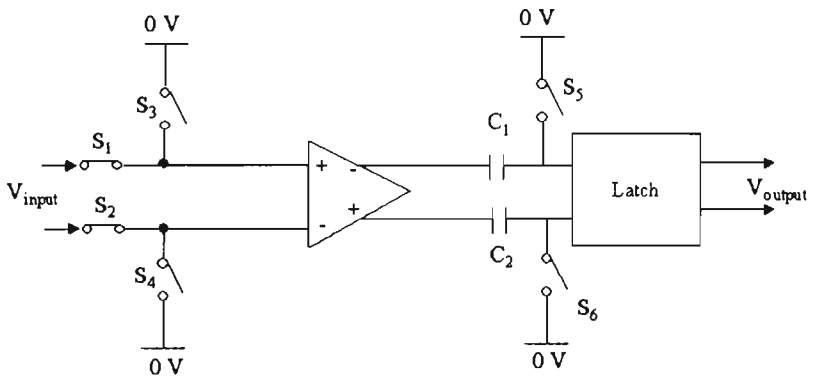



Figure 3.19: Comparator offset cancellation techniques (output offset storage) [70].

With IOS, closing a unity gain loop around the preamplifier and then storing the offset on the input coupling capacitors perform the cancellation. In OOS, the preamplifier input is shortened to cancel the offset, and then the amplifier offset is stored on the output coupling capacitance.

In the comparator with IOS, the offset voltage $V_{OS}$ after calibration is:

$$V_{OS} = \frac{V_{OS1}}{1+A_0} + \frac{\Delta Q}{C} + \frac{V_{OSL}}{A_0} \tag{3.1}$$

where $V_{OSI}$ and $A_0$ are the input offset and gain of the preamplifier, respectively, $\Delta Q$ is the mismatch in charge injection from switches $S_5$ and $S_6$ onto capacitors $C_1$ and $C_2$, and $V_{OSL}$ is the latch offset. In the comparator with OOS, the offset after calibration (residual) is [71]:

$$V_{OS} = \frac{\Delta Q}{A_0 C} + \frac{V_{OSL}}{A_0} \tag{3.2}$$

From Equations 3.1 and 3.2, it can be seen that for similar preamplifiers, the offset after calibration achievable using OOS can be smaller than that for IOS. In conventional CMOS comparator design, a standard dynamic CMOS latch typically follows the preamplifier. As described in the following subsection, the latch has a prospectively large input offset and therefore a high-gain preamplifier is required in order to obtain low offset. In high-resolution designs, a single-stage of OOS cannot be used, whereas a single stage high-gain preamplifier with IOS endures from a long delay. From the above consideration, it has led to the use of multi-stage calibration techniques in high-resolution applications. Figure 3.20 here depicts a multi-stage comparator architecture that utilises both OOS and IOS, only when clocked sequentially [71].

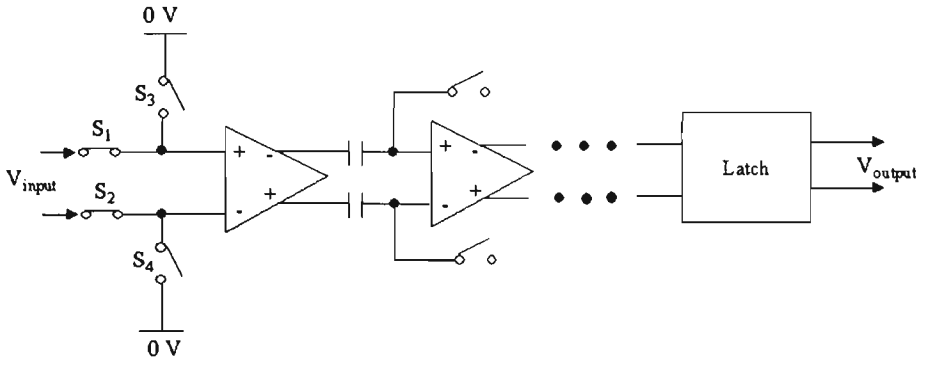



Figure 3.20: Multi-stage offset cancellation [71].

### 3.3.1.2 Design Constraints in a CMOS Latch

In order to provide the gain required to generate logic levels at the output, and to synchronize the operation of a comparator with other parts of a system, a regenerative amplifier is normally employed as the final comparator stage. A dynamic CMOS latch, shown in Figure 3.21 [71], is employed to amplify small differences to CMOS levels. The circuit operates as follow, when Φ is low, $M_5$ is 'off', $S_1$ and $S_2$ are 'on', and the latch senses the input voltages $V_{in1}$ and $V_{in2}$. When Φ turns high, $S_1$ and $S_2$ turn off to isolate nodes X and Y from the input terminals and $M_5$ turns on to instigate renaissance. In order to estimate a lower bound for the offset for the latch, and in order to reduce calculations complexity, only the mismatches between $S_1$ and $S_2$, and $M_1$ and $M_2$ have been considered here. Considering only the mismatches between $M_1$ and $M_2$, and $S_1$ and $S_2$, the input offset of the latch can be expressed as [71]:

$$V_{OSM} = \Delta V_{TH} + \frac{1}{2}\left(\frac{\Delta W}{W} - \frac{\Delta L}{L}\right)(V_{GS} - V_{TH}) + \frac{\Delta Q}{C_T} \tag{3.3}$$

where, $\Delta V_{TH}$ and $V_{TH}$ are the standard deviation and mean of the threshold voltage, $\Delta W/W$ and $\Delta L/L$ are relative dimension mismatches, $V_{GS} - V_{TH}$ represents the initial gate-source override, $\Delta Q$ is the charge injection mismatch between $S_1$ and $S_2$, and $C_T$ is the total capacitance at points X and Y (equal on both sides).

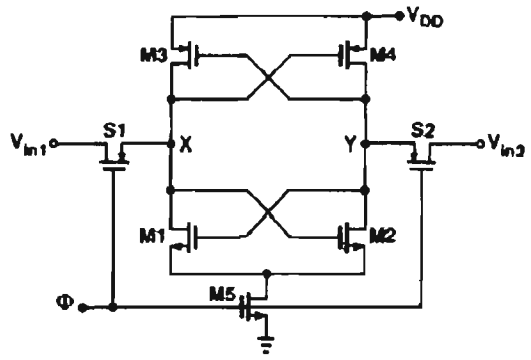



Figure 3.21: Dynamic CMOS latch [71].

The major component that arises when calculating the offset voltage is the second term in Equation 3.3. This term could be reduced by increasing $W$ and $L$ or by decreasing $V_{GS} - V_{TH}$, (i.e. decreasing the initial drain current of $M_1$ and $M_2$). Conversely, these preparations can degrade the speed of the latch by increasing the regeneration time constant $\tau_{GR}$. Therefore,

$$\tau_{GR} = \frac{C_T}{g_m} \tag{3.4}$$

where, $g_m$ is the initial transconductance of $M_1$ and $M_2$. The delay-offset artifact of this latch presumes the following outline [71]:

$$\tau_{GR} V_{OSM} = \Delta V_{TH} \frac{C_T}{g_m} + \left( \frac{\Delta W}{W} - \frac{\Delta L}{L} \right) \cdot (V_{GS} - V_{TH}) \frac{C_T}{g_m} + \frac{\Delta Q}{g_m} \tag{3.5}$$

If $C_T$ is assumed to only include the gate-source capacitance of $M_1$ and $M_2$, then Equation 3.5 can be reduced to a simpler form, as shown below in Equation 3.6:

$$\tau_{GR} V_{OSM} = \sqrt{\frac{WC_{ox}}{6 \mu_n I_D}} L^{3/2} \Delta V_{TH} + \frac{1}{3} \left( \frac{\Delta W}{W} - \frac{\Delta L}{L} \right) \frac{L_2}{\mu_n} + \frac{\Delta Q}{g_m} \tag{3.6}$$

where, $I_D$ is the initial drain current of $M_1$ and $M_2$, which is determined by the dimensions of $M_5$ and the high level of $\phi$, $\mu_n$ is the electron mobility and $C_{ox}$ is the oxide capacitance. It can be noted in Equation 3.6 that by increasing $L$, $\Delta L/L$ decreases.

When designing a Pipeline ADC, our aim is to achieve as high speed as possible. The speed of the Pipeline ADC is dependent on the sub-ADC within the Pipeline ADC,

which is usually a flash ADC. Within the flash ADC, a comparator operating at high speeds must be designed. Out of the few comparator architectures available, it is recommended in a Pipeline ADC that the comparator is designed with low-gain, and it possesses the open loop amplifier topology, cascaded with a latch.

## 3.4 Operational Amplifier Circuits

The operational amplifier, which is part of the multiplying DAC, is a very decisive component of any pipeline stage. The operational amplifier usually determines the speed of the final ADC. The open loop DC-gain of the amplifier sets a perimeter on the settling accuracy of the amplifier output, while the bandwidth and slew rate of the amplifier verify the maximal operating clock frequency. To maximise the SNR of the ADC, the amplifier should employ a large signal swing at the output.

For high-resolution and high-speed pipeline ADC designs, a large open loop DC-gain, a wide bandwidth and a high slew rate are a necessity for the amplifier. These requirements could be met by using one-stage amplifier, with folded and telescopic topologies. High open loop DC-gain can also be achieved by using multi-stage amplifier and Miller compensated amplifier. In multi-stage amplifiers, a trade off in the frequency compensation exists between the stability and bandwidth.

### 3.4.1 Telescopic Cascode Amplifier Design

The most basic design for a high-gain operational amplifier is the one-stage telescopic cascode amplifier, shown in Figure 3.22 [72].

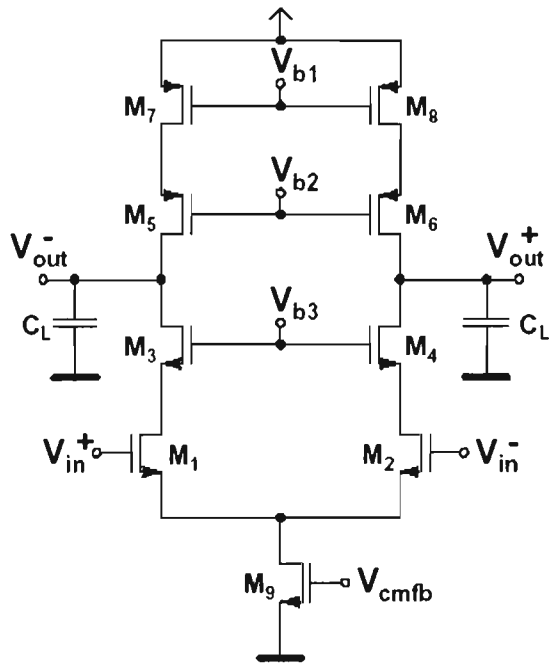



Figure 3.22: Telescopic cascode amplifier circuit [72].

With this architecture, a high open loop DC-gain can be achieved. This topology is also capable of achieving high speed when closed loop gain is low. An advantage of the single-stage architecture is the low power dissipation. However, a big disadvantage is its low maximum differential output swing ($V_{LMDS}$), which is represented by [72]:

$$V_{LMDS} = 2 \cdot V_{dd} - 10 \cdot V_{ds,sat} - 6 \cdot V_{safety} \tag{3.7}$$

where $V_{safety}$ is a safety margin added to $V_{ds,sat}$, $V_{dd}$ is the supply voltage and $V_{ds,sat}$ is the saturation voltage of a transistor.

The gain bandwidth ($G_{BW}$) of the amplifier is given by [72]:

$$G_{BW} = \frac{g_{m1,2}}{C_L} \tag{3.8}$$

where $g_{m1,2}$ is the transconductance of transistors $M_1$ and $M_2$ and $C_L$ is the load capacitance. Therefore, the $G_{BW}$ is restricted by the load capacitance. Due to the simple topology and dimensioning, the telescopic cascode amplifier would be selected for a particular application, if its output swing were large enough for that specific application.

In order to preserve the good common mode rejection ratio (CMRR) and power supply rejection ratio (PSRR) properties of the topology, additional feedback circuits for compensation have to be added to these variations.

### 3.4.2 Folded Cascode Amplifier Design

The output swing of this amplifier design is controlled by its cascoded output stage. Considering the safety margins, and the $V_{ds,sat}$ needed across the cascode instances, the differential output swing is given by:

$$V_{OS} = 2 \cdot V_{dd} - 8 \cdot V_{ds,sat} - 4 \cdot V_{safety} \tag{3.9}$$

The frequency response of this amplifier architecture is worse than that of the telescopic cascode amplifier because of a smaller transconductance of the p-channel device and a larger parasitic capacitance. The power consumption of the folded cascode amplifier is equivalent to that of a two-stage amplifier. However, due to the folded architecture, there is a larger period of freedom in trading between the input and output stage currents, gain and bandwidth.

Gain boosting by using regulation amplifiers can also be applied in the folded cascode amplifier architecture. Adding cascode transistors above the input differential pair could also increase the DC-gain. However, the enhancement in the gain is not enough for a high-resolution pipeline ADC [73]. The open loop DC-gain of amplifiers having cascode transistors can be boosted by regulating the gate voltages of the cascode transistors [74]. The selection of the feedback amplifier topology also has a physically powerful effect on the reduction of the output swing of this amplifier. Indicated in Figure 3.23 [74], the feedback amplifier input voltage is equivalent to the drain-source voltage of the transistor $M_1$. A more rigorous performance restriction of a regulated cascode amplifier can be obtained in S/H circuits where the amplifier enters slewing. From the settling behavior of a characteristic cascode amplifier in a feedback arrangement, it can be observed that after the beginning of the slewing, there is a delay prior to the amplifier operating again. This delay makes the settling of the amplifier output slower, which may cause problems in S/H circuits with fairly high voltage swings.

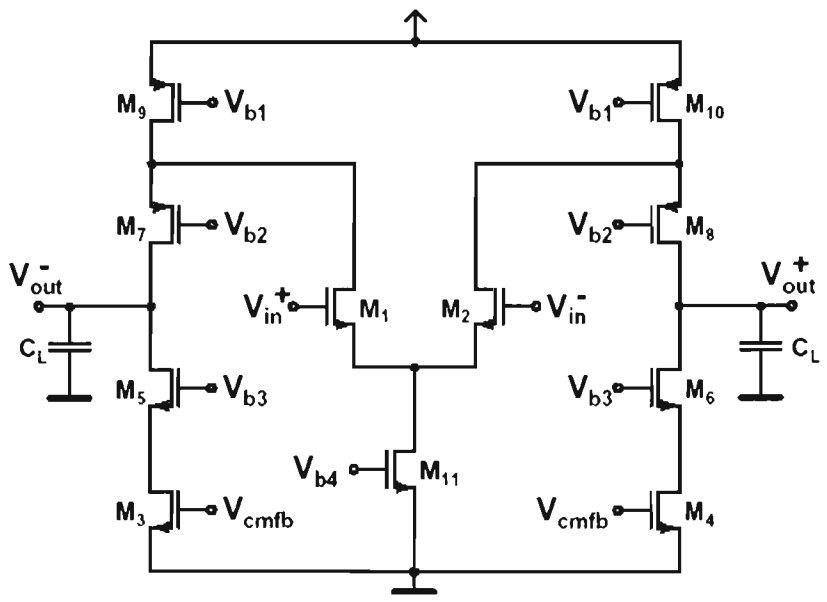



Figure 3.23: Folded cascode amplifier [74].

### 3.4.3 Miller Amplifier Design

Out of the numerous different two-stage amplifiers, Figure 3.24 shows a standard Miller compensated amplifier [75, 76]. With all of the instances in the output stage of this amplifier placed in the saturation region, it has a differential output swing given by [75]:

$$V_{OS} = 2 \cdot V_{dd} - 4V_{ds,sat} \tag{3.10}$$

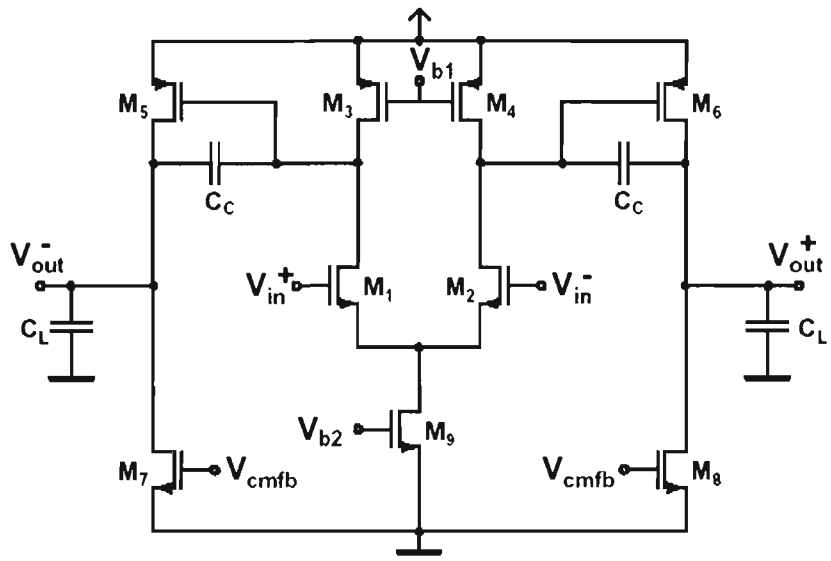



Figure 3.24: Two-Stage Miller Amplifier [75].

The gain bandwidth product ($G_{BW}$) of a Miller compensated amplifier is given approximately by [75]:

$$G_{BW} = \frac{g_{m1,2}}{C_C} \tag{3.11}$$

where $g_{m1,2}$ is the transconductance of $M_1$ and $M_2$. This constraint restricts the bandwidth of a Miller compensated amplifier. In broad-spectrum, the open loop DC-gain of the vital arrangement is not large enough for high-resolution applications.

Another drawback of this architecture is a poor power supply rejection at high frequencies because of the connection of $V_{dd}$ through the gate-source capacitance.

## 3.5 Digital-to-Analog Converter Architectures

Digital-to-analog converters (DACs) for use in pipeline ADCs can be designed using a number of different topologies. Each topology has a range of strengths and weaknesses, which can be summarised by the following criteria: integral non-linearity, differential non-linearity, chip area (in terms of die size), settling time, and matching requirements. This section briefly examines the different architectures and discusses their advantages and disadvantages.

### 3.5.1 Charge Division Architecture

A typical charge division circuit is shown in Figure 3.25. Capacitors $C_1$ to $C_N$ are all identical, and their bottom plates can switch between $V_{REF}$ and ground, allowing each capacitor to inject an amount of charge $\left(Q = C \cdot V = C \cdot V_{REF}\right)$ onto the output node. Each switch is controlled by the digital thermometer code, and hence the number of nodes turned 'on' determines the charge on the output node.

The circuit operates in two stages. In stage one, the switch $S_P$ turns 'on' and all the capacitor bottom nodes are connected to ground. This discharges the array of capacitors. In stage two, $S_P$ turns 'off', and the digital thermometer code is applied to individual switches. This applies $V_{REF}$ to all the capacitors up to the height of the thermometer code. The voltage on the output node is [76]:

$$V_{out\_node} = \frac{(j \cdot V_{REF})}{N} \tag{3.12}$$

where $j$ is the "height" of the thermometer code and $N$ is the total bit number.

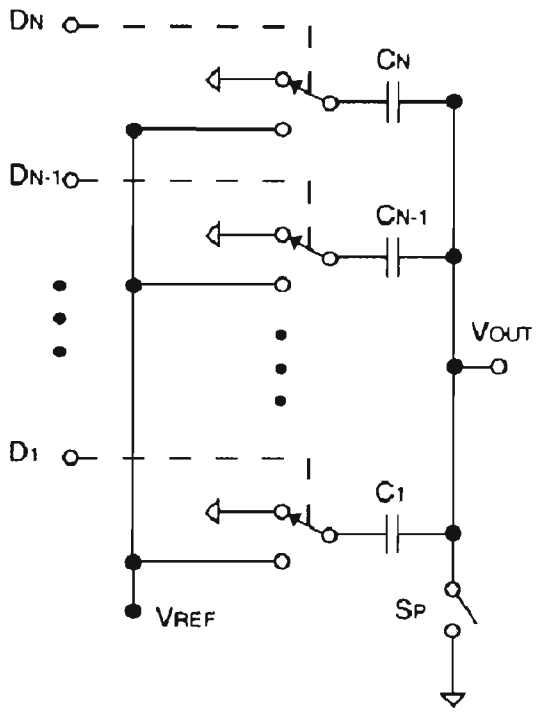



Figure 3.25: Typical charge division DAC architecture [76].

Clearly, the timing and control logic for charge division digital-to-analog converters is significantly more complex than that of resistor-ladder architectures. Another significant problem with charge division architectures is that building decently sized capacitors in CMOS takes a substantial amount of chip area. Finally, several additional nonlinearities arise, including capacitor voltage dependence and the nonlinearity of the junction capacitance connected to the output node. Implementing this topology would have used the most area consuming and relatively imprecise, therefore it was ruled out as a possible contender for the reconfigurable pipeline ADC design.

### 3.5.2 Current Division Architecture

The current division design is another reference division topology. Just like the charge division architecture, it operates by dividing a reference current among several transistors, and then selecting among the various current outputs. A typical architecture of the current division DAC is shown in Figure 3.26 [77].

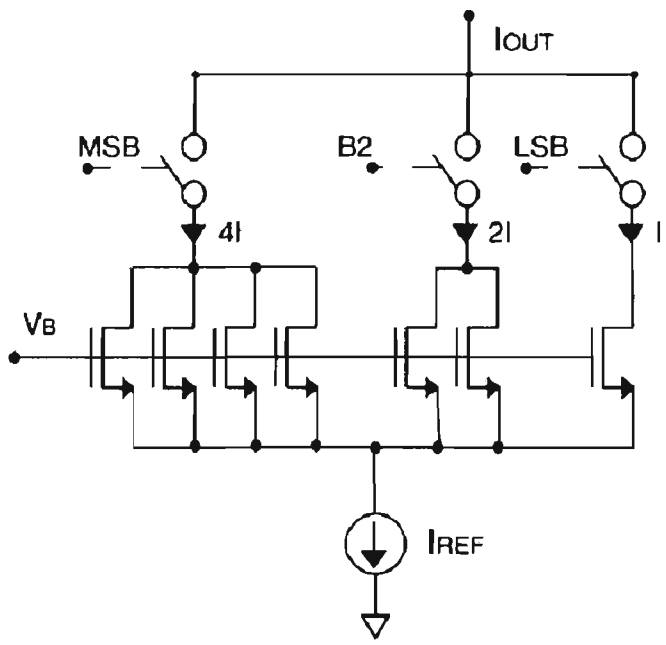



Figure 3.26: Current division DAC architecture [77].

The four devices on the leftmost side draw 4/7 of the reference current, while the center and right sides draw 2/7 and 1/7 of the reference, respectively. The digital input then turns 'on' some of the nodes, which pass their current (1I, 2I, or 4I) to the output node. The selected currents are summed, giving the analog current representation of the digital input. Sometimes a voltage output is desired rather than a current output, and to convert the output to a voltage simply requires attaching a resistor between the output node and the power supply.

There are two major disadvantages with current division topologies. First, the stack of current dividing transistors positioned above $I_{REF}$ reduces the available output voltage range, and therefore can be impractical in low voltage circuits. This is precarious, because if the output voltage decreases enough, the current dividers may go out of saturation. Secondly, since each device divides the reference current, $I_{REF}$ must be $N$ (the total number of input levels) times greater than each of the output currents. This can require a huge device to provide the current source.

### 3.5.3 Resistor-Ladder Architecture

The resistor-ladder architecture is a string of resistors in series, with the 'top' resistor tied to power and the 'bottom' resistor connected to ground, as shown in Figure 3.27 [78].

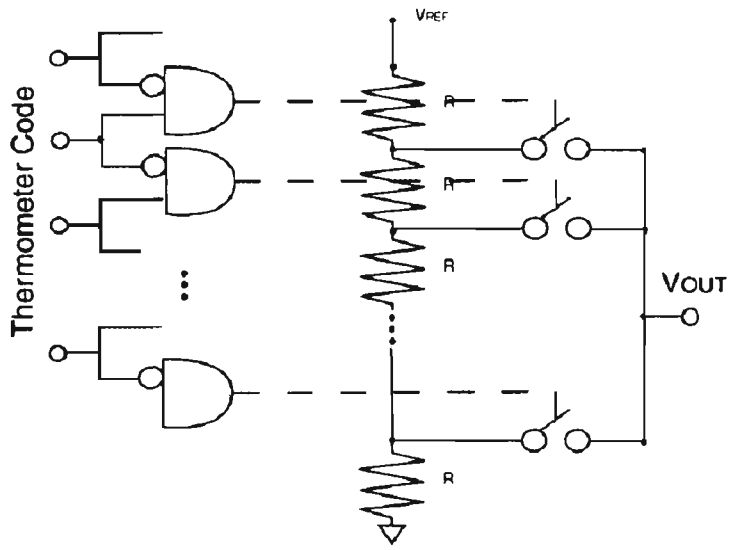



Figure 3.27: Resistor-Ladder DAC with thermometer decoding [78].

The nodes in between each resistor have different voltages depending on their proximity to power. Nodes that are higher in the ladder have higher voltages, and by using

thermometer or binary decoding on the digital signal one specific node can be selected as the correct analog voltage. The number of resistor elements determines the resolution of the resistor-ladder DAC. An $M$-bit DAC requires a ladder with $2^M$ resistors.

Resistor-ladder DACs have some other advantages besides being simple to design. They are naturally monotonic as long as the switching elements are designed correctly, and their differential non-linearity (DNL) and integral non-linearity are relatively low compared to other architectures. Due to these advantages, the resistor-ladder DAC is a good candidate to be used within the pipeline ADC.

## 3.6 Proposed Circuit Techniques for most Critical Components in ADC Design

This section describes and analyses the two most critical circuit designs used within the pipeline ADC architecture, which are the sample-and-hold (S/H) circuit and the dynamic comparator.

### 3.6.1 Proposed Sample-and-Hold Circuit

The proposed S/H circuit employed within the pipeline ADC architecture is a modification to the S/H illustrated in Figure 3.28 [76]. Before analysing the proposed S/H circuit, illustrated in Figure 3.29, the S/H circuit of Figure 3.28 must first be understood.

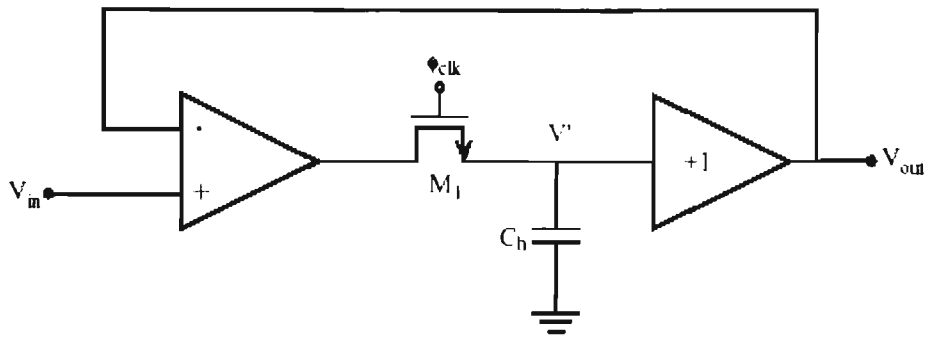



Figure 3.28: S/H circuit with an op-amp in a feedback loop [79]

When the clock $\phi_{clk}$ is high, the complete circuit responds similarly to an op-amp in a unity-gain feedback configuration. When $\phi_{clk}$ goes low, the input voltage at that time is stored on $C_h$, similarly to a simple S/H. By including an op-amp in the feedback loop, the input impedance of the S/H is greatly increased. Another advantage of this configuration is that even if the unity-gain buffer at the output has an offset voltage, the DC error due to this buffer will be divided by the gain of the input op-amp, although the input offset of the input op-amp will remain. Thus, very simple source followers can be used for the output buffer.

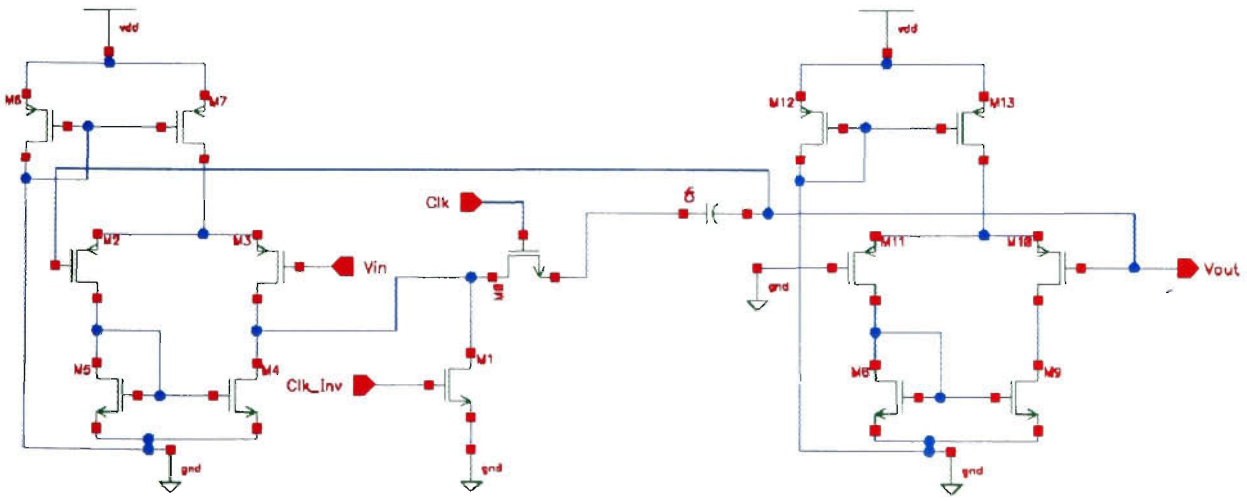



Figure 3.29: Proposed Sample-and-Hold Circuit

In the design of Figure 3.29, the holding capacitor is not directly connected to ground, but it is placed in the feedback loop with another op-amp. Assuming the second op-amp has a large gain, the input to the second op-amp is basically at zero volts. Therefore, the voltages on both sides of switch $M_0$ are nearly signal independent. Thus, when $M_0$ turns 'off', there still be charge injection and clock feed-through to the left side of $C_h$.

However, it is only going to be a DC offset and will be signal independent and cause no distortion. In addition, because the voltages on both sides of the switch $M_0$ is fixed close to ground, the finite clock rise time and fall time will not cause any sampling jitter.

Another advantage of this design as compared to the design of Figure 3.28 is due to the inclusion of $M_1$. This switch has two main benefits. It grounds the output of the first op-amp during the hold operation. During the sample operation, the voltage at this node has to go to the inverting input of the second op-amp, which is also close to ground. Therefore this approach reduces the voltage swing at this node when the S/H goes from hold operation to sample operation, and hence speeds up the acquisition time. The switch also minimises the signal feed-through when the S/H is in hold operation by grounding the signal path. The analysis results of the proposed S/H circuit are shown in Table 3.1.

Table 3.1: Proposed Sample-and-Hold Results

| **Property** | **Result** |
|---|---|
| Sampling Rate | 15.36 MSPS |
| SFDR | 64 dBc |
| Signal swing | 1.3 V |
| Supply Voltage | 2.5 V |
| Power Consumption | 0.22 mW |
| Technology | 0.18μm CMOS |

### 3.6.2 Proposed Comparator Circuit

This section describes the design of the latch comparator used in the proposed ADC architecture. In an ADC, comparators are the most critical components that directly affect the ADC overall performance. Their input offset voltage, delay and input range directly influence the resolution and speed of the ADCs. Fundamental function of comparators is to compare an input signal ($V_{in}$) with a reference signal ($V_{Ref}$) and then to generate the high logic value when $V_{in}>V_{Ref}$ and low logic value when $V_{in}<V_{Ref}$. The proposed comparator consists of a CMOS latch amplifier circuit and an S-R latch circuit hugging the CMOS latch amplifier, as illustrated in Figure 3.30. The CMOS latch circuit consists of a differential pair using PMOS switches ($M_0$, $M_1$ and $M_2$) and a cross-coupled circuit using NMOS transistors ($M_9$, $M_{11}$). The roles of PMOS switch transistors ($M_3$ and $M_4$) and NMOS switch transistors ($M_{10}$ and $M_{12}$) are to isolate the differential pair and the cross-coupled pair and to discharge the drains of $M_9$ and $M_{11}$ to ground to keep the output unchanged of S-R latch circuit ($M_5$, $M_6$, $M_7$, $M_8$, $M_{13}$, $M_{14}$, $M_{15}$, $M_{16}$) during the re-charge mode. The comparator operation is described as follows: In re-charge mode (when the clock signal is high), the differential pair and cross-coupled circuit are isolated. The drain gates of the NMOS transistors are pulled to ground while the drain gates of the positive-channel metal oxide semiconductor (PMOS) transistors are pulled to $V_{DD}$. When the clock signal goes low, $M_0$ acts as a current source providing current $I_D$ given by:

$$I_D = \frac{k}{2}\frac{W}{L}(V_{bias} - V_{DD} - V_T)^2 \tag{3.13}$$

where $k = \mu_P C_{ox}$, $V_{bias}$ is the bias voltage, $V_T$ is threshold voltage, $W$ is the width of that particular transistor, and $L$ is the corresponding length of the transistor.

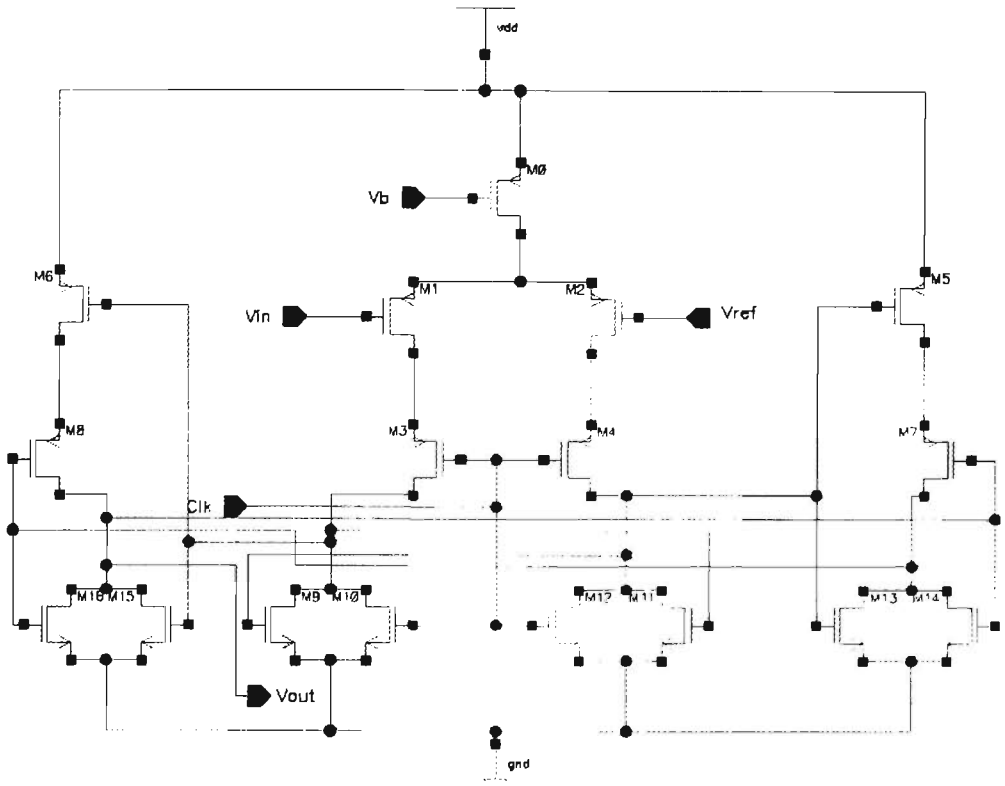



Figure 3.30: Dynamic Comparator Circuit

The voltage difference between $V_{in}$ and $V_{Ref}$, will induce difference currents $I_{D1}$ and $I_{D2}$ flowing in two perfectly matched PMOS transistors ($M_1$ and $M_2$). These currents are represented as follows [80]:

$$I_{D1} = \frac{I_D}{2} + \frac{kW}{4L}\Delta V \cdot \sqrt{\frac{4I_D}{k\left(\frac{W}{L}\right)} - \Delta V^2} \tag{3.14}$$

$$I_{D1} = \frac{I_D}{2} - \frac{kW}{4L}\Delta V \cdot \sqrt{\frac{4I_D}{k\left(\frac{W}{L}\right)} - \Delta V^2} \tag{3.15}$$

where $\Delta V = V_{in} - V_{Ref.}$

These different currents create the regeneration process of the NMOS switches $M_9$ and $M_{11}$. The regeneration process could be further explained by the help of Figure 3.31.

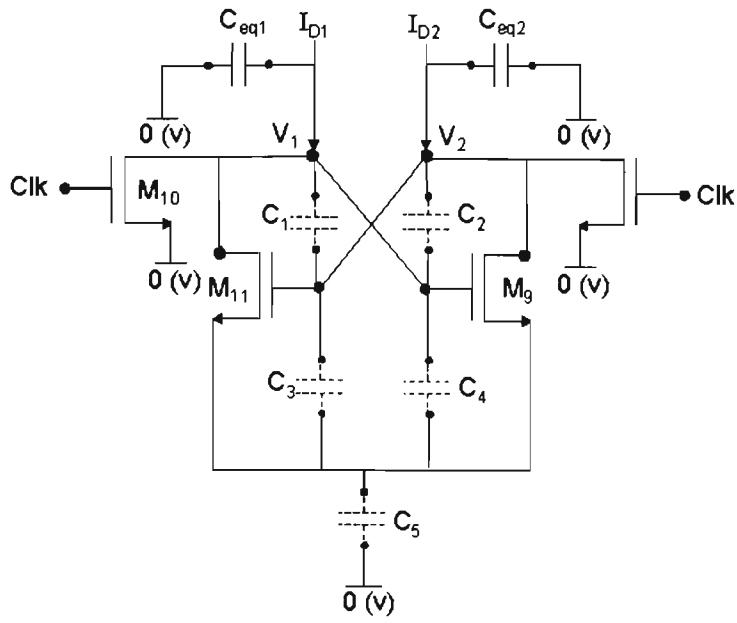



Figure 3.31: Cross coupled pair of comparator

The capacitors $C_1$ through $C_5$ are lumps into $C_{eq1}$ and $C_{eq2}$. This approximation is valid because grounded capacitance has dominant value and one can represent the much smaller coupling capacitance due to the Miller effect [81]. The inputs currents initially charge the input capacitances $C_{eq1}$ and $C_{eq2}$, while switches $M_{10}$ and $M_{12}$ are turned off. The rising of gate voltage of switches $M_9$ and $M_{11}$ will increase the drain current. The regenerative action starts when the closed-loop gain through switches $M_9$ and $M_{11}$ become greater than one [81]. This gain is given by:

$$gm_9 \cdot R_{L9} \cdot gm_{11} \cdot R_{L11} > 1 \qquad (3.16)$$

where $R_{L9}$ and $R_{L11}$ are the load resistances of transistor $M_9$ and $M_{11}$ respectively. This phenomenon occurs when both $M_9$ and $M_{11}$ are in deep subthreshold region. The regenerative action starts when [81]:

$$\frac{I_{DM9} \cdot I_{DM11}}{I_{D1} \cdot I_{D2}} > (\lambda \cdot \xi \cdot V_t)^2 \approx 3 \times 10^{-6} \quad (3.17)$$

where parameter λ is a linear function of effective channel length and $V_t$ is the threshold voltage. Suppose that $V_{in} > V_{Ref}$ then $I_{D1} < I_{D2}$, therefore $V_2$ will rise faster than $V_1$. Due to the regenerative action, increasing $V_2$ will further decrease $V_1$. When $V_2 > V_1 + V_T$ the NMOS $M_{11}$ will go to saturation mode, thus it will pull voltage $V_1$ to ground, where NMOS $M_9$ will be cut-off, and hence $V_2$ will be pulled up to $V_{DD}$. Figure 3.32 illustrates the regeneration process.

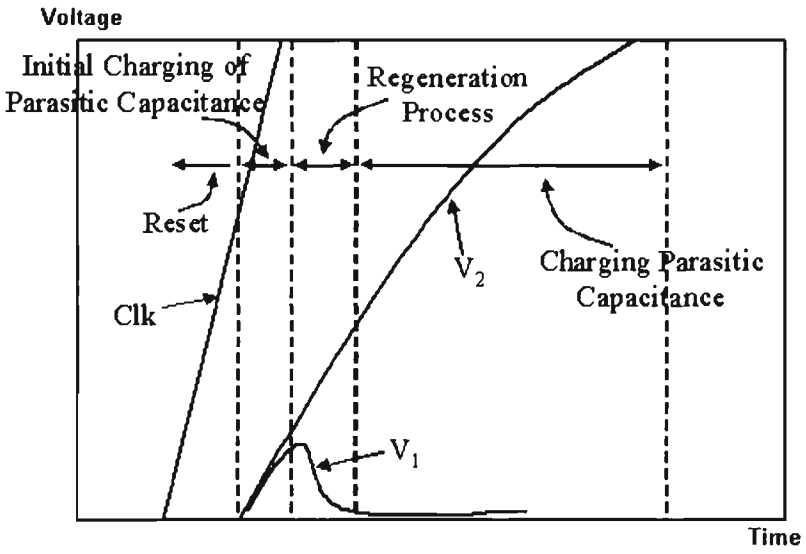



Figure 3.32: Regeneration Process [81].

### 3.6.2.1 Comparator Optimisation

The proposed comparator offers three main advantages, namely high speed, small device size and minimal static power dissipation. However, the offset error of this comparator is typically large. The reason for this is because when $V_{in}$ and $V_{Ref}$ are approximately equal to each other, roughly equal input currents to the regeneration

stage will be produced. This scenario will require longer time for the voltage difference between $V_1$ and $V_2$ to reach the threshold voltage to saturate either $M_9$ or $M_{11}$. This offset error of the comparator could be reduced by optimising the *W/L* ratios of the PMOS and NMOS transistors.

#### 3.6.2.1.1 PMOS Differential Pair Optimisation

By using Equation 3.14 and 3.15, the difference between the input currents to the regeneration stage can calculated to be:

$$\Delta I = I_{D1} - I_{D2} = \frac{kW}{2L} \cdot \Delta V \cdot \sqrt{\frac{4I_D}{k\left(\frac{W}{L}\right)} - \Delta V^2} \tag{3.18}$$

Figure 3.33 illustrates the offset voltage against the *W/L* ratio of the PMOS switches in the differential pair at 500 MHz. When the *W/L* ratios of the PMOS differential pair are increased, the $\Delta I$ to saturate $M_9$ and $M_{11}$ also increases. Under this condition the offset error will be reduced. However, if the *W/L* ratios of the differential pair are large, this will make currents $I_{D1}$ and $I_{D2}$ also large, resulting in $V_1$ and $V_2$ reaching high logic levels which will disable the S-R latch before the regeneration takes place.

This will increase the offset voltage, therefore maintaining the proper function of the dynamic comparator.

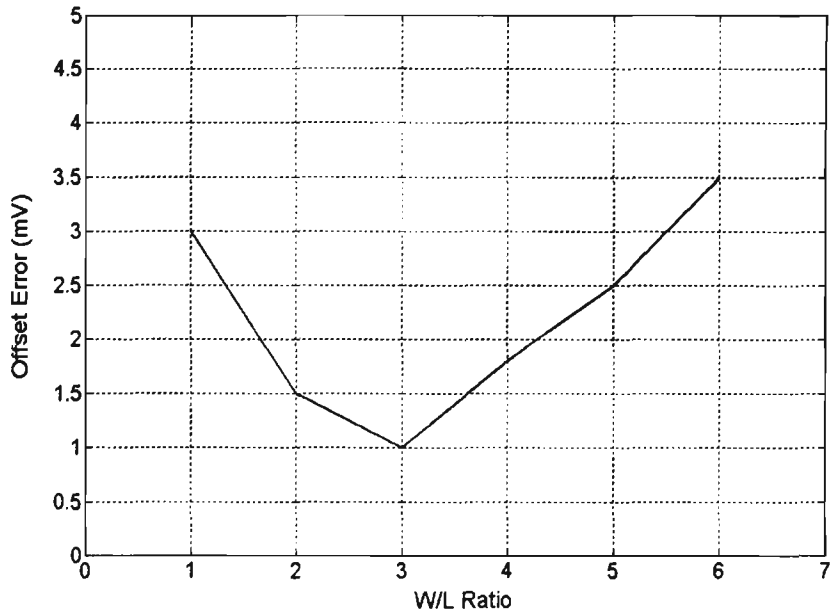



Figure 3.33: Optimisation of PMOS transistor pair

Hence, the offset error initially decreases as the *W/L* ratios are increased, and then as the *W/L* ratios are further increased, the offset error increases. The optimised *W/L* ratios of the PMOS transistors are obtained when the offset error of the comparator is at its minimum value of 1mV. Table 3.2 shows the appropriate *W/L* ratios of these transistors.

Table 3.2: W/L Ratios of the PMOS transistors

| **Transistors (Figure 3.30)** | **W/L Ratio** |
|---|---|
| $M_0$ | 5.6 |
| $M_1$ | 2.94 |
| $M_2$ | 2.94 |

#### 3.6.2.1.2 NMOS Regeneration Circuit Optimisation

The switching time of a transistor is given by [80]:

$$T_S = \frac{1}{f_T} = 2\pi \cdot \frac{V_T \cdot WL \cdot C_{js}}{I_D} \tag{3.19}$$

where $f_T$ is the switching frequency and $C_{js}$ is the source junction capacitance. Reducing the lengths and widths of $M_{10}$ and $M_{12}$ will produce smaller switching time, however this will be greatly influenced by the technology used. For the cross-coupled pair of the comparator, the drain current $I_D$ of the NMOS transistor in the subthreshold region is given by [80]:

$$I_D = \frac{W}{L} \cdot qXD_n \cdot n_{po} \cdot e^{\left(k+\frac{V_t}{n}\right)} \cdot e^{\left(\frac{V_{GS}-V_T}{nVt}\right)} \cdot \left(1 - e^{\frac{V_{DS}}{V_t}}\right) \tag{3.19}$$

where $W$ is the width, $L$ is the length, $XD_n$ is the depletion-layer width, and $q$ is the charge. By increasing the $W/L$ ratios of the NMOS transistors will produce larger $I_D$ and therefore the regeneration process will begin sooner than as stated by Equation 3.17. Figure 3.34 illustrated the offset voltage as a function of the $W/L$ ratios of the NMOS transistors in the regeneration circuit.

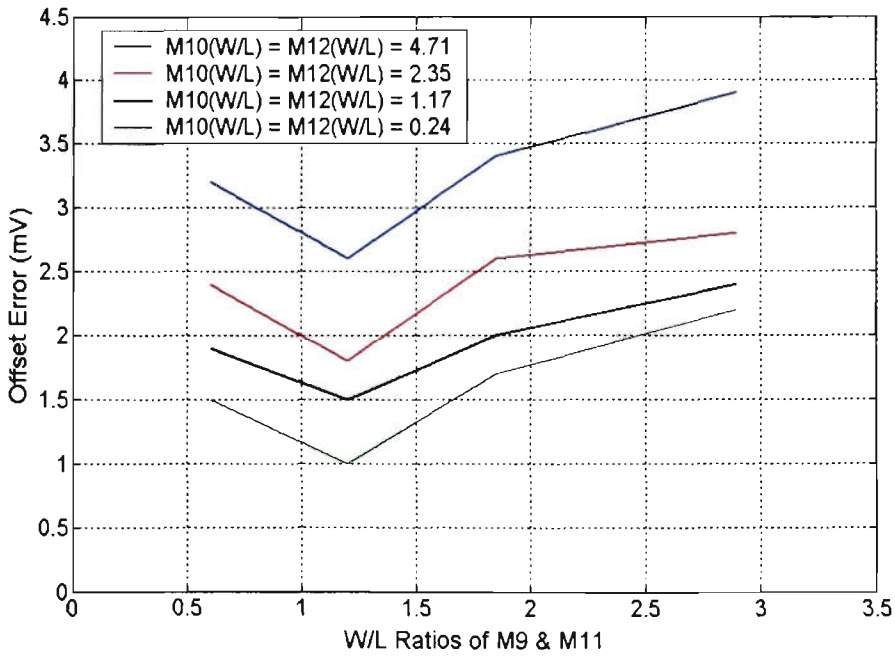



Figure 3.34: Optimisation of NMOS regeneration circuit

As the lengths and widths of $M_{10}$ and $M_{12}$ are decreased, the comparator offset error reduces accordingly. While the *W/L* ratios of $M_9$ and $M_{11}$ are increased, the offset error initially is reduced, and as the *W/L* ratios are further increased, the offset error is also increases. Table 3.3 presents the NMOS transistor values for minimum offset error.

Table 3.3: *W/L* Ratios of Regeneration circuit transistors

| **Transistors (Figure 3.30)** | **W/L Ratio** |
|---|---|
| $M_9$ | 1.18 |
| $M_{10}$ | 0.24 |
| $M_{11}$ | 1.18 |
| $M_{12}$ | 0.24 |

#### 3.6.2.1.3 S-R Latch Optimisation

The most critical optimisation of the comparator circuit is the optimisation of the S-R latch circuit. It is the S-R latch that holds the output of the comparator when the comparator is in recharge mode. The information is required to be ready at the output of the S-R latch before the comparator changes to the recharge process. Thus, the smaller the delay time of the S-R latch, the more accurate the result would be.

The rise time and fall time of the output signals must be balanced, therefore optimisation of the S-R latch involves minimising the widths and lengths of the NMOS and PMOS transistors while maintaining balanced rise and fall time. At almost perfectly balanced rise time and fall time, the *W/L* ratios of the transistors within the S-R latch are shown in Table 3.4.

Table 3.4: W/L Ratios of S-R Latch

| Transistors (Figure 3.30) | W/L Ratio |
|---|---|
| $M_5$ | 1.25 |
| $M_6$ | 1.25 |
| $M_7$ | 1.25 |
| $M_8$ | 1.25 |

### 3.6.2.2 Comparator Analysis

Optimisation strategies, such as the ones described above will reduced the offset error of the dynamic comparator at certain sampling frequencies. However, the sampling frequency has a rather big influence on the offset error. Figure 3.35 illustrates the offset error of the comparator as a function of various sampling frequencies.

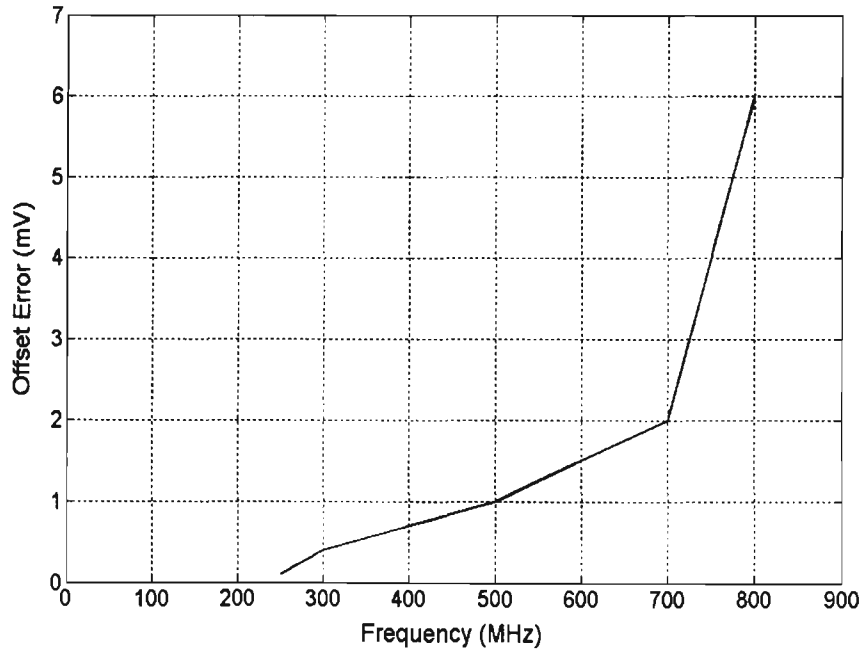



Figure 3.35: Comparator Offset Error as function of Frequency

From Figure 3.35, it can be seen that for frequency less then 250 MHz, the offset error is less than 100 μV, and only 1mV at 500 MHZ. The offset error is fairly linear between

the range of 250MHz and 700MHz. Once the sampling frequency goes beyond 700MHz, there is a fast increase by the offset error. Table 3.5 summarises the most critical results of the dynamic comparator, from an ADC point of view.

Table 3.5: Comparator Results at 2.5V supply

| **Property** | **Result (At 500 MHz)** | **Result (At 15.36 MHz)** |
|---|---|---|
| Maximum Operating Frequency | 800 (MHz) | |
| Power Consumption | 280.5 (μW) | 27.62 (μW) |
| Noise Figure | 4.48 (dB) | 3.2 (dB) |
| Offset Error | 1.05 (mV) | < 50 (μV) |

The performance results of the proposed CMOS comparator analysed in Table 3.5 are significantly better than expected in accordance to the required speed of 15.36 MHz and a noise figure of less than 4.5 dB. In comparison to other implementation [27-29], the results of Table 3.5 indicate a considerable improvement in speed and a decrease in power consumption.

## 3.7 Conclusion

This chapter discussed the implication of the building block components of specific circuits within the pipeline ADC to satisfy the design requirements of this ADC. Mutli-step ADCs employ a sample-and-hold circuit at the front end of the overall topology. The S/H circuit must achieve high speed and high linearity with low power

consumption. Additionally, sampling circuits can be used to improve the timing and bandwidth boundaries of one-step converters such as flash architectures.

On the other hand, design of fast exactness comparator circuits requires vigilant trade-offs among parameters such as speed, power consumption, and resolution. The resolution of a comparator circuit is inhibited by the input offset of its latch, while the speed is often limited by the preamplifier override recovery. From this statement, it can be summarised that if the latch offset is reduced in a reliable way, the preamplifier can be designed for lower gain and therefore faster recovery. CMOS comparator techniques have been introduced, in particular the offset cancellation technique. To achieve a small residual offset, the technique combines a preamplifier circuit and a regenerative latch, both with offset cancellation. This architecture radically unwinds the preamplifier gain requirements, allowing high speed and low power consumption. This chapter also described design techniques for operational amplifiers, which are utilised for low power, high-speed, and low-voltage data converters.

# Chapter 4

# *Sub-ADC Architecture*

## 4.1 Introduction

The objective of this research is to design and implement a low power, reduced complexity reconfigurable ADC for a mobile terminal receiver. The resolution of the ADC will be scaled according to the interference experienced by the adjacent channel and co-channel interferers. This chapter exploits the findings of chapter 2, where a pipeline ADC topology, due to its good combination of high speed and low power consumption, is the most suitable ADC architecture for the mobile receiver. In a pipeline ADC, the most critical component is the sub-ADC, so careful investigation and a wise choice of what kind of sub-ADC should be used, is most important. Usually, the flash topology is employed, due to its fast speed, but because our concern here is power consumption, we managed to create new design of a modified-flash ADC. In order to get an in depth knowledge of the performance of an ADC, static and dynamic specifications for a standard ADC are also defined in this chapter. Prior to designing the sub-ADC, knowledge on the resolution of the first pipeline block is required. A

statistical analysis on the dynamic range for this design is performed, which in fact justifies the design of a 4-bit sub-ADC in the first block of the pipeline chain.

## 4.2 ADC Specifications

In order to fully understand the performance of any ADC, the specifications of the static and dynamic domains need to be addressed. Firstly, the static domain, where the integral non-linearity (INL) and differential non-linearity (DNL) of the converter is described. Secondly, the dynamic domain where the communications specifications, such as signal-to-noise ratio (SNR), total harmonic distortion (THD), effective number of bits (ENOB) and the dynamic range (DR) are described.

### 4.2.1 Static Specifications

The most considerable evaluation of static specifications of an ADC is the DNL and INL. The properties of these specifications include the quantisation error or noise ($Q_n$) of the converter, which is associated with the accuracy of the ADC. By analysing the transfer curve of an ADC, the integral non-linearity and differential non-linearity could be defined and explained.

#### 4.2.1.1 ADC Differential Non-Linearity (DNL)

The ADC differential non-linearity can be calculated from the transition voltages, which are calculated from the histogram of the captured data points, shown in Figure 4.1.

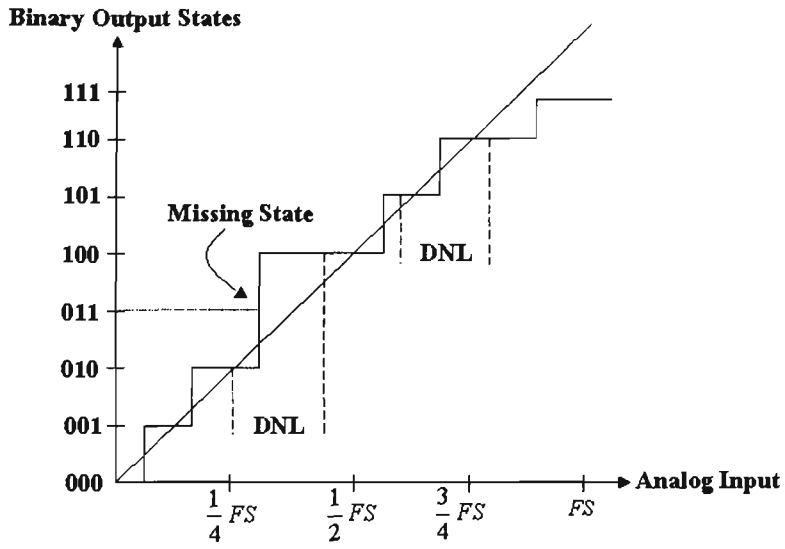



Figure 4.1: ADC Differential Non-Linearity (DNL) [82].

The DNL can be expressed as [82]:

$$DNL(j) = \frac{data[j+1] - data[j]}{device_{LSB}} - 1 \tag{4.1}$$

The $device_{LSB}$ is the least significant bit of the ADC and is expressed as:

$$device_{LSB} = \frac{data(M-1) - data(0)}{M} \tag{4.2}$$

where *data[j]* is the ADC transition voltage, $j$ is equal to 0, 1, 2 .... ($M$-2), where $M$ is the total number of points.

### 4.2.1.2 ADC Integral Non-Linearity (INL)

The ADC INL measures the deviation of each code centre point from the ideal straight line, as shown in Figure 4.2.

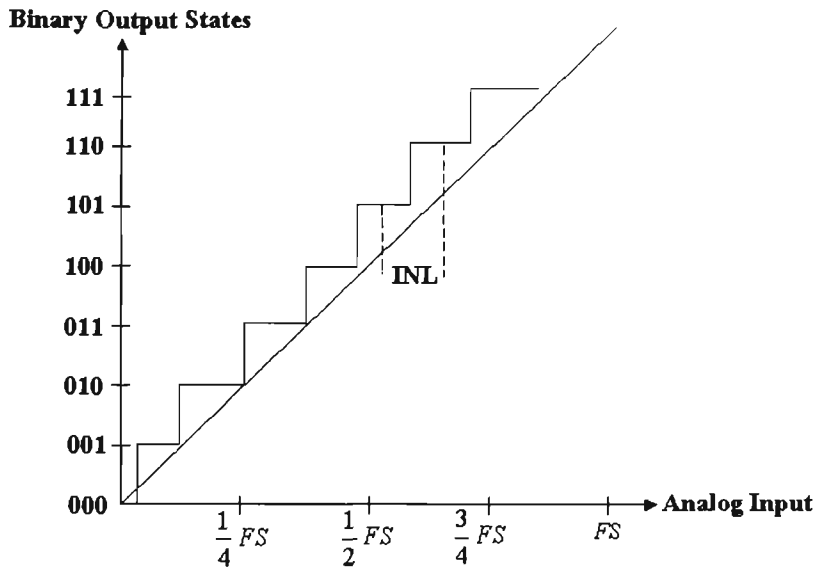



Figure 4.2: ADC Integral Non-Linearity (INL) [83].

The INL of an ADC can be expressed as follows [83]:

$$INL(j) = \frac{data[j] - (device_{LSB} \cdot j + data[0])}{device_{LSB}} \tag{4.3}$$

where the $device_{LSB}$ is also equivalent to $\frac{data(M-1) - data(0)}{M}$.

## 4.2.2 Distortion Characteristics (Dynamic Specifications)

Distortion measurement is obtained by sourcing the input sine wave to the system. The analog response is first captured and then analysed in the frequency domain. This means that the processed waveform is converted into its spectrum using the Fast-Fourier-Transform (FFT) algorithm, and the calculations are based on the frequency components.

Typical distortion measures are:

- Total Harmonic Distortion (THD)

- Signal-to-Noise Ratio (SNR)
- Signal-to-Noise plus Distortion Ratio (SNDR)
- Spurious Free Dynamic Range (SFDR)
- Effective Number of Bits (ENOB)

#### 4.2.2.1 Total Harmonic Distortion (THD)

The THD compares the combined power of the $M$ harmonics with the power of the input signal. The THD is described and calculated as the ratio of the root mean square (rms) sum of the first $M$ harmonic components, usually up to the $5^{th}$ harmonic, to the rms value of the full-scale input voltage signal ($V_{FS}$). The THD expressed in decibels (dB) is [83, 84]:

$$THD = 20 \cdot \log\left(\frac{\sqrt{\sum_{j=2}^{M} F_j^{\,2}}}{F_h}\right) \tag{4.4}$$

where $F_j$ ($j$=2.....$M$) are the harmonics of the output signal, $M$ is the number of harmonics, and $F_h$ is the fundamental of the output signal.

#### 4.2.2.2 Signal-to-Noise Ratio (SNR)

The SNR is calculated as the ratio of the rms value of the input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics. The SNR is expressed as [83, 85]:

$$SNR = 20 \cdot \log \frac{F_f}{\sqrt{\sum_{\min_{BW}}^{\max_{BW}} M_j^{\,2}}} \tag{4.5}$$

where $F_f$ is the fundamental of the input signal, $M_j$ are the spectral noise components excluding harmonics, $max_{BW}$ and $min_{BW}$ are the maximum and minimum bandwidths, respectively. Equation 4.5 could also be expressed in terms of dB for a single-tone sine signal, where SNR is given by [86]:

$$SNR = 2^M \cdot \sqrt{\frac{3}{2}} = (6.02M + 1.76) \quad \text{dB} \tag{4.6}$$

Equation 4.6 indicates that each additional bit, $M$, enhances the SNR by 6.02 dB.

#### 4.2.2.3 Signal-to-Noise plus Distortion Ratio (SNDR)

The SNDR compares the power of the input signal with the combined power of the harmonics and noise. SNDR is calculated as the ratio of the rms value of the input signal to the rms sum of all other spectral components below the Nyquist frequency ($N_f$), including harmonics. The Nyquist frequency ($N_f$) is defined as:

$$Nf = \frac{Sampling\ Frequency}{2} \tag{4.7}$$

The SNDR is expressed as [85]:

$$SNDR = 20 \cdot \log \frac{F_f}{\sqrt{\sum_{\min_{BW}}^{\max_{BW}} M_j^{\,2} + \sum_{j=2}^{M} F_j^{\,2}}} \tag{4.8}$$

where $F_f$ is the fundamental of the input signal, $M_j$ are the spectral noise components excluding harmonics, $max_{BW}$ and $min_{BW}$ are the maximum and minimum bandwidths, $F_j$ ($j$=2.....$M$) are the harmonics of the output signal.

#### 4.2.2.4 Effective Number of Bits (ENOB)

This specification is defined as the number of bits required in an ideal ADC so that the mean squared noise power in the ideal ADC equals the mean squared power of the residual error in the real ADC. ENOB defines the available resolution, which is influenced by:

- Noise
- Quantisation noise or quantisation error
- DNL and INL

A major factor is the ADC's inherent uncertainty. Even an ideal ADC produces a quantisation error, defined as a saw-tooth function and illustrated in Figure 4.3 [85].

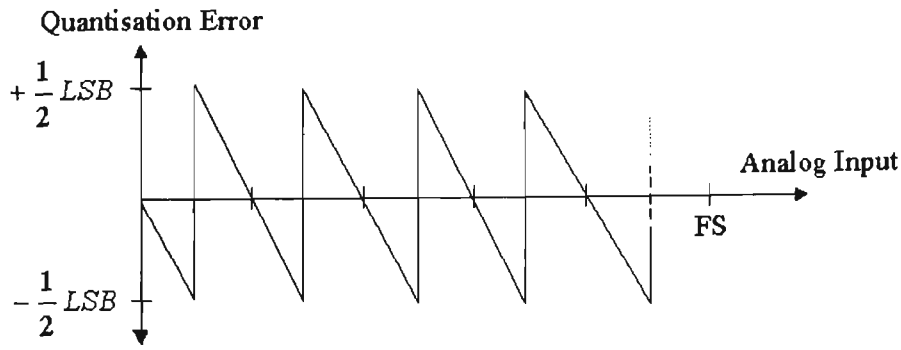



Figure 4.3: ADC Quantisation Error [85].

The quantisation error is expressed by the ENOB. For a linear ADC, this characteristic is described as:

$$ENOB = \frac{SNR - 1.76}{6.02} \tag{4.9}$$

#### 4.2.2.5 Spurious Free Dynamic Range (SFDR)

The SFDR is the ratio of the largest spectral component to the rms value of the full-scale input signal, and is described as [87]:

$$SFDR = 20 \cdot \log\left(\frac{V_{SC}}{V_f}\right) \tag{4.10}$$

where $V_{SC}$ is the voltage amplitude of the maximum spurious component, and $V_f$ is the voltage amplitude of the fundamental.

### 4.2.3 Receiver ADC Dynamic Range Analysis

The dynamic range ($DR_{ADC}$) of an ADC is the input power for which the signal-to-noise ratio of the ADC is greater than zero dB. To obtain the dynamic range the SNR as a function of the input power needs to be calculated. The number of bits can also determine the DR of an ADC.

This section presents the receiver ADC's dynamic range analysis which justifies the design of a 4-bit first stage ADC of the entire pipeline chain. Altering the word-length (bits) of the ADC can have a severe impact on the performance of the receiver if the word-length is reduced. This may occur if the DR of the ADC may be below a certain tolerance level. A dynamic range analysis with respect to a variable word-length ADC

must be investigated to determine which word-lengths will not affect the noise performance of the receiver. The relationship between $DR_{ADC}$ and the effective number of bits $N$, has been investigated in [87] and is as follows:

$$DR_{ADC} = 20 \cdot \log_{10}(2^N) \tag{4.11}$$

Equation 4.10 yields 6.02 dB of dynamic range per bit, therefore is simplified to:

$$DR_{ADC} = 6.02 \cdot N \quad [dB] \tag{4.12}$$

To obtain the corresponding effective number of bits if the dynamic range is known, N corresponds to:

$$N = \frac{DR_{ADC}}{6.02} \tag{4.13}$$

Figure 4.4 illustrates the dynamic range of the ADC with variable resolutions.

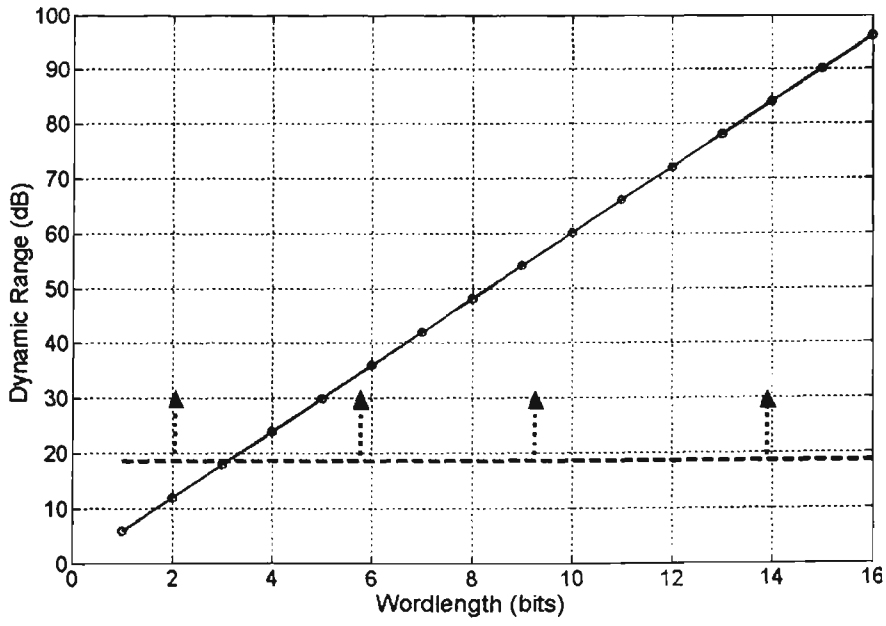



Figure 4.4: Dynamic Range Analysis of ADC

The required system signal-to-noise ratio, which needs to be met for adequate performance, is 6.5dB. An additional safety margin of 2 bits would be acceptable to combat any input spikes. Therefore, acceptable word lengths are $\geq 4$. The minimum word length is 4.

## 4.3 First Pipeline ADC Stage

The design of the first pipeline block of the reconfigurable ADC was largely influenced by the dynamic analysis of the ADC within the UTRA-TDD system. The dynamic range of the overall system, according to the UTRA-TDD specifications justified that the ADC could have any number of pipeline stages, which also determines the number of bit, as long as the minimum resolution is 4-bits. This was justified by Figure 4.4. From this analysis, highest degree of emphasis must be given to the sub-ADC of the pipeline architecture, because it is this block that produces the digital output. Usually a flash ADC topology is used as a sub-ADC of the pipeline, but as described in the literature review, chapter 2, this design dissipates a lot of power. Therefore a modified flash architecture has been implemented and compared in terms of power consumption with the typical flash ADC and the two-step ADC.

### 4.3.1 Sub-ADC (Modified Flash) Architecture

When speed is the first priority in the design process of an ADC, flash topology ADC is considered as first choice, but when we add the complexity of the flash ADC, we are forced to compromise between performance and complexity. The following steps are used to design the new 4-bit flash ADC.

(i) Start with $2^{(N-2)} + 2$ comparators and label them in ascending order, as shown in Figure 4.5. The analog input voltage $V_{in}$ is connected to the non-inverting inputs of all the comparators and the inverting input of the MSB comparator is set to $8V_{Ref}/16$, $4V_{Ref}/16$ and $12V_{Ref}/16$.

(ii) The outputs of these 3 comparators are used to control the switches, which are connected to the appropriate fractions of the reference voltage, $V_{Ref}$.

(iii) The outputs of the comparators ($Comp_4$, $Comp_5$, $Comp_6$) are encoded into appropriate values as shown in Table 4.1.

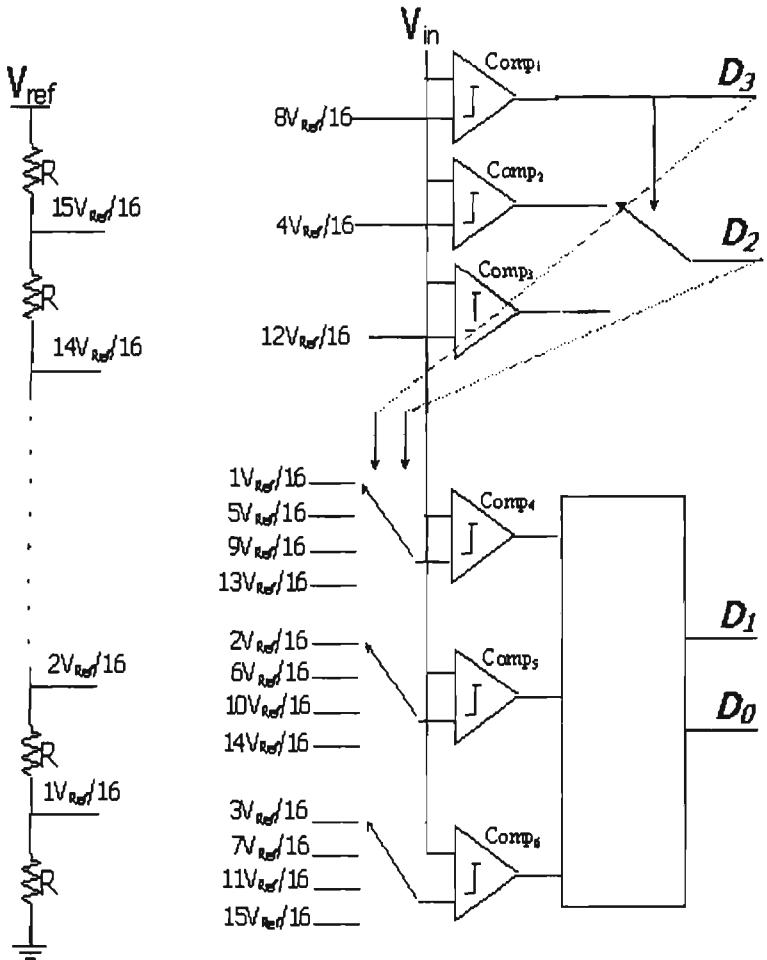



Figure 4.5: Modified-Flash ADC Architecture

Table 4.1: Relationship between comparator outputs and ADC outputs

| O15 | O14 | O13 | O12 | O11 | O10 | O9 | O8 | O7 | O6 | O5 | O4 | O3 | O2 | O1 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

$O_8 = 1, O_{12} = 1$

$O_8 = 1, O_{12} = 0$

$O_8 = 0, O_4 = 1$

$O_8 = 0, O_4 = 0$

The main advantage of the modified flash ADC approach is the reduction of comparators, which is most critical and the most area-consuming component in the flash ADC design. For $N$-bit of resolution, the modified ADC architecture requires only $(2^{(N-2)}+2)$ comparators, comparing to $2^N$-1 comparators required by the full flash ADC topology. Also, the modified flash ADC requires a much less complex encoder, than that of the traditional full flash ADC. The encoder logic expressions for the modified-flash ADC are described below:

$$\begin{aligned} D_1 &= O_5 \\ D_0 &= O_5 + \overline{O_6}.O_4 \end{aligned} \tag{4.14}$$

where $O_i$ is the output of comparator $i$.

It should be observed that intentionally the output of the second comparator ($Comp_2$) is switched instead of switching its input in the modified flash ADC. Although a comparator will be saved if we switch the input of $comp_2$, the speed of the system will dramatically decrease since the data should be available at the output of $comp_1$ before the second comparator ($Comp_2$) can initiate its comparison. Using the ADC architecture in Figure 4.5, the first three comparators ($Comp_1$, $Comp_2$ and $Comp_3$) can perform their comparison simultaneously, and the delay to the selected output is only that of a 2:1 MUX, which is very small, and hence the system sampling speed will be increased.

Another key characteristic of the proposed ADC architecture in Figure 4.5 is that it can perform the conversion in one clock cycle, similar to the full flash ADC topology. The traditional full flash ADC and the proposed modified ADC both employ the dynamic latched-type comparator, described in chapter 3, which includes a SR latch to keep the comparator output during its recharge-mode. In the traditional full flash ADC topology, described in chapter 2, to maximise the sampling speed, the comparators perform their comparison simultaneously in the first half clock-cycle, and its logic encoder performs its function in the other half clock-cycle while the comparators maintains their output values (in recharge-mode). Thus, the digital data should be ready after one-clock cycle.

In the modified-flash ADC architecture of Figure 4.5, the first three comparators ($Comp_1$, $Comp_2$ and $Comp_3$) complete the comparison, the 2:1 MUX perform the selection and the appropriate reference voltages propagate through the 4:1 MUX to the bottom three comparators in the first half clock-cycle. In the other half clock-cycle, while all the data are maintained since the first three comparators keep their values in

recharge-mode, the bottom comparators ($Comp_4$, $Comp_5$ and $Comp_6$) perform the comparison and the last two bits ($D_1$ and $D_0$) will be encoded. Obviously, there will be a reduction of the sampling frequency of the modified flash ADC comparing with that of the full flash but the sampling frequency reduction is minor.

### 4.3.1.1 Noise Analysis

The existence of noise in CMOS integrated circuits is basically due to the fact that electrical charge is not continuous but is carried in discrete amounts to the electron charge, and thus noise is associated with fundamental processes in the integrated-circuit devices. When working at high frequencies, the noise generated within the device itself will play an increasingly important role in its overall performance [88]. Therefore, a model that can accurately predict the noise characteristics of the device is crucial for integrated circuit design.

As it was illustrated in Figure 4.5, the modified-flash ADC contains a resistor ladder, which consists of 16 resistors, two 2:1 switches, three 4:1 switches and six comparators. The noise model of each of these components is analysed mathematically and presented in this section.

#### 4.3.1.1.1 Resistor Ladder Noise Analysis

In a passive resistor, thermal noise is the most dominant source of noise, so here we only consider this type of noise. This noise source is a fundamental physical phenomenon and is present in any linear passive resistor. In a conventional resistor $R_L$,

as shown in Figure 4.6, the noise source can be represented by a series voltage generator as [88]:

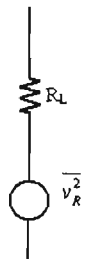



Figure 4.6: Noise source in resistor [88].

$$\overline{V^2{}_R} = 4kTR_L\Delta f \tag{4.14}$$

where $k$ is the Boltzman's constant, $T$ is the operation temperature, $R_L$ is the resistor value, $\Delta f$ is the small bandwidth at frequency $f$. This type of noise is due to the random thermal motion of the electrons and is unaffected by the presence or absence of direct current, since typical electron drift velocities in a conductor are much less than electron thermal velocities [88]. Using equation 4.14, one resistor in the flash ADC resistor chain ladder generates a noise power of $1.66\times10^{-17}\cdot\Delta f$ ($V^2$). Therefore the entire resistor chain will generate a total noise power of $2.656\times10^{-16}\cdot\Delta f$ ($V^2$).

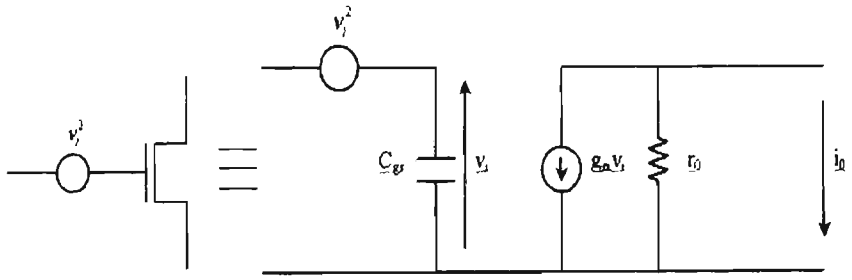
#### 4.3.1.1.2 2:1-MUX Noise Analysis

Before considering the entire 2:1 MUX, noise source in a MOS transistor must first be considered. The major noise sources in a MOS transistor are thermal noise and flicker noise.

$$\overline{V_i^2} = \frac{8kT}{3g_m}\Delta f + K\frac{I^a{}_D}{f}\Delta f \tag{4.15}$$

where $g_m$ is the MOS transconductance, $I_D$ is the drain current, $K$ is a constant for a particular device, $a$ is a constant in the range of 0.5 to 2 [89]. The first term in equation 4.15 represents the thermal noise of the MOS transistor, and the second term corresponds to the flicker noise of that transistor.

These noises could also be represented by using the equivalent input noise generator as shown in Figure 4.7 [90].



(a) (b)

Figure 4.7: MOSFET equivalent input noise generator (a) Symbol (b) Circuit detail [90]

The flicker noise component is approximately independent of bias current and voltage. For typical MOS transistor, flicker noise is inversely proportional to the active gate area of the transistor, and it is also inversely proportional to the gate-oxide capacitance per unit area [88]. The noise generator for MOS transistor, thus, can be expressed as follows:

$$\overline{V_i^2} = \frac{8kT}{3g_m}\Delta f + \frac{K_f}{WLC_{ox}f}\Delta f \tag{4.16}$$

where $W$ and $L$ are the width and length of a MOS transistor, respectively, $C_{ox}$ is the oxide capacitance, $g_m$ is the MOS transconductance, $k$ is the Boltzman's constant, $T$ is

the operation temperature, and $f$ is the operating frequency. Typical values for $K_f$ is $3\times10^{-24}$ $(V^2F)$ or $3\times10^{-12}$ $(V^2pf)$.

Figure 4.8 illustrates the 2:1 MUX with an equivalent noise generator of the overall circuit.

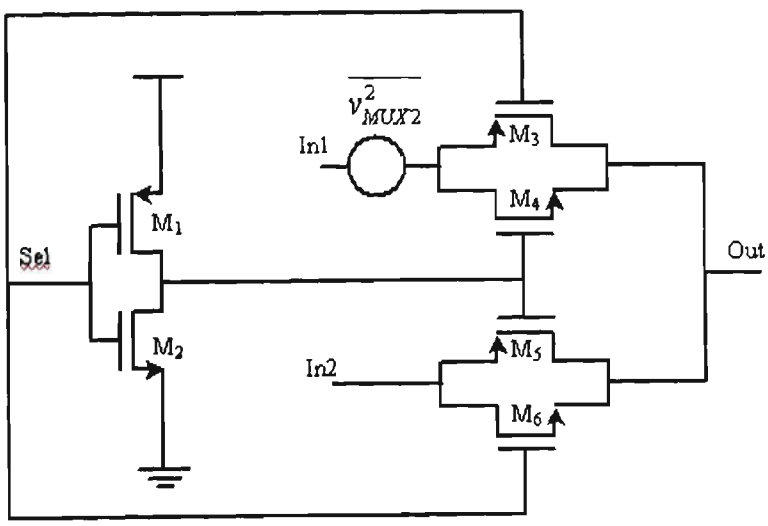



Figure 4.8: 2:1 switch (MUX) used in Modified ADC

The total output noise current for the 2:1 MUX is represented in equation 4.17.

$$\overline{i_{MUX2}^2} = g_{m5}^2\overline{V_5^2} + g_{m4}^2\overline{V_4^2} + g_{m3}^2\left(\overline{V_3^2} + r_{o1}^2 g_{m1}^2\overline{V_1^2} + g_{m2}^2\overline{V_2^2}r_{o2}^2\right)$$

$$+ g_{m6}^2\left(\overline{V_6^2} + r_{o1}^2 g_{m1}^2\overline{V_1^2} + g_{m2}^2\overline{V_2^2}r_{o2}^2\right) \qquad (4.17)$$

where $\overline{V_i^2}$ $(i = 1\ldots6)$ is the noise source generator of transistor $M_i$ which can be calculated by Equation 4.16. From equation 4.17 the input noise generator of the 2:1 MUX can be calculated:

$$\overline{V_{MUX2}^{\ 2}} = \overline{i_{MUX2}^{\ 2}}\left(r_{o3} // r_{o4}\right)^2 = \overline{i_{MUX2}^{\ 2}}\left(\frac{r_{o3} \cdot r_{o4}}{r_{o3} + r_{o4}}\right)^2 \tag{4.18}$$

Using Equation 4.18, one 2:1 MUX generates a total noise power of $4.41 \times 10^{-16} \cdot \Delta f$ ($V^2$) at an operating frequency of 400 MHz. Therefore the total noise power generated by the two 2:1 MUX is $8.82 \times 10^{-16} \cdot \Delta f$ ($V^2$).

#### 4.3.1.1.3 4:1-Switch Noise Analysis

Figure 4.9 illustrated the 4:1 MUX with the equivalent noise generator included.

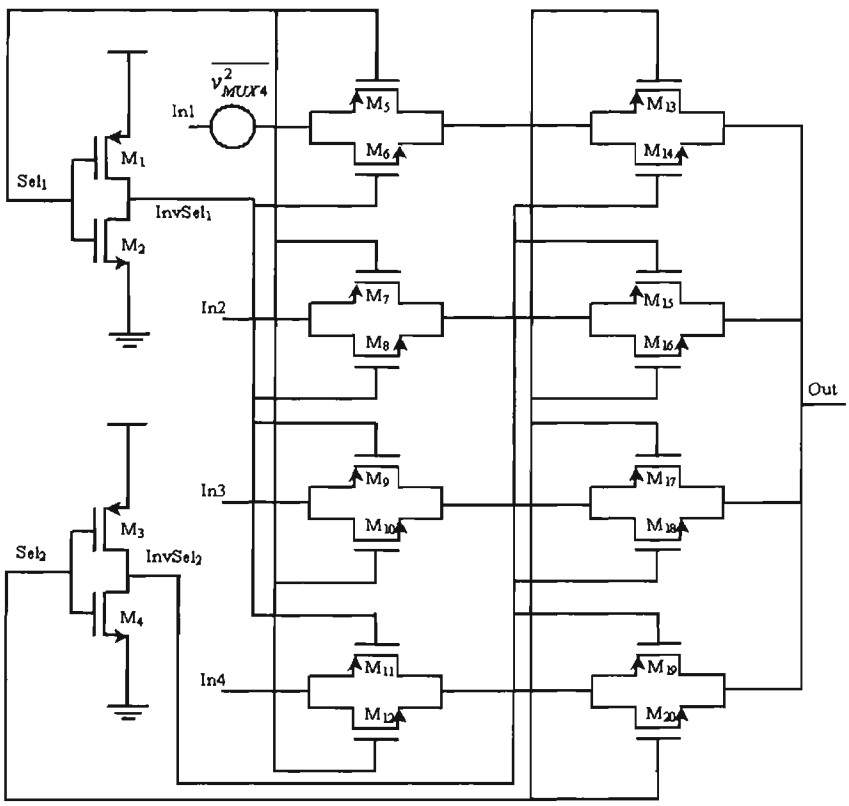



Figure 4.9: 4:1-MUX used in Modified ADC

Let,

$$\overline{V_{IN1}^{\ 2}} = r_{o1}^{\ 2} g_{m1}^{\ 2} V_1^{\ 2} + r_{o2}^{\ 2} g_{m2}^{\ 2} V_2^{\ 2} \tag{4.19}$$

$$\overline{V_{IN2}^{\,2}} = r_{o3}^{\,2} g_{m3}^{\,2} V_3^{\,2} + r_{o4}^{\,2} g_{m4}^{\,2} V_4^{\,2} \tag{4.20}$$

From the mathematical analysis on the 4:1 MUX, the total output noise current is:

$$\begin{aligned}\overline{i_{MUX4}^{\,2}} = {} & g_{m5}^{\,2}\overline{V_5^{\,2}} + g_{m6}^{\,2}\left(\overline{V_6^{\,2}} + \overline{V_{IN1}^{\,2}}\right) + g_{m7}^{\,2}\overline{V_7^{\,2}} + g_{m8}^{\,2}\left(\overline{V_8^{\,2}} + \overline{V_{IN1}^{\,2}}\right) \\ & + g_{m9}^{\,2}\left(\overline{V_9^{\,2}} + \overline{V_{IN1}^{\,2}}\right) + g_{m10}^{\,2}\overline{V_{10}^{\,2}} + g_{m11}^{\,2}\left(\overline{V_{11}^{\,2}} + \overline{V_{IN1}^{\,2}}\right) + g_{m12}^{\,2}\overline{V_{12}^{\,2}} \\ & + g_{m13}^{\,2}\overline{V_{13}^{\,2}} + g_{m14}^{\,2}\left(\overline{V_{14}^{\,2}} + \overline{V_{IN2}^{\,2}}\right) + g_{m15}^{\,2}\left(\overline{V_{15}^{\,2}} + \overline{V_{IN2}^{\,2}}\right) + g_{m16}^{\,2}\overline{V_{16}^{\,2}} \\ & + g_{m17}^{\,2}\overline{V_{17}^{\,2}} + g_{m18}^{\,2}\left(\overline{V_{18}^{\,2}} + \overline{V_{IN2}^{\,2}}\right) + g_{m19}^{\,2}\left(\overline{V_{IN2}^{\,2}} + \overline{V_{19}^{\,2}}\right) + g_{m20}^{\,2}\overline{V_{20}^{\,2}}\end{aligned} \tag{4.21}$$

where $\overline{V_i^{\,2}}$ ($i$ = 1...20) is the noise source generator of transistor $M_i$ which can be calculated by Equation 4.13. From Equation 4.21 the input noise generator of the 4:1 MUXUS can be calculated:

$$\begin{aligned}\overline{V_{MUX4}^{\,2}} &= \overline{i_{MUX4}^{\,2}} \cdot \left[\left(r_{o5} \,//\, r_{o6}\right) + \left(r_{o13} \,//\, r_{o14}\right)\right] \\ &= 2 \cdot \overline{i_{MUX4}^{\,2}} \cdot \left(\frac{r_{o5} \cdot r_{o6}}{r_{o5} + r_{o6}}\right)\end{aligned} \tag{4.22}$$

Using Equation 4.22, one 4:1 MUX generates a total noise power of $7.07\times10^{-16}\cdot\Delta f$ ($V^2$) at an operating frequency of 400 MHz. Therefore the total noise power generated by the three 4:1 MUXs is $2.121\times10^{-15}\cdot\Delta f$ ($V^2$).

#### 4.3.1.1.4 Comparator Noise Analysis

In the same manner, the CMOS voltage latched-comparator, described in chapter 3 and presented here in Figure 4.10, was analysed for noise.

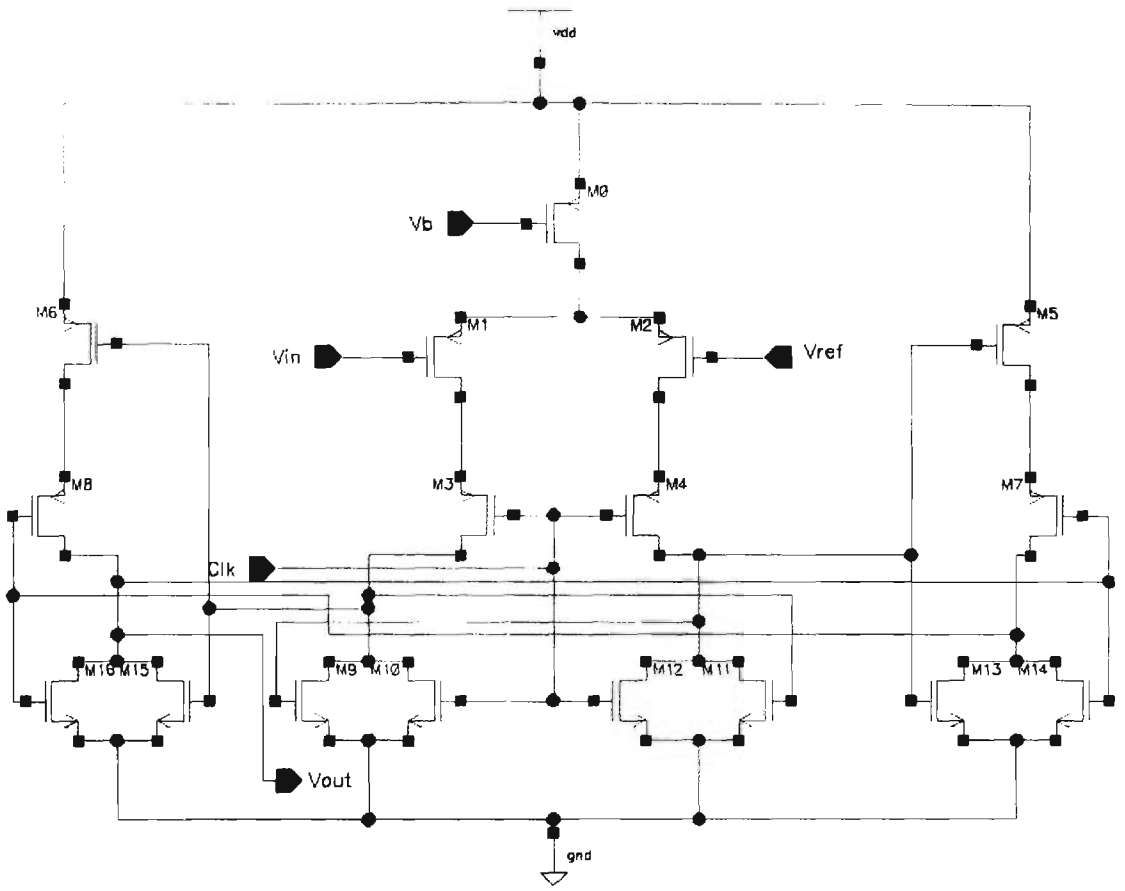



Figure 4.10: Dynamic comparator circuit

The input noise generator for one comparator can be described as:

$$\overline{v_{comp}^2} = \left(\frac{g_{m1}}{g_{m2}}\right)^2 \overline{v_1^2} + 2\overline{v_2^2} + 2\left(\frac{g_{m4}}{g_{m2}}\right)^2 \overline{v_4^2} + 2\left(\frac{g_{m6}}{g_{m2}}\right)^2 \overline{v_6^2} + 2\left(\frac{g_{m8}}{g_{m2}}\right)^2 \overline{v_8^2}$$

$$+ 4\left(\frac{g_{m10}}{g_{m10} + g_{m14}}\right)^2 \overline{v_{10}^2} + 4\left(\frac{g_{m14}}{g_{m10} + g_{m14}}\right)^2 \overline{v_{14}^2} \qquad (4.23)$$

Using equation 4.23 one comparator generates a total noise power of $5.3\times10^{-16}\cdot\Delta f$ ($V^2$) at an operating frequency of 400 MHz. Therefore the total noise power generated by six comparators working full time will be $3.18\times10^{-15}\cdot\Delta f$ ($V^2$). Detailed noise analysis and calculations on the latched-comparator used in this design could be found in Appendix B.

### 4.3.1.2 Probability Analysis

The new flash ADC contains six comparators. The probability of switching of each of these comparators is calculated mathematically in order to find out how much power each comparator consumes. To calculate the probability of each comparator a sine wave input is applied to the modified-flash ADC, as shown in Figure 4.11.

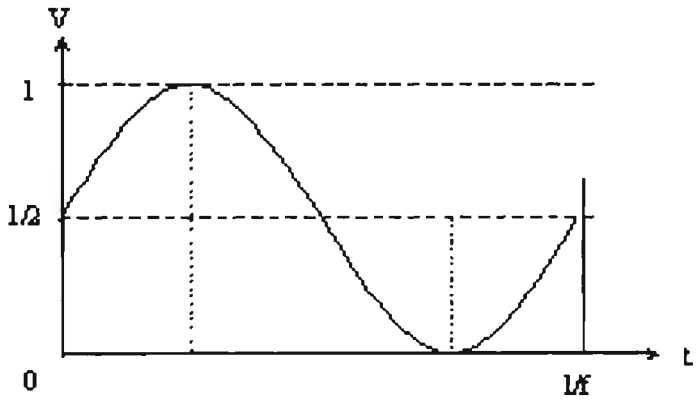



Figure 4.11: Sine wave input to ADC [91].

The sine wave input can be modelled as:

$$V_{in} = \frac{1}{2}\sin[2\pi ft] + \frac{1}{2} \tag{4.24}$$

where $f$ is the input signal frequency.

The probability of each comparator switching has been analysed. The probability that comparator 1 outputs a '1' can be described by the following model:

$$P(Comp_1 = '1') = \textit{The fraction of time in one period that } V_{in} \geq 0.25V = t(V_{in} \geq 0.25V)$$

In similar manner the probability of the rest of the comparators switching were calculated and are shown below.

$$P(Comp_2 = '1') = t\,[V_{in} \geq 0.5\ V] \tag{4.25}$$

$$P(Comp_3 = '1') = t\,[V_{in} \geq 0.75\ V] \tag{4.26}$$

$$P(Comp_4 = '1') = t\,[V_{in} \geq 0.8125\ V] + t\,[0.5625 \leq V_{in} < 0.75] + t\,[0.3125 \leq V_{in} < 0.5] + t\,[0.0625 \leq V_{in} < 0.25] \tag{4.27}$$

$$P(Comp_5 = '1') = t\,[V_{in} \geq 0.875\ V] + t\,[0.625 \leq V_{in} < 0.75] + t\,[0.375 \leq V_{in} < 0.5] + t\,[0.125 \leq V_{in} < 0.25] \tag{4.28}$$

$$P(Comp_6 = '1') = t\,[V_{in} \geq 0.9375\ V] + t\,[0.6875 \leq V_{in} < 0.75] + t\,[0.4375 \leq V_{in} < 0.5] + t\,[0.1875 \leq V_{in} < 0.25] \tag{4.29}$$

The probability of a certain comparator is off can be described as:

$$P(Comp_i = '0') = 1 - P(Comp_i = '1') \tag{4.30}$$

where $i$ is the comparator number ( $i = 1 \ldots 6$). Table 4.2 shows the probability switching of all six comparators. $P(Output = '1')$ describes the probability that a certain comparator output is on, and $P(Output = '0')$ describes that a comparator output is zero. The probability of a certain comparator being on or off will affect the noise that the new flash ADC will generate.

Table 4.2: Probability of each comparator

| **Comparator number** | ***P(Ouput = '1')*** | ***P(Output = '0')*** |
|---|---|---|
| $Comp_1$ | 0.75 | 0.25 |
| $Comp_2$ | 0.5 | 0.5 |
| $Comp_3$ | 0.25 | 0.75 |
| $Comp_4$ | 0.707 | 0.293 |
| $Comp_5$ | 0.5 | 0.5 |
| $Comp_6$ | 0.293 | 0.707 |

From the probability analysis of each comparator, it can be stated that the six comparators are equivalent to three of the comparators working full time. Therefore the total noise power generated can be said to be:

$$\text{Noise Power} = \frac{3.18\times 10^{-15}\cdot \Delta f}{2}\ (V^2), \text{ or } 1.59\times 10^{-15}\cdot \Delta f\ (V^2).$$

Table 4.3 presents a summary of the noise analysis for each component within the new flash ADC architecture. The total noise power is also calculated and presented in Table 4.3.

Table 4.3: Summary of noise power in New ADC.

| | **Noise in one component** | **Number of components in new flash ADC** | **Total Noise in specific components** |
|---|---|---|---|
| Resistor | $1.66\times 10^{-17}\cdot \Delta f$ | 16 | $2.65\times 10^{-16}\cdot \Delta f$ |
| 2:1 MUX | $4.41\times 10^{-16}\cdot \Delta f$ | 2 | $8.82\times 10^{-16}\cdot \Delta f$ |
| 4:1 MUX | $7.07\times 10^{-16}\cdot \Delta f$ | 3 | $2.12\times 10^{-15}\cdot \Delta f$ |
| Comp. | $5.30\times 10^{-16}\cdot \Delta f$ | 3 (operating full time) | $1.59\times 10^{-15}\cdot \Delta f$ |
| Total Noise of ADC | | | $4.86\times 10^{-15}\cdot \Delta f$ |

### 4.3.2 Analysis of the Modified-Flash ADC

The measured performance of all three ADCs are summarised in Table 4.4. According to the 3GPP specification on UTRA-TDD, a typical $\Delta f$ value is 5MHz. Therefore the total noise power of the system using this value will be $2.43\times10^{-8}$ ($V^2$).

Table 4.4: Comparison results of the ADC circuits at 400 MHz

| **Description** | **4-bit Full Flash** | **4-bit 2-step Flash** | **4-bit Mod.-Flash (This design)** |
|---|---|---|---|
| NMOS Devices | 179 | 109 | 84 |
| PMOS Devices | 194 | 117 | 90 |
| Resistors | 16 | 16 | 16 |
| Power Consumption | 18.26 mW | 10.38 mW | 7.46 mW |
| Noise Power ($\Delta f$ = 5 MHz) | | | $2.43\times10^{-8}$ $V^2$ |
| Resolution | 4 bits | 4 bits | 4 bits |
| Technology | 0.18 µm CMOS | 0.18 µm CMOS | 0.18 µm CMOS |
| Voltage Supply | 2.5 volts | 2.5 volts | 2.5 volts |

The full flash ADC, the two-step flash ADC, and the modified-flash ADC have been designed and simulated using 0.18µm.

Figure 4.12 presents the plots of differential non-linearity and integral non-linearity errors of the modified flash ADC at 400MHz sampling frequency. It can be seen that the DNL and INL achieved are 0.36 and 0.41 LSB respectively.

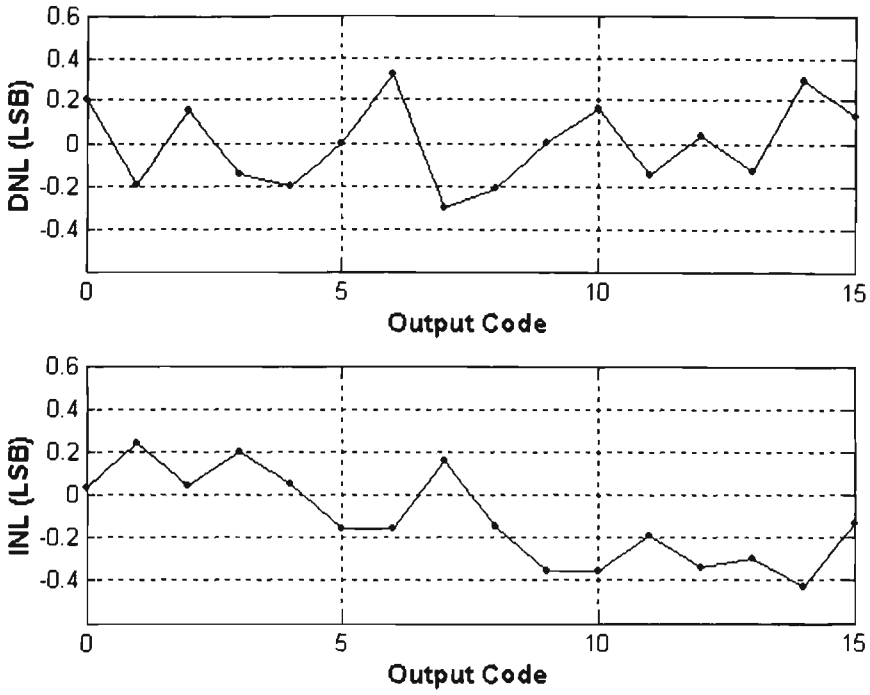



Figure 4.12: DNL and INL of the Modified-Flash ADC at 400 MHz

When the operating frequency of the analog-to-digital converter is increased, the power consumption increases dynamically. This increase is proportional to the frequency. Figure 4.13 illustrates the power analysis of the three ADCs.

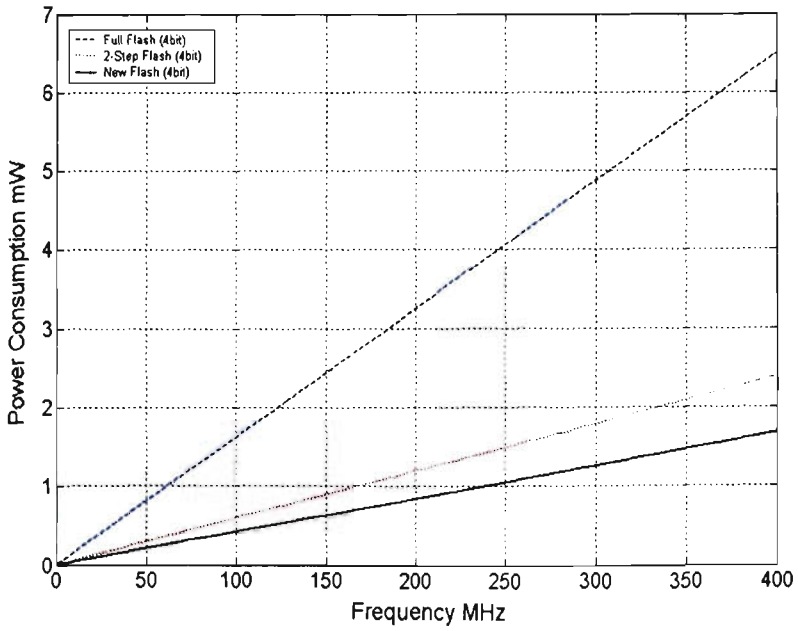



Figure 4.13: Power Analysis of the all three ADCs

As mentioned earlier, the comparator is the most critical and the most area-consuming component of the modified-flash ADC design. Table 4.5 shows the number of comparators required for all three flash ADC circuits.

Table 4.5: Number of Comparators required for each Flash design

| **Resolution (bits)** | **4-bit, Full Flash** $(2^N - 1)$ | **4-bit, 2-Step Flash** $2^{(N-1)}$ | **4-bit Flash (This design)** $2^{(N-2)} + 2$ |
|---|---|---|---|
| 4 | 15 | 8 | 6 |
| 6 | 63 | 32 | 18 |
| 8 | 255 | 128 | 66 |
| 10 | 1023 | 512 | 258 |
| 12 | 4095 | 2048 | 1026 |
| 14 | 16383 | 8192 | 4098 |
| 16 | 65535 | 32768 | 16386 |

The specifications of the UTRA-TDD system require a sampling rate of only 15.36 MSPS, therefore analysis on the modified-flash ADC has also been performed at this frequency. Table 4.6 compares the power consumption of all three designs at 15.36 MSPS.

Table 4.6: Comparison results of the ADC circuits at 15.36 MSPS

| | **4-bit, Full Flash** $(2^N - 1)$ | **4-bit, 2-Step Flash** $2^{(N-1)}$ | **4-bit Flash (This design)** $2^{(N-2)} + 2$ |
|---|---|---|---|
| Power Consumption | 6.50 mW | 2.39 mW | 1.68 mW |
| Supply Voltage | 2.5 V | 2.5 V | 2.5 V |
| Technology | 0.18 μm CMOS | 0.18 μm CMOS | 0.18 μm CMOS |

From the above analysis, it can be concluded that the advantages of the new ADC architecture include less components therefore smaller size, and lower power

consumption. These characteristics make this new device better candidate for many applications where power and size are the major factors.

## 4.4 Conclusion

The Sub-ADC is the most critical component of the pipeline ADC architecture. Making the right choice of which topology to employ is highly dependent on the design application. In this research, power consumption is the greatest concern due to the UTRA-TDD application. The standard flash design can operate at high frequencies, but it consumes large power due to the high device count. Therefore modification to the standard flash design has been done to compromise between power consumption and speed requirement.

The first block of the pipeline ADC, which is a 4-bit, CMOS modified ADC has been presented in this chapter. It requires only $(2^{(N-2)} + 2)$ comparators to implement the modified N-bit flash ADC. This approach greatly reduces the complexity of the full flash ADC and the two-step flash ADC. The new ADC architecture dissipates only 1.68 milliwatts of power at 15.36 MSPS as compared to a full flash ADC of 6.5 milliwatts and a two-step flash of 2.39 milliwatts. Results indicate that a 74% power saving is obtained and 53% of die size could be saved when the modified-flash ADC is used instead of the full flash architecture within the first pipeline ADC block. For comparison reasons all three analog-to-digital converters were operated at the UTRA-TDD system-sampling rate of 15.36 MSPS.

# Chapter 5

# *Reconfigurable ADC with Fixed Filter*

## 5.1 Introduction

In this chapter, a reconfigurable pipeline ADC architecture for TDD mode of the Universal Mobile Telephone Service, terrestrial radio access is presented. The advances in this chapter develop the findings of chapter 2, where the strength of quantisation noise ($Q_n$) is dependant on various dynamics and there is a minor probability of highly severe $Q_n$. Therefore, a fixed length for the receiver ADC would be inefficient resulting in unnecessary battery power drain. The basic concept of the reconfigurable ADC is to only utilise the required $Q_n$ to meet the specified bit energy to interference ratio (*Eb/No*), while restricting the filter adjacent channel protection (ACP) factor within the receiver at a fixed value of 33 dB, as per the 3GPP specifications.

This is obtained by employing a variable $Q_n$, which yields optimum efficiency. The $Q_n$ power, which meets the required *Eb/No* depends on the strength of ACI powers (out-of-band) received and the power of the in-band (desired signal and intra-cell interference) received power. This concept is demonstrated in a spectrum presented in Figure 5.1. As

illustrated in Figure 5.1 (a), when the adjacent channel interference (ACI) and the co-channel interference are both low, the noise floor of the ADC can be increased resulting in low resolution. On the other hand, as shown in Figure 5.1 (b), if the ACI and the co-channel interference are both high, the noise floor is decreased, providing high resolution. In the case where the SNR levels are always high, there is a distinct advantage of the proposed pipeline ADC. This means that the ACI will be low, resulting in low resolution and therefore saving vast amount of power. The in-band and out-of-band signal powers are monitored in real time.

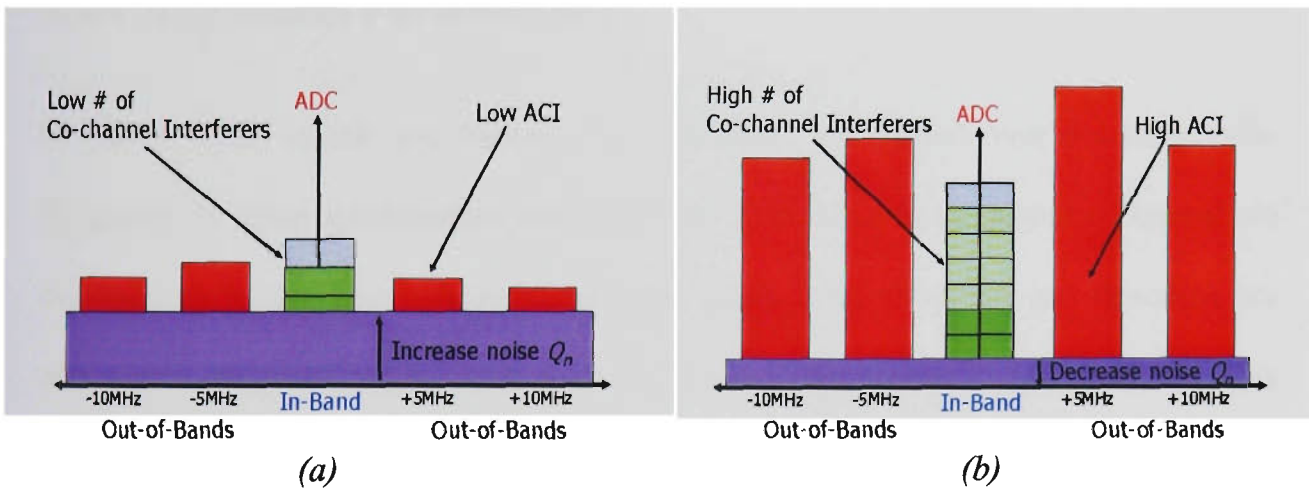



Figure 5.1: Spectrum analysis of operational concept of reconfigurable ADC

The chapter is structured as follows: section 5.2 presents and details the reconfigurable ADC design. All components within the reconfigurable architecture are described together with their operation. A statistical analysis of the reconfigurable ADC in a simulation environment is performed in section 5.3. The analysis demonstrates the efficiency of the design when applied to the UTRA-TDD system. The statistical analysis is of a static nature. Section 5.4 describes the implementation of the reconfigurable ADC, and illustrates the implemented design. Conclusions are presented in section 5.5.

## 5.2 Reconfigurable Pipeline ADC Design

The architecture of the reconfigurable pipeline ADC consists of a number of components to enable a scalable $Q_n$. Firstly, the algorithm enabling the ADC to exploit scalable $Q_n$ is formulated and the corresponding system architecture is introduced. The subsequent sections describe the operation of each of the components in the reconfigurable architecture.

### 5.2.1 Algorithm Formulation

In UTRA-TDD, uplink and downlink transmissions are carried over the same radio frequency by using synchronised time intervals. Time slots in the physical channel are divided into transmission and reception part. Information on uplink and downlink are transmitted reciprocally [89]. This makes TDD mode susceptible to ACI as nearby MSs and BSs cause interference to each other depending on frame synchronisation and channel asymmetry. This design presents results for downlink UTRA-TDD operation due to its near far problem. Figure 5.2 [93] presents a multi-operator downlink ACI scenario in UTRA-TDD.

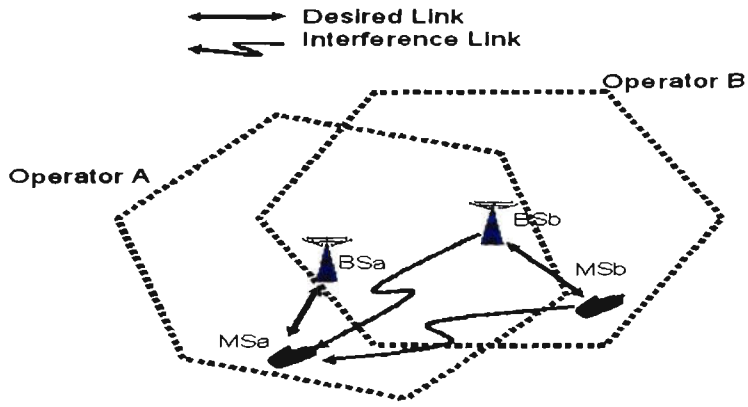



Figure 5.2: Downlink ACI scenario in UTRA-TDD [90].

Two interference sources exist in the downlink: adjacent MS and adjacent BS. The interference overlaps are BS→MS and MS→MS. If adjacent operators have synchronised frames and employ the same asymmetry, it would eliminate MS→MS interference. This cannot be assumed in practice and hence interference is experienced from both sources dependant on frame synchronisation and asymmetry. To obtain an understanding, consider Figure 5.3 [93]. User $MS_1$ employs a time offset ($t_{off}$) and both users $MS_1$ and $MS_2$ have time slots ($t_{slot}$) that represents the time allocated for uplink and downlink. Due to the offset in time, each user jams the other in uplink and downlink mode.

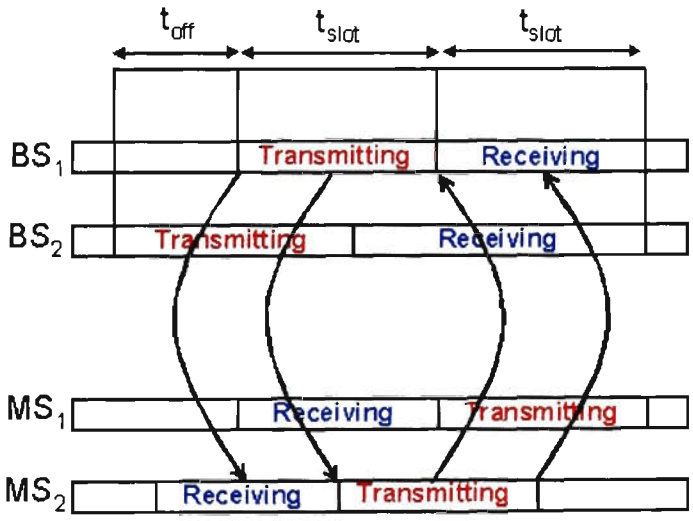



Figure 5.3: UTRA-TDD Interference Overlaps [93].

A synchronisation factor (α) needs to be employed in determining the amount of interference experienced at a source. This is modeled by the arbitrary time offset, $t_{off}$ and normalised by the time slot, $t_{slot}$ producing [93]:

$$\alpha = \frac{t_{off}}{t_{slot}} \tag{5.1}$$

Figure 5.4, illustrates the architecture of an UTRA-TDD MS receiver [57]. The block diagram demonstrates the general operation of the receiver showing the location of the proposed reconfigurable device in the topology. A control unit is proposed that makes a comparison between in-band (reference) and out-of-band (comparison) powers and scales the resolution of the ADC.

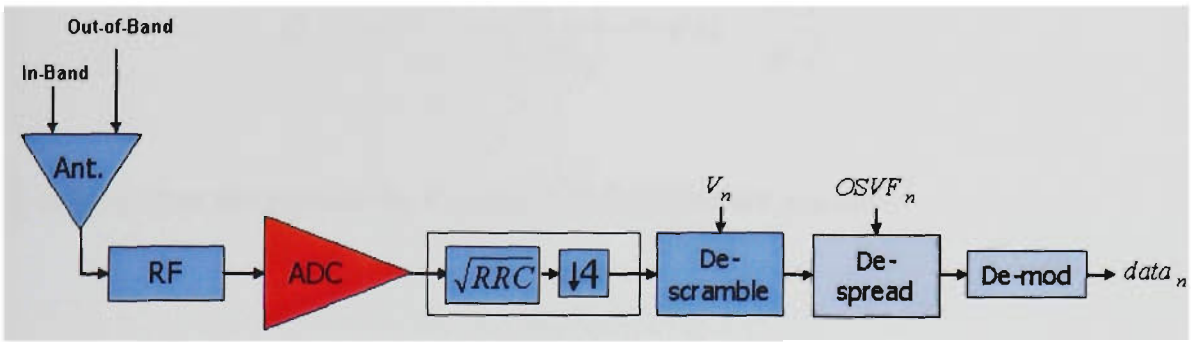



Figure 5.4: UTRA-TDD receiver architecture for one time slot [57].

The algorithm for the reconfigurable ADC is formulated from the *Eb/No* model given in Equation 5.2. Considering intra-cell interference is always present as orthogonality may not be achievable in practice and the received signal powers have been propagated.

$$Eb/No = \frac{\mathrm{P}rx^{i}\, pg}{\mathrm{P}rx^{i}(M-1)+\frac{ACI^{i}}{ACP}+\eta+Qn^{i}} \tag{5.2}$$

where $P_{rx}{}^{i}$ is the received desired signal power at the $i^{th}$ MS in the COI and is defined as follows:

$$P_{rx}{}^{i} = \frac{P_{rec}{}^{i}}{\kappa^{i}} \tag{5.3}$$

$P_{rx}^{\ i}$ is determined by the code power of the BS divided by the path loss of the $i^{th}$ MS within one time slot in the COI. The processing gain *pg* and thermal noise $\eta$ are known (static), as well as the target bit energy to interference ratio (*Eb/No)*. Solving Equation 5.2 for $Q_n^{\ i}$ yields:

$$Q_n^{\ i} = \Pr x^i \left(1 + \frac{pg}{Eb/No}\right) - \Pr x^i M - \frac{ACI^i}{ACP} - \eta \tag{5.4}$$

To differentiate the signals the following definitions are needed:

- *In-band* signal ($Prx^iM$) – This is purely the output of the filter containing the *desired* signal as well as intra-cell interference from other MS's served by the BS within the same timeslot.

- *Out-of-band* signal ($ACI^i$) – This signal is the interference that the receiver RRC filter has moderated. It can be obtained by using a high pass filter (HPF) corresponding to an inverse of the receiver filter. This method is inefficient, as the processing complexity will be doubled. In digital signal processing (DSP), a HPF equivalent filter can be a subtraction operation where the output of the LPF is subtracted from a delay unit. This is efficient to implement in hardware and is significantly less costly than a complex HPF.

- *Desired* signal ($Prx^i$) - This signal can only be obtained once the *in-band* signal is de-spread with the corresponding user orthogonal variable spreading factor (OSVF) code.

Based on the above definitions, the reconfigurable ADC will be established by a feed back structure as some receiver processing is required to obtain the necessary signals for a $Q_n$ calculation.

## 5.2.2 Receiver Architecture with Reconfigurable ADC

The reconfigurable ADC architecture for a receiver is proposed in Figure 5.5. The architecture consists of pipeline ADC architecture, RRC filter, de-spreader, de-scrambler, de-modulator, decimation factor and signal power measurement. The three inputs required by the control unit in order to reconfigure the ADC, are obtained from the filter and the de-spreader. Clearly varying amplitudes of each signal is required before they are reprocessed by the control unit where the most efficient $Q_n$ is calculated. This is achieved by the signal power measurement components in the architecture where the signals are averaged over a certain length of time.

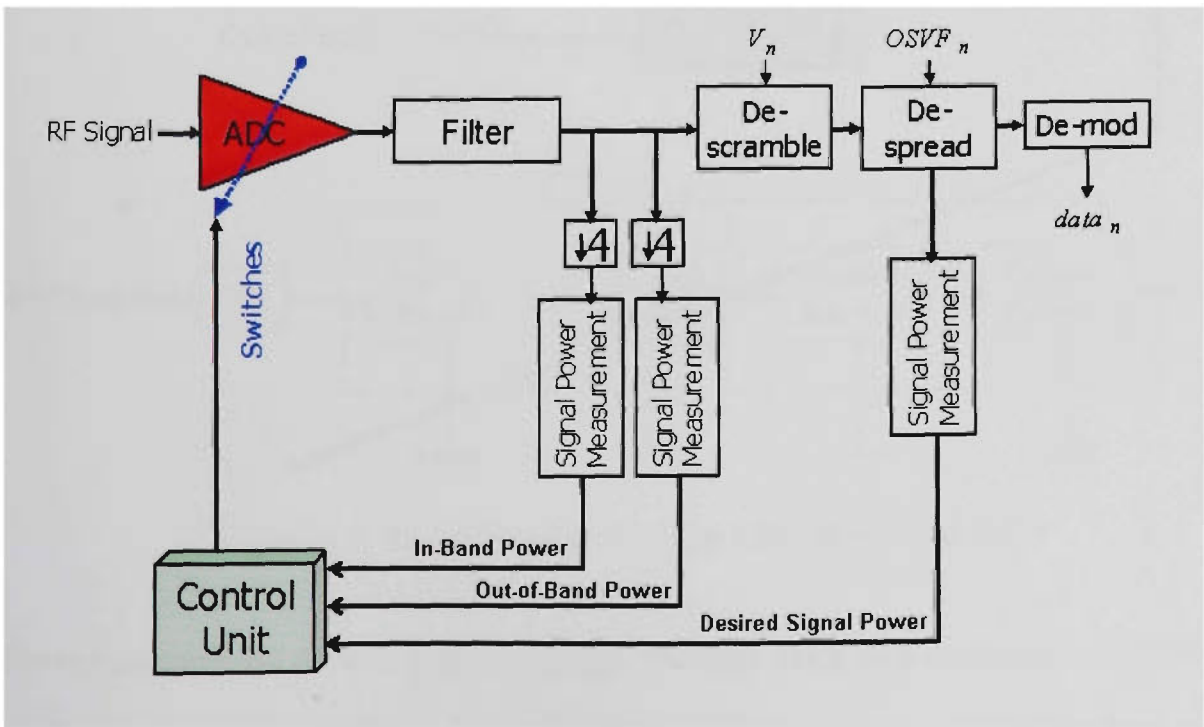



Figure 5.5: Reconfigurable receiver ADC architectural block diagram

### 5.2.2.1 Pipeline ADC Structure

The reconfigurable ADC circuit employs the pipeline topology. The architecture is controlled and scaled through the system control unit, as shown in Figure 5.5. The control unit is the brain of the reconfigurable architecture. This unit accepts the three input signals namely, *In-band* signal ($Prx^iM$), *Out-of-band* signal ($ACI^i$), *Desired* signal ($Prx^i$) and by using appropriate algorithms, it determines how many bits are required to ensure the *Eb/No* is met at all times. The control unit sends a signal to the ADC that control how many blocks need to be activated. The changes take place for the next frame input to the ADC. The feedback loop is performed constantly per frame to ensure the minimum number of bits is used. Figure 5.6 shows the topology of the reconfigurable pipeline ADC.

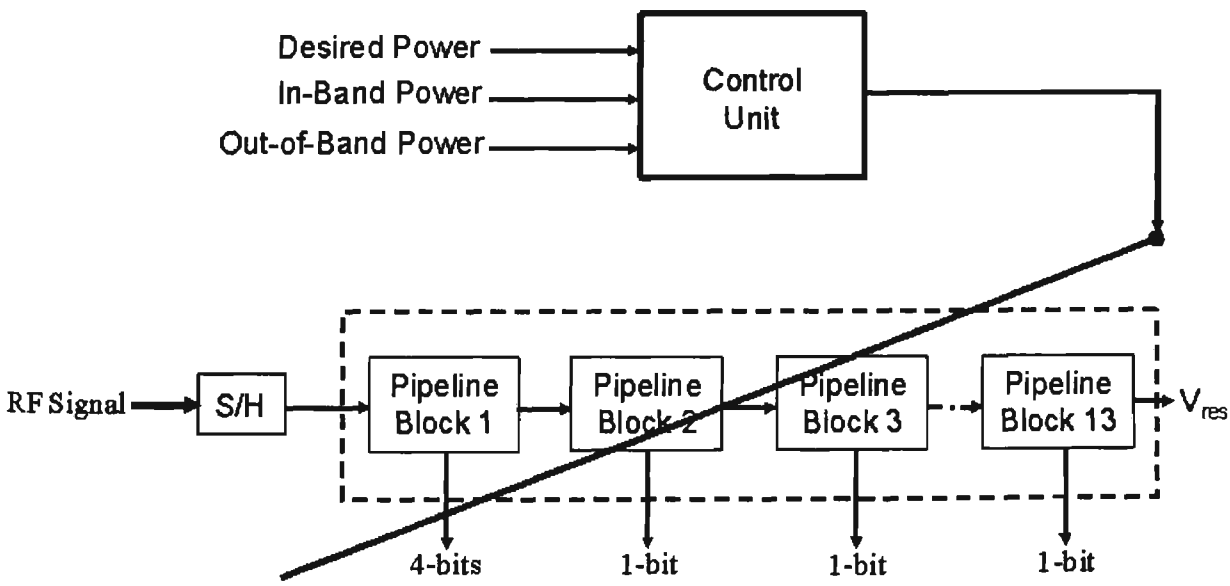



Figure 5.6: Reconfigurable Pipeline ADC block diagram

The system employs thirteen pipeline blocks. The first block outputs 4-bits, as described in chapter 4, and the remaining twelve blocks output 1-bit each. Within each of the 1-bit

blocks, a 1.5-bit pipeline topology is used, consisting of a sub-ADC, sub-DAC, and a gain amplifier.

### 5.2.2.2 Decimation Factor

The task of the decimation factor in the architecture is simply to down sample the received symbols by the same factor that is employed in the interpolation stage within the transmitter. Figure 5.7 illustrates an example of operation of the decimation algorithm. The decimation factor for 3GPP specification is 4 for the receiver ADC, therefore down sampling the data rate to 3.84 MHz. The decimation procedure is an essential process in multirate signal processing. It competently allows the sampling frequency of the system to decrease without unnecessary effects on the signal such as the quantisation noise.

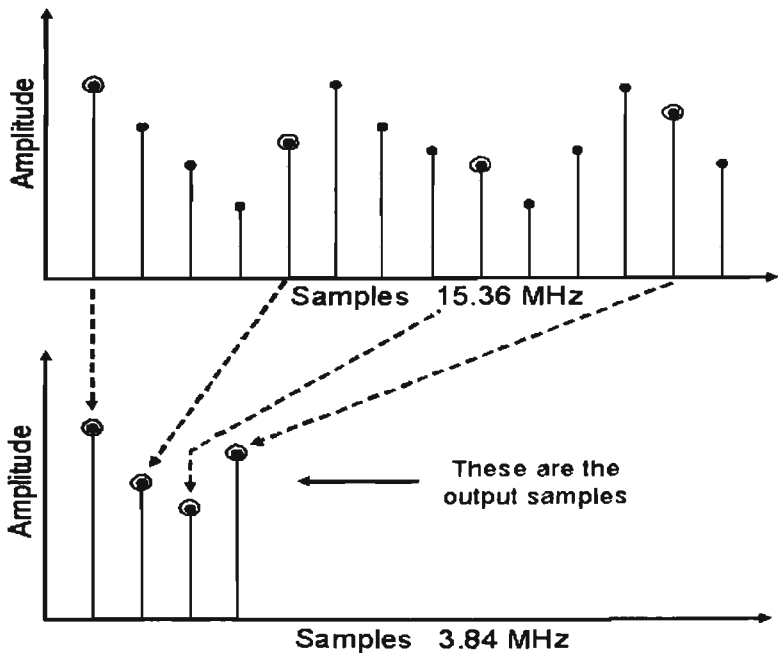



Figure 5.7: Decimation operation, down sampling by factor of 4.

In the TDD receiver mode, the decimation phase only allows every fourth sample of its input to go through to the output, therefore omitting every three samples of its input.

### 5.2.2.3 Signal Power Measurement

The signal power measurement consists of two components, which are the full wave rectifier (FWR) and the averaging filter (AF). Figure 5.8 illustrates the operation of the signal power measurement component.

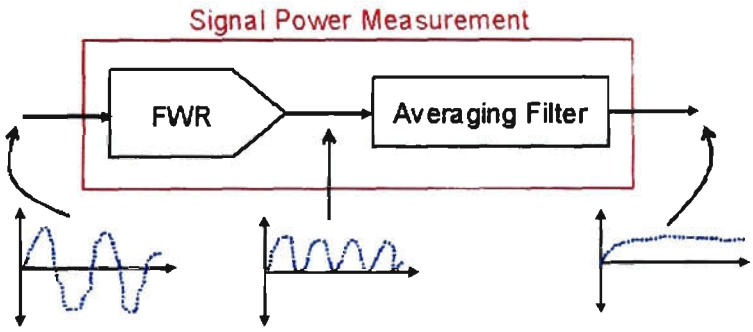



Figure 5.8: Signal Power Measurement

#### 5.2.2.3.1 Full Wave Rectifier

The first component is the FWR. The absolute amplitude of each signal must be taken before an average is found with the subsequent averaging filter. In digital signal processing it is a low complex operation. The inverse of each sample is found dependent if the sample is negative in magnitude. In hardware, the FWR is a two's compliment operation. Figure 5.9 depicts an example demonstrating the operational steps for a negative input with a word length of five bits. The first bit is the sign bit and the subsequent four bits are the magnitude. Figure 5.10 illustrates the operation of the FWR in a flowchart format.

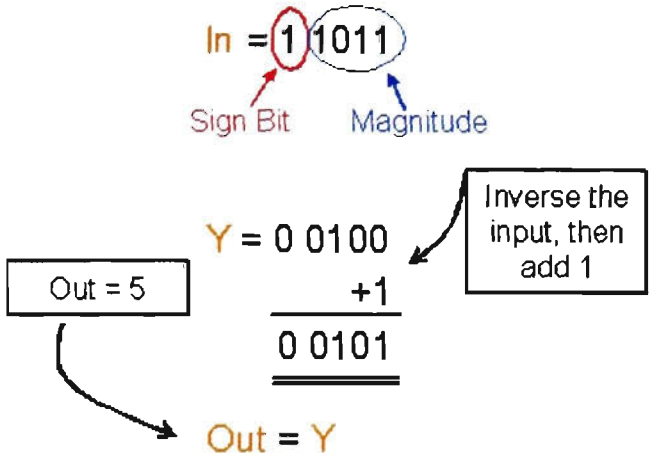



Figure 5.9: Two's compliment operation in digital hardware with a word

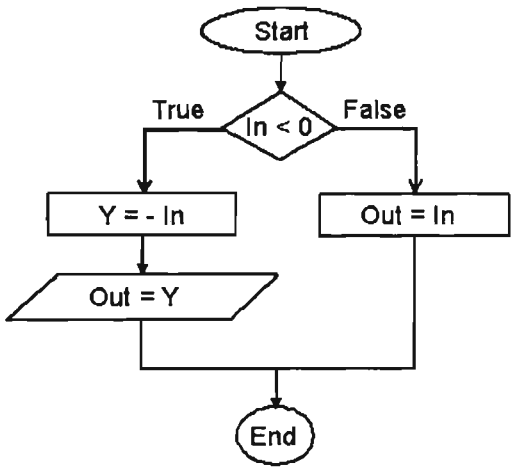



Figure 5.10: Operation of the FWR

### 5.2.2.3.2 Averaging Filter

The averaging filter is a first order IIR digital low pass filter (LPF). It computes an average on a vector of sampled data using a delayed input sample and the previous output sample for each input sample. The requirement for implementation will not be costly as only two multipliers and two addition units are required. A delay unit is represented by $Z^{-1}$, as shown in Figure 5.11, and the difference equation $y(n)$ is defined as follows [94, 95]:

$$y(n) = \left[\left(x(n) + x(n-1)\right) \bullet \upsilon\right] + \left[y(n-1) \bullet \delta\right] \tag{5.5}$$

where *x(n)* is the current input sample, *x(n-1)* is a delayed input sample, *y(n-1)* is a delayed output sample and $\upsilon$ is defined as [94]:

$$\upsilon = \frac{(1-\delta)}{2} \tag{5.6}$$

where δ is described as follows [94]:

$$\delta = \frac{\cos \theta c}{1 + \sin \theta c} \tag{5.7}$$

where $\theta c$ is a normalised frequency of $0.002\pi$ [94]. The impulse response is infinite in duration, and the IIR filter can be modeled by the resistor capacitor (RC) circuit, as shown in Figure 5.11.

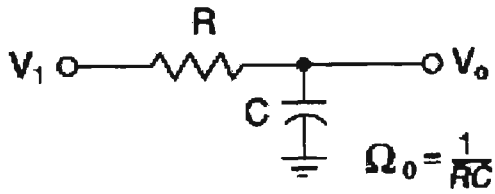



Figure 5.11: RC Low Pass Filter Network [94].

The basic components of the digital filter network, as shown in Figure 5.12, are the multiplier (α), adder (Σ), and delay element ($Z^{-1}$).

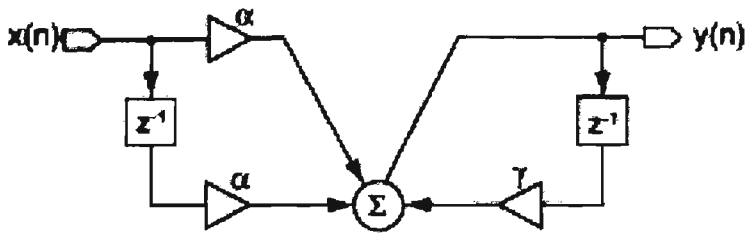



Figure 5.12: Digital Low-Pass Filter Network [94].

The final output sample of the filtered data is the average amplitude of the entire stream of input samples, which is fed to the control unit.

### 5.2.2.4 Control Unit

The control unit is the intelligence in the reconfigurable architecture. It calculates the required quantisation noise based on the three signals powers, as presented in section 5.2.1, and by using an intelligent algorithm calculates the appropriate dynamic range of the ADC. A look-up-table (LUT) is used to intelligently switch the pipeline blocks of the ADC '*off*', if not required, saving significant power.

The $Q_n$ is not the only aspect to determine the new length of the ADC. If it was, there would be a likelihood of some data loss. As the architecture employs a feedback loop, and two of the inputs to the control unit come from the filter, the filter length is applied to the next lot of samples, not the current, therefore any loss of information must be dealt by the filter.

The architecture reconfigures the ADC to the new length and applies it to the next lot of samples. As it is a TDD system where a near far problem exists, an adjacent MS may switch-on close to the MS of interest at the same time it is receiving the next lot of

samples. If this adjacent MS is transmitting to its base station, it will result in a major jamming of the signal. Therefore, the minimum 4-bits of resolution may not be sufficient to meet the system *Eb/No*. The operation and reconfigurability aspect of the ADC here is based on a fixed ACP value of 33 dB, obtained from the 3GPP specifications. In order to obtain the word length of the ADC, the calculated $Q_n^i$ is substituted in the following equation:

$$n^i = \frac{10 \bullet \log 10\left(\frac{(ACI^i + \Pr x^i) \bullet Decimation_F}{Q_n^i}\right)}{6.02} + Safety_M \qquad (5.8)$$

where $n^i$ is the word length of the ADC at a given location in the COI that satisfies the *Eb/No*, $ACI^i$ is the adjacent channel interference of the system fixed at 33 dB according to the specifications of the 3GPP, $Safety_M$ is the safety margin of additional 2 dB to take care of large peaks. Once the $Q_n$ of the ADC is calculated from Equation 5.4, the corresponding resolution can be derived by calculating the dynamic range. The dynamic range (DR) of the ADC is a measure of the noise floor in comparison to the largest input voltage, but in this case, it is in comparison to the largest input wattage yielding:

$$DR = 10 \cdot \log_{10}\left(\frac{Max_W}{Noise_W}\right) \quad [dB] \qquad (5.9)$$

where $Noise_W$ is the noise floor assigned to the quantisation noise derived in Equation 5.4, and $Max_W$ is the maximum input wattage defined as a sum of the desired and out-of-band signal powers and is given by:

$$Max_W = \left(P_{rx}^{\ i} + I_{adj}^{\ i}\right) \cdot Decimation_F \tag{5.10}$$

The summation of the desired and out-of-band signal powers are scaled by the decimation factor, $Decimation_F$. The corresponding ADC resolution is:

$$n_{ADC} = \frac{DR}{6.02} \tag{5.11}$$

A LUT can be used to convert the calculated dynamic range from Equation 5.9 to the corresponding switches to control the pipeline ADC resolution. Equation 5.11 can be used but will be inefficient as extra computational processing is needed. It will not only give integer value for the required ADC resolution but floating point values as well. Hence, LUT is still required to round the calculated resolution to an integer. The LUT to convert dynamic range to corresponding ADC switches is presented in Table 5.1.

Table 5.1: Control Unit Look Up Table

| **Dynamic Range (dB)** | **ADC Resolution** | ***Bits_Switch*** **(Logic "0" or "1") Corresponding to 13 Pipeline Blocks** |
|---|---|---|
| DR ≤ 24.0804 | 4 | 1000000000000 |
| 24.0804 ≤ DR ≤ 30.1005 | 5 | 1100000000000 |
| 30.1005 ≤ DR ≤ 36.1206 | 6 | 1110000000000 |
| 36.1206 ≤ DR ≤ 42.1407 | 7 | 1111000000000 |
| 42.1407 ≤ DR ≤ 48.1608 | 8 | 1111100000000 |
| 48.1608 ≤ DR ≤ 54.1809 | 9 | 1111110000000 |
| 54.1809 ≤ DR ≤ 60.2010 | 10 | 1111111000000 |
| 60.2010 ≤ DR ≤ 66.2211 | 11 | 1111111100000 |
| 66.2211 ≤ DR ≤ 72.2412 | 12 | 1111111110000 |
| 72.2412 ≤ DR ≤ 78.2613 | 13 | 1111111111000 |
| 78.2613 ≤ DR ≤ 84.2814 | 14 | 1111111111100 |
| 84.2814 ≤ DR ≤ 90.3015 | 15 | 1111111111110 |
| 90.3015 ≤ DR ≤ 96.3216 | 16 | 1111111111111 |

The dynamic range is given in dB units but in implementation can be left in units of watts for simplification, therefore disregarding the log functionality.

## 5.3 Statistical Analysis

A statistical analysis in the UTRA-TDD mode was performed to demonstrate the efficiency of the reconfigurable ADC. Section 5.3.1 presents the simulation environment, which consists of the simulation platform, and the simulation parameters used in the system. In section 5.3.2 all results from the statistical analysis are presented, which in fact justifies the design of the reconfigurable ADC.

### 5.3.1 Simulation Environment

The cell topology presented in Figure 5.13 is used as a simulation platform. The distance between the COI (shaded cell) BS and the immediate adjacent channel BS along the *a* axis is 50 meters. Parameters used in this work are presented in Table 5.2.

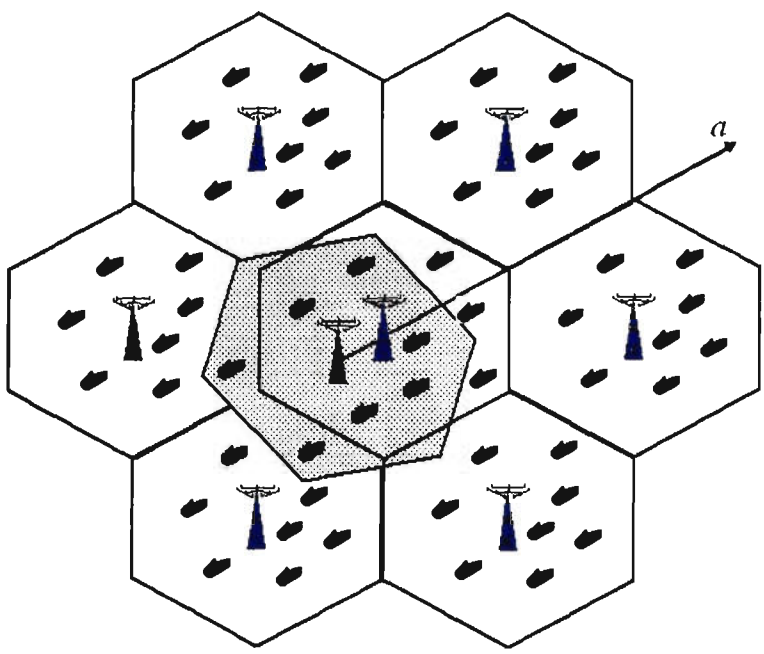



Figure 5.13: Cell topology where multiple cells are causing ACI.

Table 5.2: Simulation Parameters

| **Parameter** | **Value** |
|---|---|
| Bit Rate | 32 Kbits/s |
| Max TX Power (dBm) | Downlink: 10, Uplink: 4 |
| Thermal Noise (dBm) | -102.85 |
| Required Eb/No (dB) | 3.5 |
| Receiver Sensitivity, without Imargin (dBm) | -112.89 |
| Lognormal Shadowing variable $\sigma$ (dB) | 12 |
| Cell Radius (m) | 100 |
| # of Interfering Adjacent Cells | 7 |
| # of users in each Interfering Adjacent Cell | 8 |
| Synchronisation factor $\alpha$ | Uniform random 0 to 1 |
| Path loss exponent $\gamma$ | 3.0 |
| Full Scale input Voltage $V_{fs}$ | 2 |

The layer of interfering hexagon cells was approximated with seven cells as it was found that beyond these cells the caused interference was insignificant [96].

The BSs were located in the centre of the cells. The required *Eb/No* might seem low, but this is due to the assumption of powerful coding mechanism, such as turbo coding. The inherent assumption was that UTRA-TDD is primarily used for data-oriented services.

## 5.3.2 Statistical Results

Users in the COI and adjacent channel cells were placed randomly using a uniform distribution. Monte Carlo simulations were carried out to obtain the cumulative distribution function (CDF) of the interference powers $I_B$ and $I_M$, at each random point. In addition, the $Q_n$ levels at each of these points were found.

The results obtained are for a near full load of eight users in each of the seven adjacent channel interfering cells and a near full load in the COI. A lognormal shadowing variable of 12dB was used in the simulation obtained from the 3GPP specifications.

Figure 5.14 illustrates the CDF of the ADC word length values. Four different synchronisation factor (α) values were generated on each Monte Carlo run. Lognormal shadowing of 12dB was used. It is clear that there is a low percentage of higher $Q_n$ and lower $Q_n$.

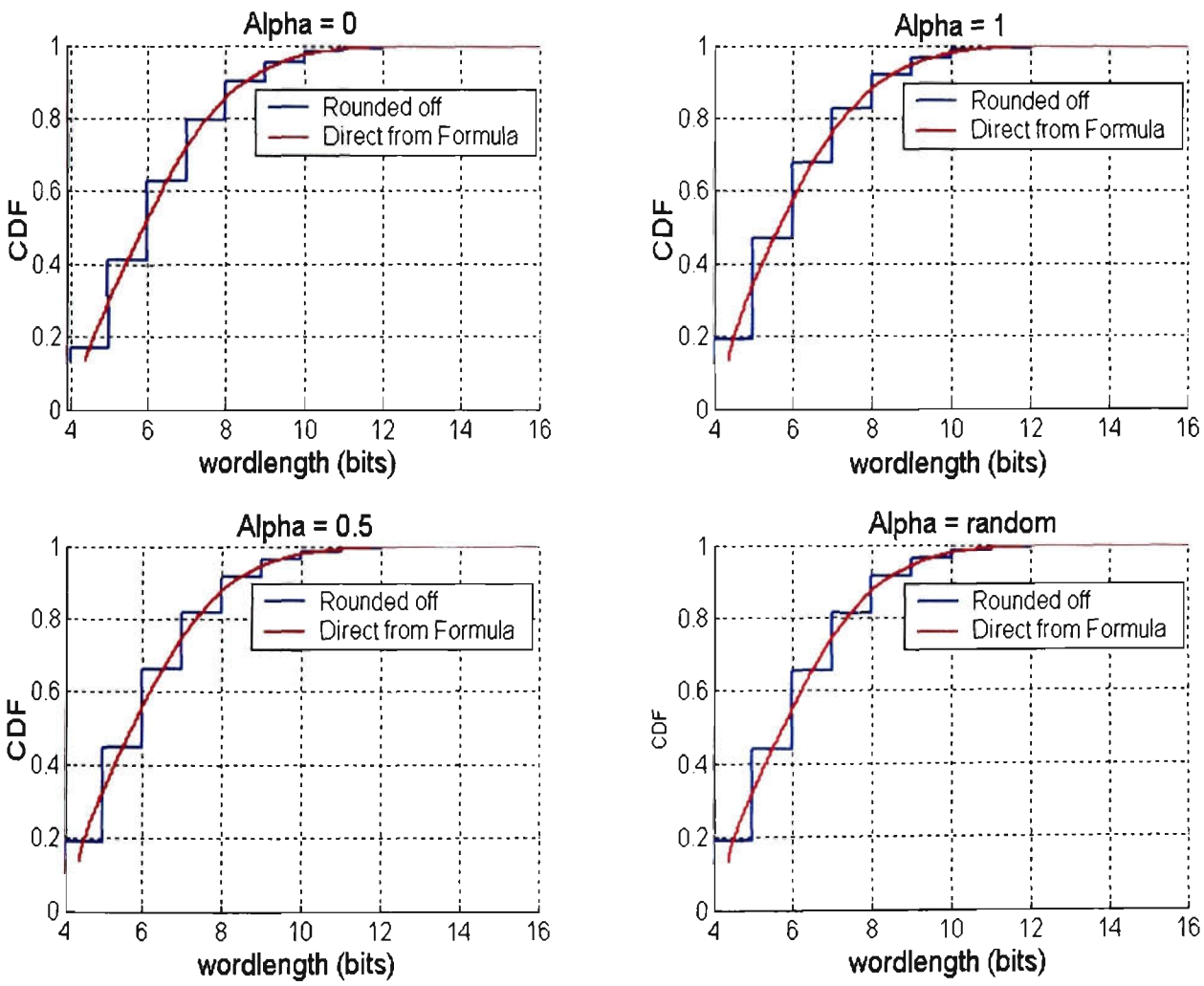



Figure 5.14: CDF of ADC word lengths

Table 5.3 provides a comparison of the different median and standard deviation values for all four different synchronisation factors by using the plots of Figure 5.13.

Table 5.3: Effect on Resolution with different α.

| Alpha | Median Value (bits) | Standard Deviation |
|---|---|---|
| α = 0 | 5.897 | 2 |
| α = 1 | 5.649 | 2 |
| α = 0.5 | 5.728 | 2 |
| α = random | 5.764 | 2 |

From Table 5.3 it can be summarised that even though the difference between the median values of the resolutions at different alpha values is significantly small, there is still some percentage of difference. In the implementation process the alpha values will not affect the resolution due to the rounding off condition. All resolution with decimal points will have to be rounded off to the higher resolution.

It can be observed in Table 5.3 that when the synchronisation factor α = 0, which means that there is MS → MS interference only, there is a high probability of the required resolution being between 3.897-bits and 7.897-bits. When α = 1, meaning that there is only BS → MS interference, the probability of required resolution is slightly different to that when α = 0, and is between 3.649-bits and 7.649-bits. When α = 0.5, meaning that 50 % of the interference is from BS → MS and 50 % is from MS → BS, the probability of required resolution is between 3.728-bits and 7.728-bits. The final value for α = random, is when any possibility of interference can occur, and the probability of required resolution is between 3.764-bits and 7.764-bits.

All boundary values above are calculated using the standard deviation of 2. It can be seen that alpha has small affect on the resolution, therefore it can be stated that the highest probability of required resolution within the reconfigurable system is between 4 bits and 8 bits, and that resolution lower than 4-bits and higher than 10-bits will occur very rarely. Figure 5.15 illustrates CDF plots of the power consumption for the different synchronisation factors.

Once again a slight difference of power consumption for different alpha vales can be noticed. There has been a greater analysis performed on the plot of Figure 5.15 (d), due to the fact that here $\alpha$ is random, which what it would be in a real life scenario.

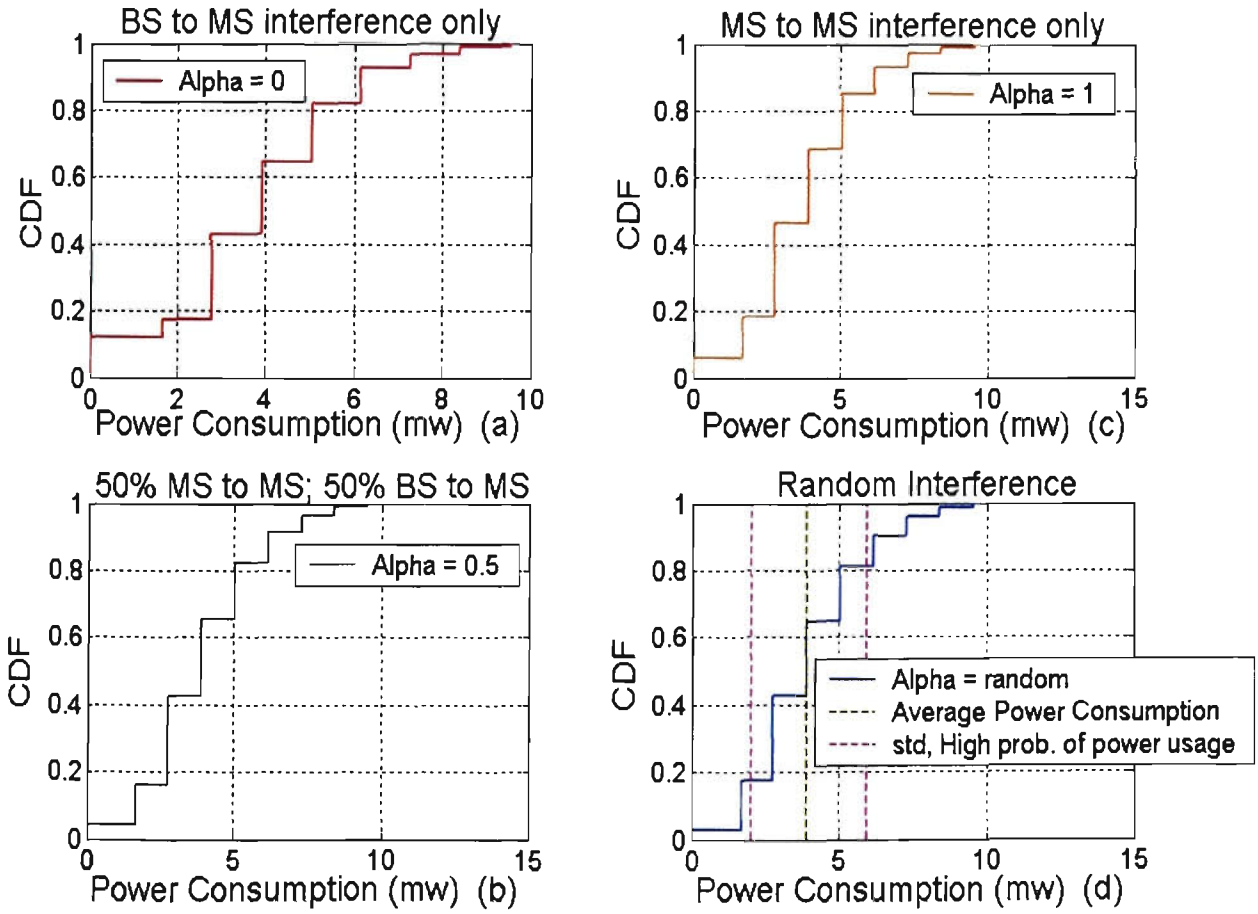



Figure 5.15: CDF of ADC Power Consumption

The last CDF plot of Figure 5.15 (d), shows the power consumption for the entire 16-bits ADC. The middle dotted line indicates the mean power consumption of the converter, which is 3.92mW, and is present when the average 6-bits resolution of the reconfigurable ADC is used. The other two dotted lines surrounding the mean power consumption dotted line, are the standard deviation boundaries, which indicate the highest probability of power usage of the reconfigurable architecture, which occur between 1.68mW and 6.16mW. These boundaries correspond to 4-bits and 8-bits. The results of Figure 5.15 also justify the analysed results illustrated in Figure 5.14.

## 5.4 Implementation of the Reconfigurable ADC

Prior to illustrating the final layout implementation of the reconfigurable ADC, the design process, design techniques, and layout considerations are first presented in this section.

### 5.4.1 Design Flow and Techniques

This section describes the appropriate CMOS design flow and the circuit design techniques used for the design and layout of the components within the ADC.

#### 5.4.1.1 CMOS IC Design Flow

The CMOS design flow consists of defining circuit inputs and outputs, hand calculations, schematic entry of design, circuit simulations, layout of the circuit, simulations including parasitics, re-evaluation of the circuit inputs and outputs, and finally fabrication and testing. Figure 5.16 [94] illustrates the CMOS IC design flow.

This is the general design flow used to design an integrated circuit. More detailed insight of the design flow used for the design, simulation and layout implementation of the pipeline ADC is illustrated in Figure 5.17. The figure illustrates the EDA tools used to design, simulate, and implement the pipeline ADC, which are supplied by *Cadence*.

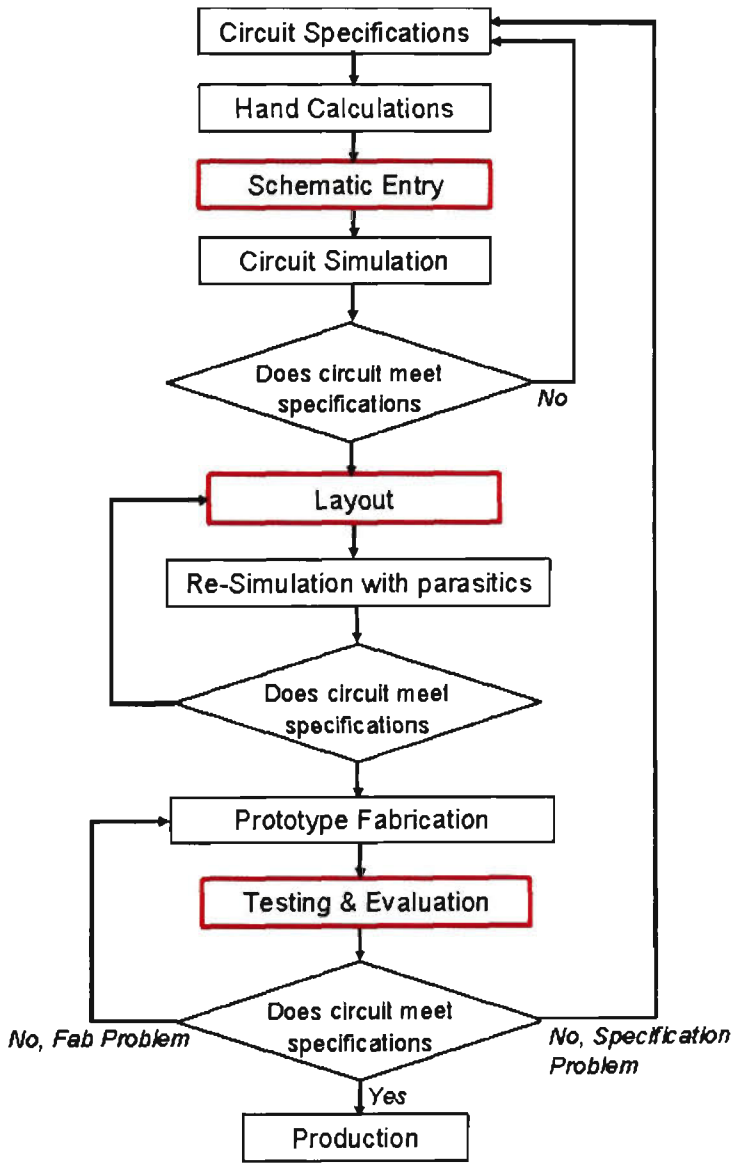



Figure 5.16: CMOS IC design process [97].

At first, the circuits were designed at transistor level using the *Virtuoso Schematic Editor* (Analog Artist), for every component of the ADC, where the designs were checked and symbol cells for future use were created. The *Spectre* simulator was used

for simulation of the ADC design and the appropriate Netlist files were loaded into *Virtuoso XL*, where approximately 80% of the layout was generated. The layout of the reconfigurable ADC was fully completed by the use of Layout Editor. Virtuoso place and route tools were used to place and route the design. *DIVA* layout versus schematic checks were carried out and the GDSII files were generated for fabrication.

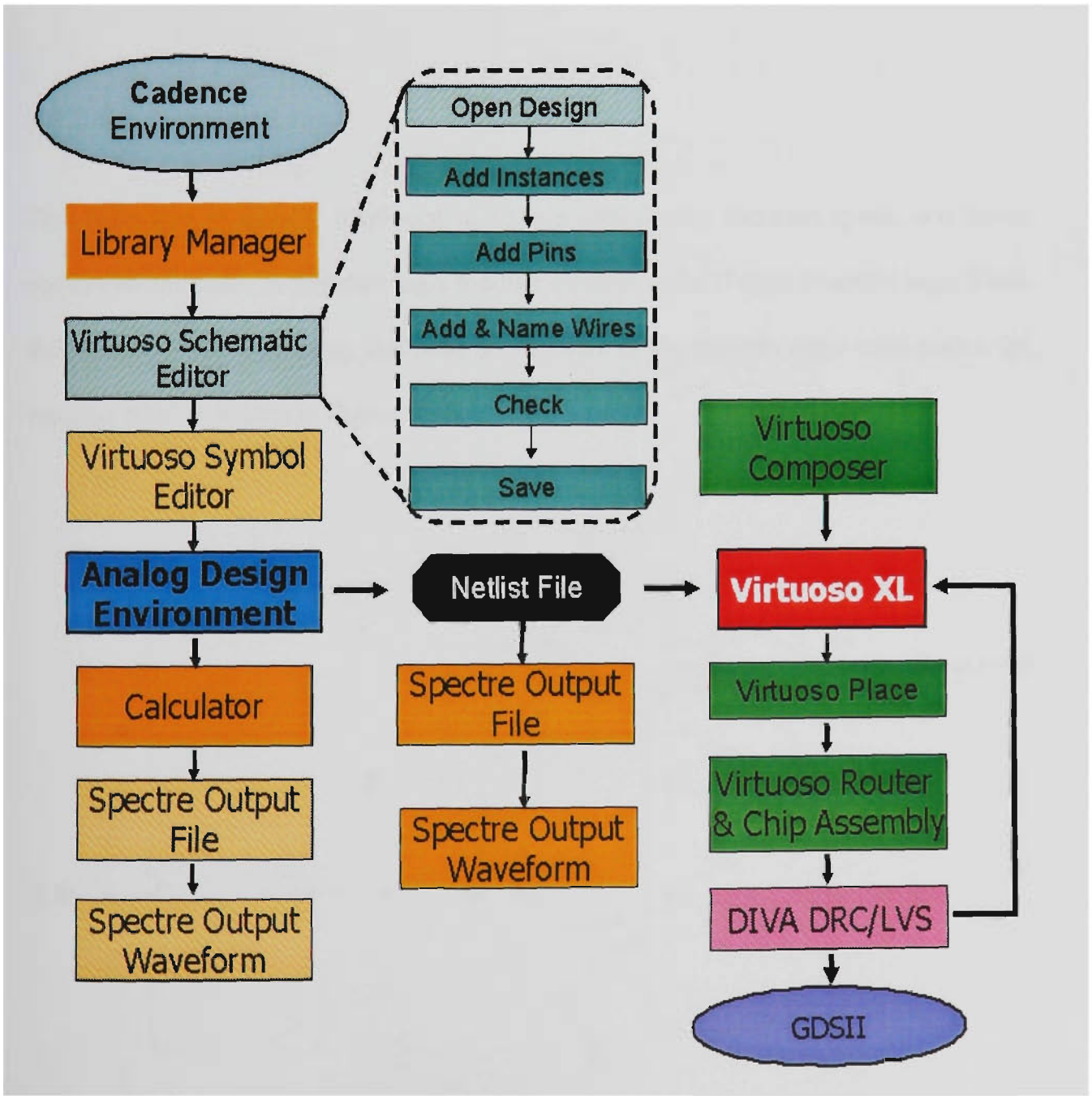



Figure 5.17: Design flow employed for reconfigurable ADC

### 5.4.1.2 ADC Digital Section

Since the ADC has been designed and implemented at transistor level to achieve maximum performance and optimisation, it is important to investigate and analyse the best design technique for the digital section. The design technique employed is the domino logic [98].

#### 5.4.1.2.1 Domino Logic

This technique is usually employed to reduce complexity, increase speed, and lower power consumption. A Domino logic module consists of an N-type dynamic logic block followed by a static inverter. The domino structure of the encoder logic used within the pipeline ADC is shown in Figure 5.18.

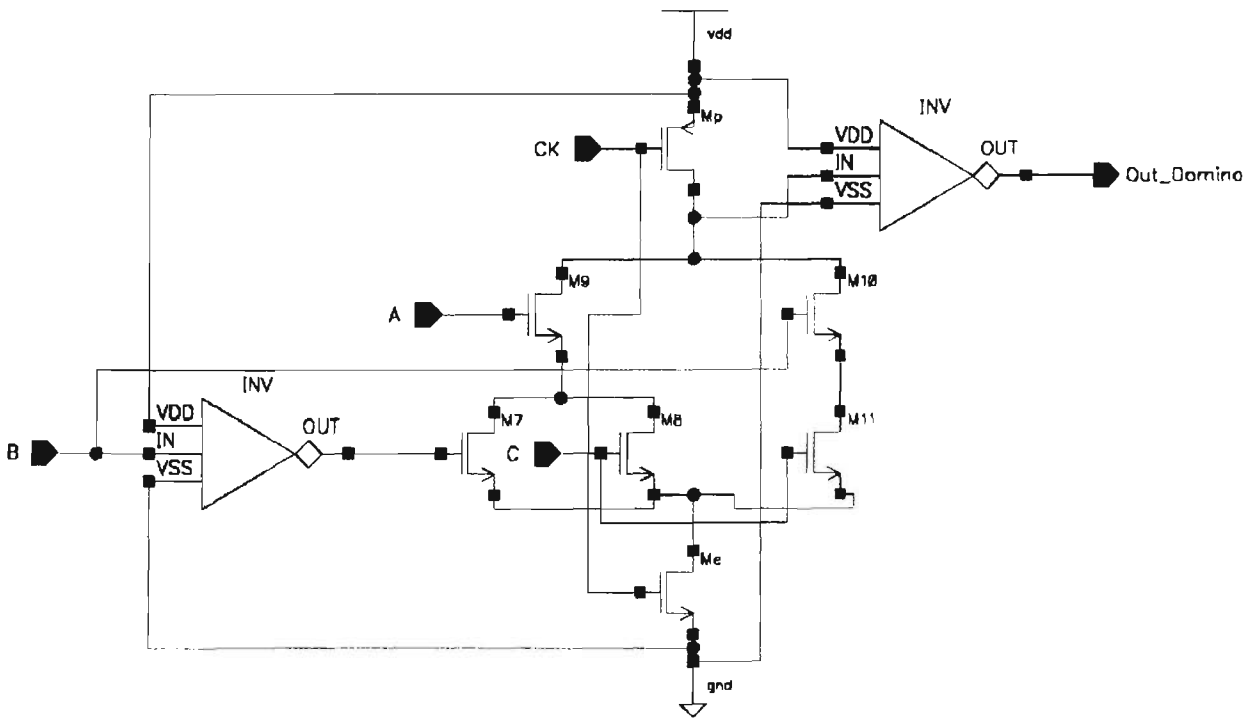



Figure 5.18: Domino structure of encoder used

During precharge, the output of the N-type dynamic gate is charged up to $V_{DD}$ and the output of the inverter is set to 0. During evaluation phase, based on the inputs, the dynamic gate conditionally discharges and the output of the inverter makes a conditional transition from $0 \rightarrow 1$. The input to a Domino gate always comes from the output of another Domino gate. This ensures that all inputs to the Domino gate are set to 0 at end of the precharge period. Hence, the only possible transition for the input during the evaluation period is the $0 \rightarrow 1$ transition. The introduction of the static inverter has the additional advantage that the fan-out of the gate is driven by a static inverter with a low-impedance output, which increases noise immunity.

This circuit has the following properties:

- Since each dynamic gate has a static inverter, only noninverting logic can be implemented.
- Very high speeds can be achieved: only a rising edge delay exists. The static inverter can be optimised to match the fan-out.

## 5.4.2 Layout Considerations

In doing layouts for digital circuits, the speed and the area are the two most important issues. In contrast, in doing layout for analog circuits, performance characteristics such as speed, area, power consumption and timing, should all be considered simultaneously. For example, in an amplifier design, good matching in devices is necessary to minimise the offset voltage, and good shielding is required to protect critical nodes from being disturbed. Without proper layout, the mismatches and the coupled noise would be quite large and would significantly degrade the performance of the amplifiers.

In addition to this, due to the fact that the ADC is a mixed-signal device, mixed signal layout issues must be considered.

### 5.4.2.1 Mixed-Signal Layout Considerations

Naturally, analog ICs are more sensitive to noise than digital ICs. For any analog design to be successful, careful attention must be given to layout issues, particularly in a digital environment. Sensitive analog nodes must be protected and shielded from any potential noise sources. Grounding and power supply routing must also be considered when using digital and analog circuitry on the same substrate. Since the majority of the ADCs use switches, which are controlled by digital signals, separate routing channels must be provided for each type of signal.

Techniques used to increase the success of mixed-signal designs differ in complexity and precedence. Approaches regarding minimisation of noise are very critical and should be considered very seriously. A mixed-signal layout approach is shown in Figure 5.19 [97]. A successful mixed-signal design will always minimise the effect of the digital switching on the analog circuitry.

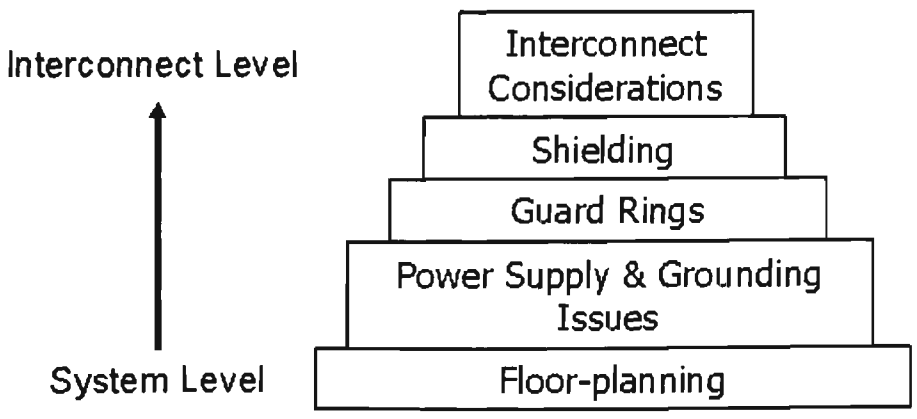



Figure 5.19: Mixed-Signal layout strategy [97].

#### 5.4.2.1.1 Floor-Planning

The position of responsive analog instances can greatly affect the performance of a circuit. Many concerns must be considered. In designing a mixed-signal system, approaches regarding the floor-plan of the circuitry should be analysed before the layout is to take place. The analog circuitry should be classified by the sensitivity of the analog signal to noise. For example, low-level signals or high impedance nodes typically associated with the input signals are considered to be sensitive nodes. These signals should be closely guarded and shielded especially from the digital output pins. High-swing analog circuits such as comparators and output buffer amplifiers should be positioned between the sensitive analog circuits and the digital circuits. The digital circuitry is usually labeled by speed and function. Since digital output buffers are usually designed to drive capacitive loads at very high speeds, they should be kept as far as possible from the sensitive analog signals. The high and low speed digital circuits should be placed between the insensitive analog and the output buffers. Figure 5.20 [99] illustrates these mixed-signal floor-planning approaches.

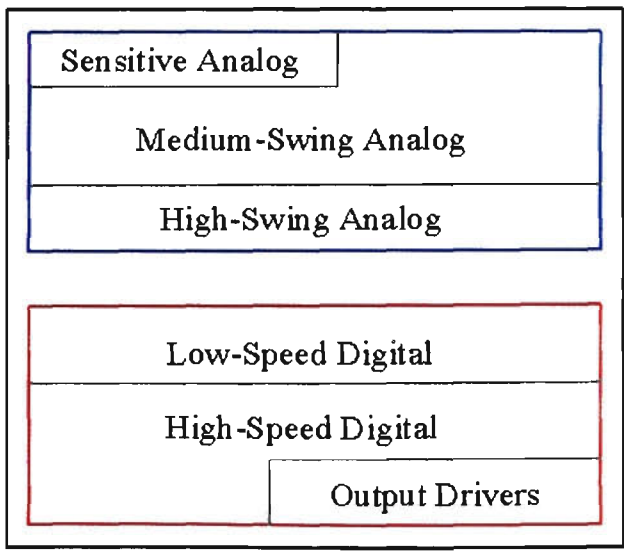



Figure 5.20: Mixed-Signal Floor-Plan [99].

### 5.4.2.1.2 Power Supply and Grounding Considerations

Each time analog and digital circuits are on a same chip, noise could be injected from the digital system to the sensitive analog circuitry through the power supply and ground connections. Much of the intercoupling can be reduced by cautious consideration of how power and ground are supplied to both analog and digital circuits. This phenomenon can be explained with the help of Figure 5.21 [97].

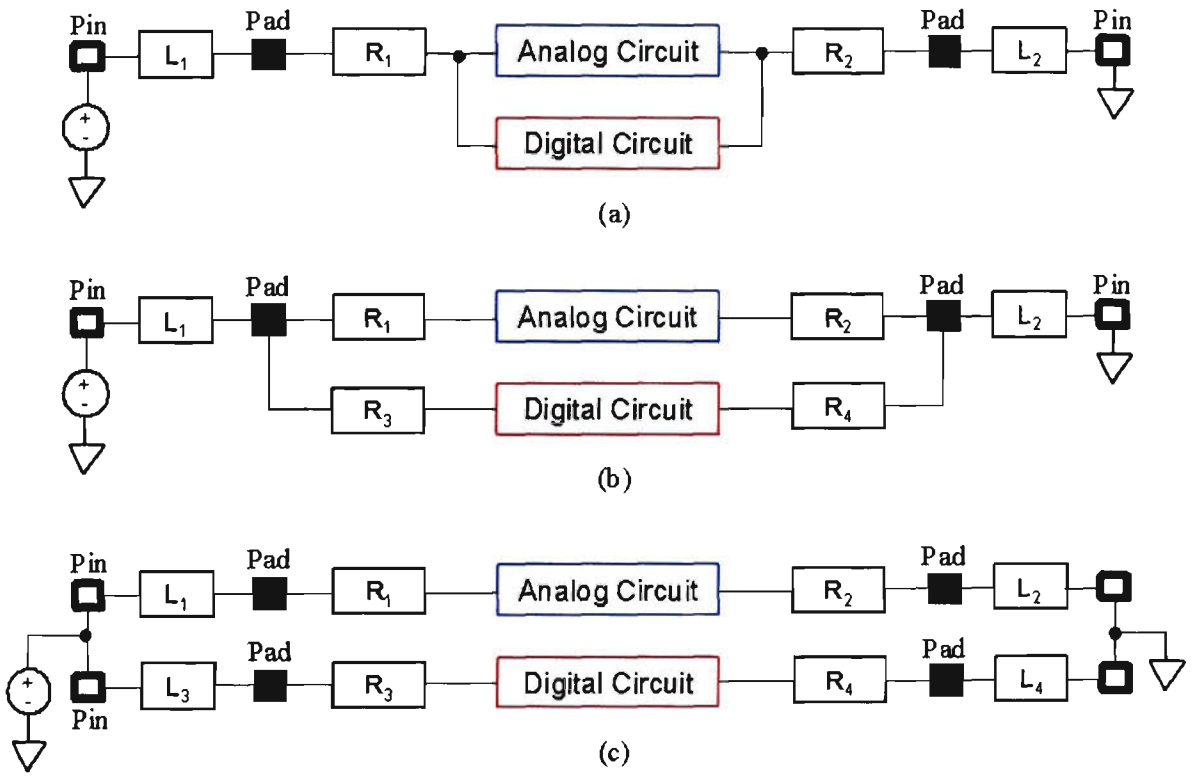



Figure 5.21: Power and ground connection [97].

In Figure 5.21 (a), the analog and digital circuits share the same routing to a single pad for power and ground. The resistors, $R_1$ and $R_2$ represent the small non-negligible resistance of the interconnect to the pads. The inductors, $L_1$ and $L_2$ represent the inductance of the bonding wire which connects the pads to the pin on the lead frame. Seeing as digital circuitry is characterised by high transient currents due to switching, a

small amount of resistance associated with the interconnect can result in major voltage spikes. Low-level analog signals are very sensitive to such interference, therefore resulting in a impure analog system. One way to reduce the interference, illustrated in Figure 5.21 (b), is to exclude the analog and digital circuit from sharing the same interconnect. The routing for the supply and ground for both the analog and digital sections are provided separately. Even though this removes the parasitic resistance due to the common interconnect, there is still a common inductance due to the bonding wire which still will cause interference.

Another method that minimises interference even more that the method illustrated in Figure 5.21 (b), is the method shown in Figure 5.21 (c). By using separate pads and pins, the analog and the digital circuits are completely decoupled. The current through the analog interconnect is much less sudden that the digital, therefore the analog circuitry has a so called "quiet" power and ground. However, this technique is dependent on whether extra pins and pads are available for this use. It is a wise choice to use two separate power supplies because if both types of circuits are not powered up simultaneously, latch-up could easily result.

#### 5.4.2.1.3 Guard Rings

Guard rings should be used wisely throughout a mixed-signal environment. Circuits that process sensitive signals should be placed in a separate well with guard rings around that particular circuit. This is usually performed on the analog sections of the chip layout.

#### 5.4.2.1.4 Shielding

Number of techniques subsist which can shield sensitive, low-level analog signals from noise resulting from digital switching. A shield can take the form of a layer tied to analog ground placed between two other layers, or it can be a barrier between two signals running in parallel.

If at all possible, one should avoid crossing sensitive analog signals, such as low level analog input signals, with any digital signals. The parasitic capacitance coupling the two signal line can be as much as a couple of *fF*, depending on the process. If it can not be avoided, then attempt to carry the digital signal using the top layer of metal. Another situation that should be avoided is running interconnect containing sensitive analog signals parallel and adjacent to any interconnect carrying digital signals. Coupling occurs due to the parasitic capacitance between the lines. If this situation can not be avoided, then an additional line connected to analog ground should be placed between the two signals. This method can also be used to partition the analog and digital sections of the chip.

## 5.4.3 Reconfigurable ADC Layout

The pipeline ADC top-level block diagram is presented in Figure 5.22. Partitioning is a critical aspect of layout implementation and must be considered very decisively. The top level block diagram of the ADC shows all the digital inputs and outputs being at opposites sides as far away from each other as possible. The maximum resolution for the ADC is 16 bits where *Out1...Out16* are the digital output pins. *Vin* is the analog input to the ADC, *Vref* is the input reference voltage, *CLK* is the clock of the system,

*VDD* and *Vss_ang* are the power supply and ground to the analog section, respectively, *Vdd* and *Vss_dif* are the power supply and ground to the digital section respectively, *Vb* is the bias voltage, *Control* is the control signal that activates which and how many pipeline blocks need to be turn 'on', and *Vres* is the final analog output.

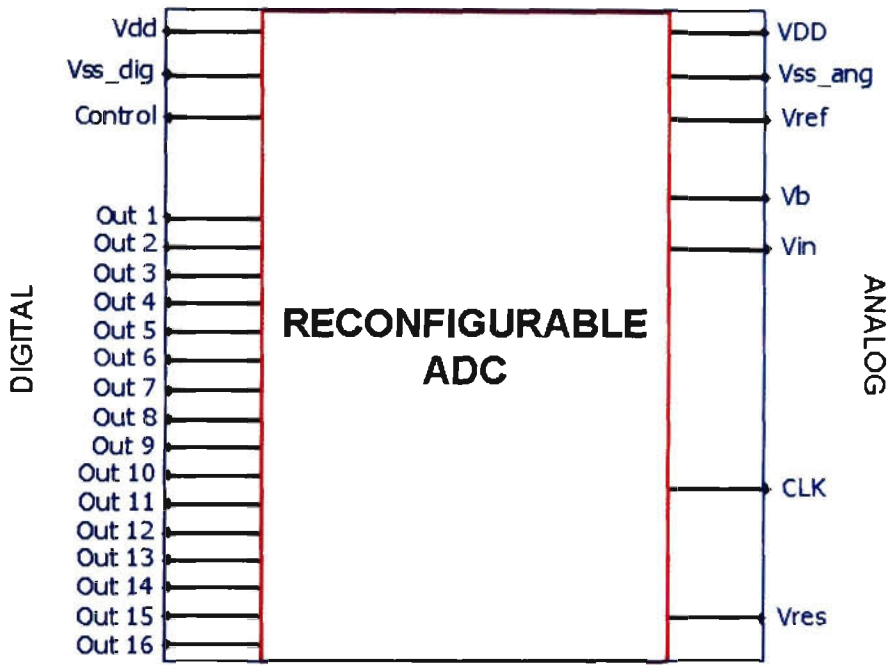



Figure 5.22: Block Diagram of ADC ASIC

The schematic of the ASIC was designed using the Analog Design Environment tool from Cadence and simulated using Spectre simulator. The layout of the ADC was performed on Layout Editor from Cadence using full custom 0.18μm technology. Figure 5.23 illustrates the layout of the 16-bits ADC.

Once again the ADC layout shows the appropriate partitioning with the analog cells being separated from the digital cells. A guard ring around the analog section is also used.

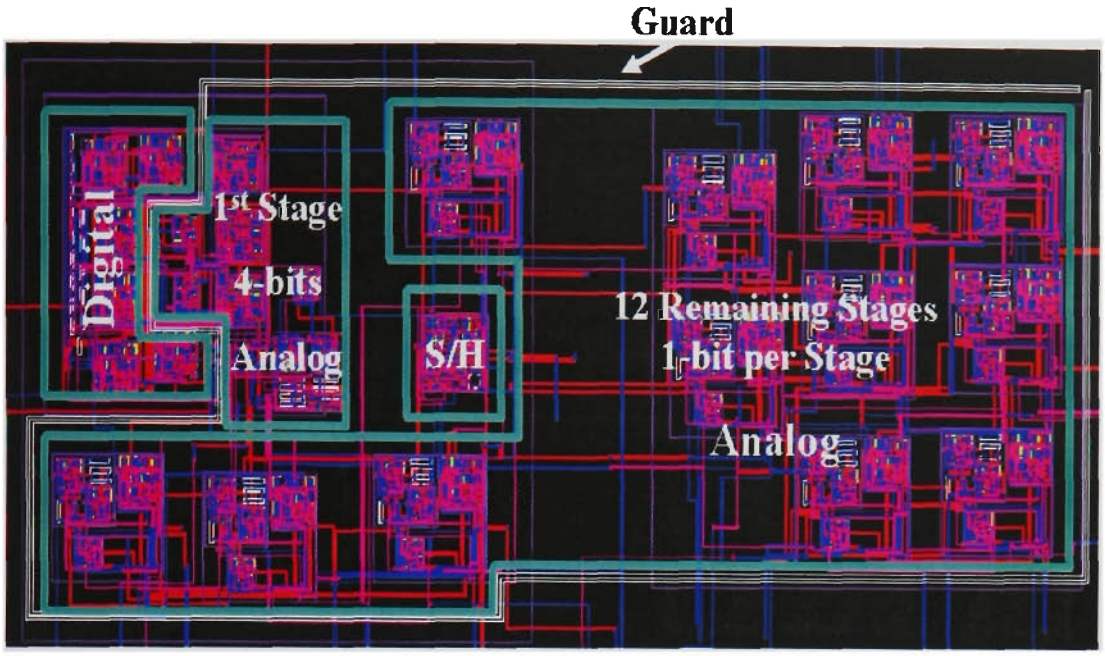



Figure 5.23: Layout of ADC

A performance analysis was completed on the ASIC ADC to ensure it meets timing requirements as well as low power properties. The simulated results are presented in Table 5.4.

Table 5.4: ADC Performance Results

| **Parameter** | **Performance Value** |
|---|---|
| Core Supply Voltage | 2.5 V |
| Maximum Clock Frequency with 16 bits resolution | 60 MHz |
| Required Clock Frequency for UTRA-TDD | 15.36MHz |
| Average Power Consumption @ 15.36 MHz | 3.92 mW |
| Average SNR | 37.88 dB |
| Average DR | 36.12 dB |
| Critical Path | 16.7 nsec |
| Technology | 0.18 μm CMOS |
| INL | 0.39 LSB |
| DNL | 0.43 LSB |
| Core Area | 0.35mm$^2$ |

Figure 5.24 illustrates the dynamic power consumption against the ADC resolution. Appendix C describes the Cadence power consumption measurement flow.

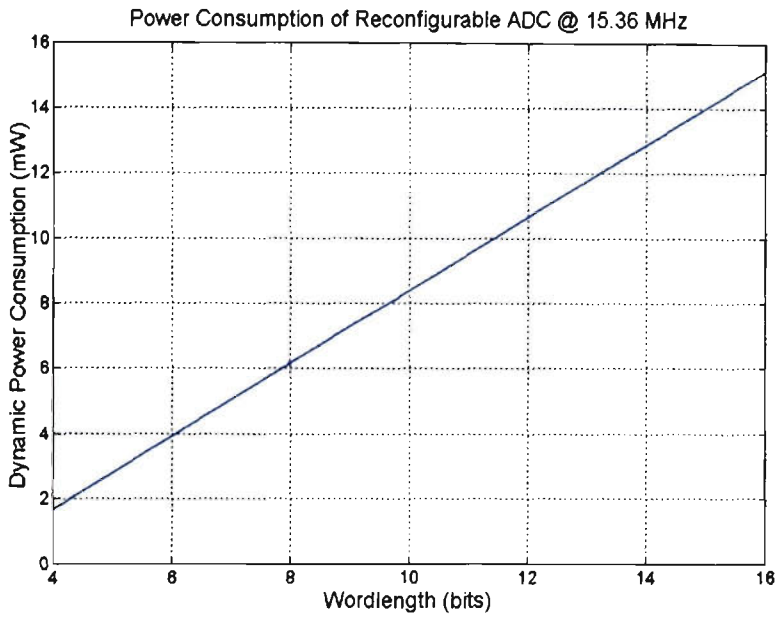



Figure 5.24: Dynamic Power Consumption of ASIC components in ADC at 15.36 MHz

It is clear that as the word length increases, the power consumption increases proportionally. The power consumption ranges from 1.68mW to 15.12mW for word lengths of 4 bits to 16 bits respectively. The power consumed by the new reconfigurable ADC architecture can be given by:

$$P_{ADC} = \left(\frac{n}{\xi}\right) P_{BLOCK} + P_{S/H} + P_{DEC} \qquad (16)$$

where $n$ is the scalable word length, $P_{BLOCK}$ is the dynamic power consumption of a specific ADC block of $\xi$ bits, $P_{S/H}$ is the power consumed by the front end S/H, and $P_{DEC}$ is the power consumed by the digital error correction circuit. Table 5.5 tabulates the power consumption for the variable word length ADC. A maximum power reduction of 88.89 % has been recorded excluding the DSP control unit, when only 4-bits are

required. The average power consumption is 3.92mW, providing an average power saving of 74.07 %.

Table 5.5: Power Consumption of Reconfigurable ADC

| Resolution (Bits) | Power Consumption (mW) | Power Saving (%) |
|---|---|---|
| 4 | 1.68 | 88.89 |
| 5 | 2.80 | 81.48 |
| 6 (average) | 3.92 | 74.07 |
| 7 | 5.04 | 66.67 |
| 8 | 6.16 | 59.26 |
| 9 | 7.28 | 51.85 |
| 10 | 8.40 | 44.45 |
| 11 | 9.52 | 37.04 |
| 12 | 10.64 | 29.63 |
| 13 | 11.76 | 22.22 |
| 14 | 12.88 | 14.81 |
| 15 | 14.02 | 7.41 |
| 16 | 15.12 | 0.00 |

## 5.5 Conclusion

This chapter presented the design and implementation of the reconfigurable pipeline ADC intrinsic to the UTRA-TDD mobile station receiver. As the quantisation noise is a concerning topic within the receiver ADC, a fixed resolution ADC will not be an efficient design. The intension of the reconfigurable ADC is to provide a solution to the cost issues associated with the TDD system. In other words, to increase the battery life of the mobile station by minimising the power dissipation. The reconfigurable topology in real-time, observes the in-band and out-of-band powers, and by employing an intelligent algorithm, calculates the required resolution and switches the pipeline blocks '*on*' or '*off*' accordingly. Due to this condition only the required pipeline blocks will be switched '*on*', resulting in longer battery life.

A sampling frequency of 15.36MHz was used, due to the 3GPP specification, before down sampling the data by a decimation factor of 4. This was performed due to the interpolation factor of 4, which is used in the transmitter. The algorithm formulation for the reconfigurable ADC concluded that three signals are required to determine the appropriate $Q_n$ that gives the overall required resolution. This led to the proposal of the system architecture presented in Section 5.2.2.

The reconfigurable ADC system consisted of a number of components, namely, pipeline ADC structure with resolution switches managed by the control unit, a RRC filter with a fixed ACP value of 33 dB, a decimation factor of 4 to compromise the interpolation factor within the transmitter, and a signal power measurement components to provide clearly varying amplitudes of each three input signals to the control unit. The control unit calculates the appropriate $Q_n$ values and its corresponding bit values. A LUT is then employed to determine how many blocks of the pipeline chain need to be switched '*on*' to provide the required resolution.

A static, statistical analysis on the reconfigurable ADC was performed which in fact justified the design of a reconfigurable topology. ASIC implementation using 0.18μm technology was performed on the overall reconfigurable ADC. Performance analysis in terms of power consumption was also presented, showing the significant power saving of the reconfigurable ADC in contrast to a fixed 16-bits ADC.

# Chapter 6

# *Effect of Scalable Filter on the Reconfigurable ADC Architecture*

## 6.1 Introduction

Chapter 5 presented a reconfigurable pipeline ADC architecture for a mobile terminal receiver with a fixed filter. The reconfigurable phenomenon of the ADC was provided by a measure of the quantisation noise ($Q_n$) calculated by an intelligent algorithm of the control unit, resulting in a variable ADC resolution. The inputs to the control unit came after the filter within the receiver with a fixed *ACP* of 33 dB. This research is further extended by combining both the ADC and the RRC filter of the receiver, meaning that the $Q_n$ and the *ACP* be both variable, to see what effect a scalable filter, with variable filter lengths would have on the reconfigurable ADC. The motivation for this design is that the filter in the mobile receiver is also one of the major components that consumes vast amounts of battery power. An optimum balance factor between the ADC and the filter is found, optimising the power consumption between the two designs. This makes the architecture power efficient and only consuming minimum power to meet the signal-to-noise ratio of the system.

The combined reconfigurable architecture (CRA) for an UTRA-TDD mobile terminal receiver is described in this chapter. The reconfigurable architecture consists of a digital filter with a variable filter length and a variable word length pipelined ADC. The filter length and word length depend on the in-band and out-of-band power ratios. When *ACI* and co-channel interference (*CCI*) are low, the required number of filter coefficients (taps) and word length (bits) of the ADC are reduced which leads to lower power consumption. This is desirable in battery-powered terminals to increase talk and standby times. The downlink TDD mode of UMTS UTRA was once again chosen due to its near far problem to demonstrate the power saving capabilities of this architecture.

Figure 6.1 presents the direct conversion UTRA-TDD mobile terminal receiver, with a reconfigurable ADC and filter. The control unit accepts three signals (in-band, out-of-band and desired signal) with clearly varying amplitudes, obtained by the full wave rectifiers and the averaging filters. The basic concept of the combined reconfigurable architecture is to only utilise the required filter adjacent channel selectivity (*ACS*) to meet the required *Eb/No*. It also assigns any remaining noise available in the system to quantisation noise of the ADC. The concept of the filter is similar to that of the ADC. If adjacent channel interference and intra-cell interference powers are low, the *ACS* of the filter can be reduced and the resolution of the ADC can be decreased to a level that satisfies the *Eb/No*, therefore saving battery power. If *ACI* and intra-cell interference powers have been increased, then the *ACS* of the filter and the resolution provided by the ADC may have to increase in order to meet the *Eb/No* ratio. Once this is performed, the control unit calculates the most efficient filter length and ADC word length to reconfigures the filter and ADC respectively.

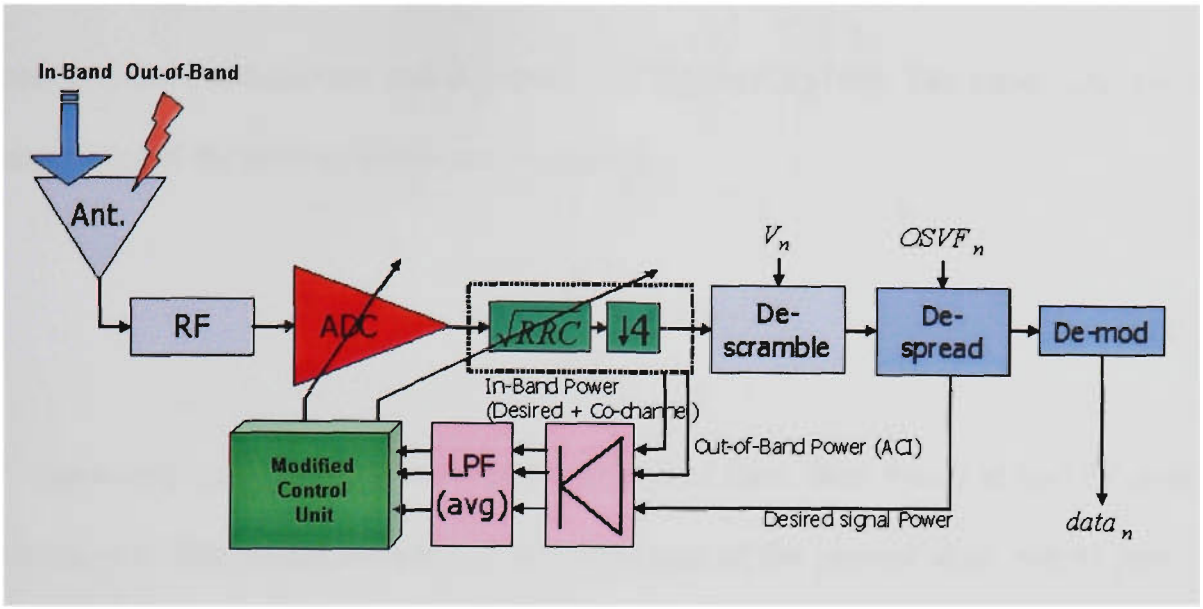



Figure 6.1: UTRA-TDD mobile receiver with reconfigurable ADC and Filter

## 6.2 System Design

The combined reconfigurable architecture is described in this section. The architecture consists on a number of components to enable a scalable $ACP$ and $Q_n$. Firstly, the filter considerations are listed and described, containing the filter type and the interference model of the filter.

Secondly, the algorithm enabling the ADC and filter to exploit scalable $Q_n$ and $ACP$ values is formulated and the corresponding system architecture is introduced. The subsequent sections describe the analysis of the scalable filter, and then the effect of the filter on the reconfigurable ADC is presented and analysed.

### 6.2.1 Filter Considerations

Digital finite impulse response (FIR) filters can be implemented using various architectures. The direct form or otherwise known as the transversal structure is the

most common architecture and is depicted in Figure 6.2 [100]. The input, *x(n)* and the output *y(n)* of the filter structure are related by:

$$y(n) = \sum_{m=0}^{M} b_m \bullet x(n-m) \tag{6.1}$$

$z^{-1}$ represents a delay unit of one sample or unit of time, thus, *x(n-1)* is *x(n)* delayed by one sample. The output sample is a weighted sum of the present input and *M* previous samples of the input.

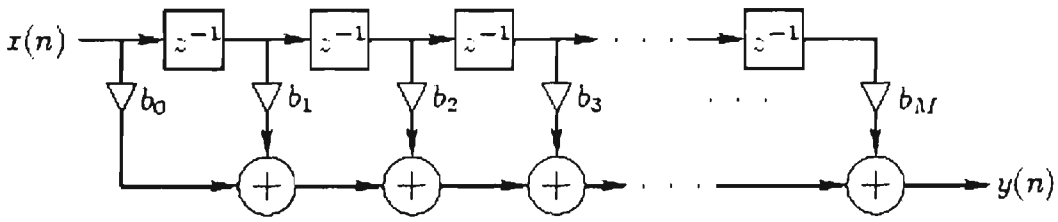



Figure 6.2: Transversal FIR filter structure [100]

The computation of each output sample requires the following hardware [100]:

- *M* memory locations to store the input samples
- *M+1* memory locations to store the coefficients
- *M* multiplication operations
- *M* addition operations.

A linear phase structure is a variation of the transversal structure, which takes advantage of symmetrical coefficients and in effect, uses half the required multiplications and additions. The only disadvantage is more complex indexing of data is required. For odd and even phase filters, the transfer function *H(z)* can be written as [97]:

$$H(z) = \sum_{m=0}^{M/2-1} b_m \left(z^{-m} + z^{-(M-m)}\right) + b\left(\frac{M}{2}\right) z^{-(m/2)} \qquad M \text{ odd} \quad (6.2)$$

$$H(z) = \sum_{m=0}^{(M+1)/2-1} b_m \left(z^{-m} + z^{-(M-m)}\right) \qquad M \text{ even} \quad (6.3)$$

where $z^{-m}$ is the filter delay with $m$ varying from 0 to ($M$/2-1), $M$ is the number of filter coefficients (taps), and $b_m$ is the actual coefficient of the filter. The corresponding difference equations are as follows [100]:

$$y(n) = \sum_{k=0}^{M/2-1} b_m x(m-k) + x\left(m-(M-k)\right) + b\left((M)/2\right) x\left(m-(M/2)\right) \qquad M \text{ odd} \quad (6.4)$$

$$y(n) = \sum_{k=0}^{M/2-1} b_m x(m-k) + x\left(m-(M-k)\right) \qquad M \text{ even} \quad (6.5)$$

where $x$ is the input signal with $k$ varying from 0 to ($M$/2-1). Figure 6.3 [100], illustrates the linear phase structure where seven coefficients are used.

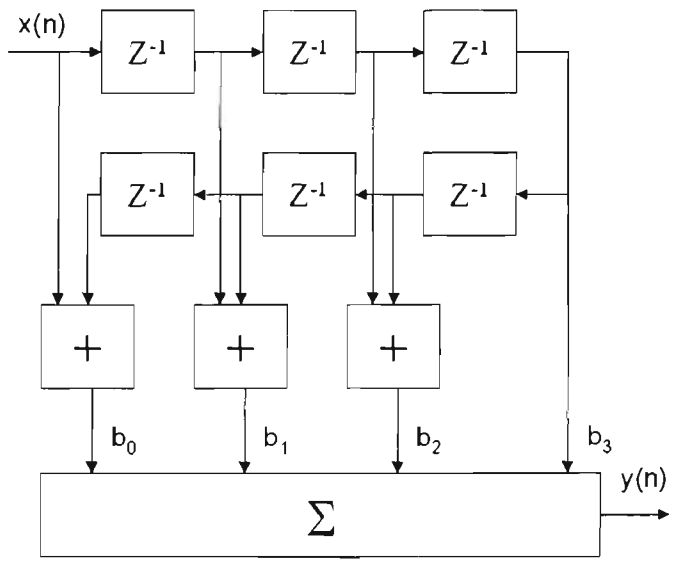



Figure 6.3: Linear Phase FIR filter structure [100]

Numerous optimisation techniques exist for reducing power dissipation in complex digital FIR filter implementations for next generation telecommunications equipment [101-109]. These techniques will not reduce it to its most efficient structure as they are not reconfigurable. In order to even consider the design of a reconfigurable filter, the *ACP* and the *ASC* models must be obtained.

## 6.2.2 Scalable RRC Filter

This section describes the digital scalable filter. The filter is a pulse-shaping filter with a FIR. The equation is as follows:

$$y(n) = \sum_{j=0}^{N-1} x(n-j) \cdot b(j) \tag{6.6}$$

where *y(n)* is the filter output sample at *'n'*, *x(n-j)* defines the input samples delayed by *'j'* samples, *b(j)* defines the filter coefficients. *N* is the filter length. The impulse response of the pulse-shaping filter is a root-raised cosine (RRC), $RC_0(t)$, defined by the 3GPP and given by [96]:

$$RC_0(t) = \frac{\sin\left(\pi \frac{t}{T_C}(1-\alpha)\right) + 4\alpha \frac{t}{T_C} \cos\left(\pi \frac{t}{T_C}(1+\alpha)\right)}{\pi \frac{t}{T_C}\left(1 - \left(4\alpha \frac{t}{T_C}\right)^2\right)} \tag{6.7}$$

where the roll-off factor $\alpha = 0.22$ and $T_c$ is the chip duration of 2.6042e-7 seconds. The reconfigurable digital filter system block diagram is presented in Figure 6.4. The system

block diagram presents the basic operation of the filter. The system employs a folded FIR structure, and shaves off and adds taps to the ends of the impulse response to lower or raise the stop band dB level. The components in the system are a variable low pass filter (LPF); high pass filter, two full wave rectifiers, two simple LPF filter networks and a control unit that determines how many taps are needed to attenuate interference.

As the receiver deals with a complex signal, it may not be necessary to have the control loop on both in-phase (real) and quadrature (imaginary) signals. It may be sufficient for the in-phase filter to control the tap length for both itself and the quadrature filter. Therefore, the control unit applies only to the in-phase filter.

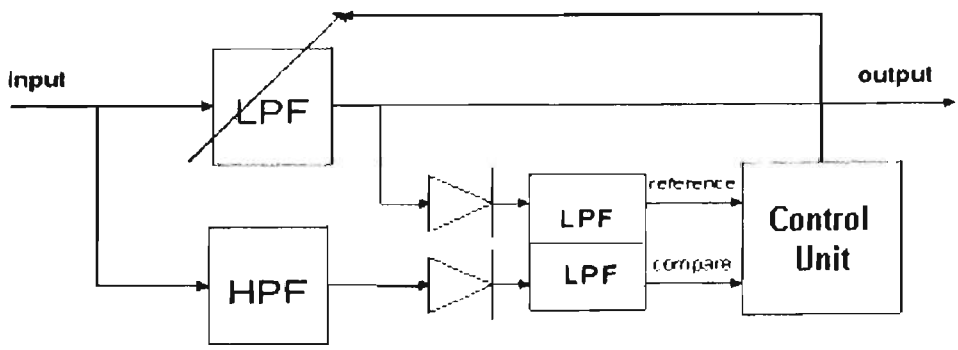



Figure 6.4: Reconfigurable Digital Filter System

Figure 6.5 shows in detail how the filter taps using the intelligent control unit algorithm, are shaved off. The output of the control unit is also sent to the ADC to control the resolution. The figure also depicts the operation of the LPFs, resulting in a high pass signal.

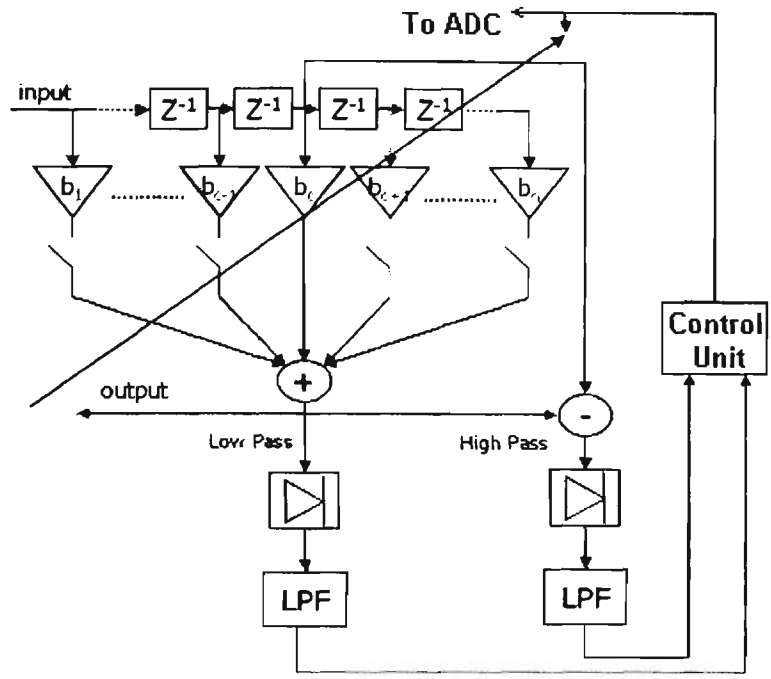



Figure 6.5: Scalable Digital Filter System (Detailed)

The software/hardware partition of the filter architecture is presented in Figure 6.6.

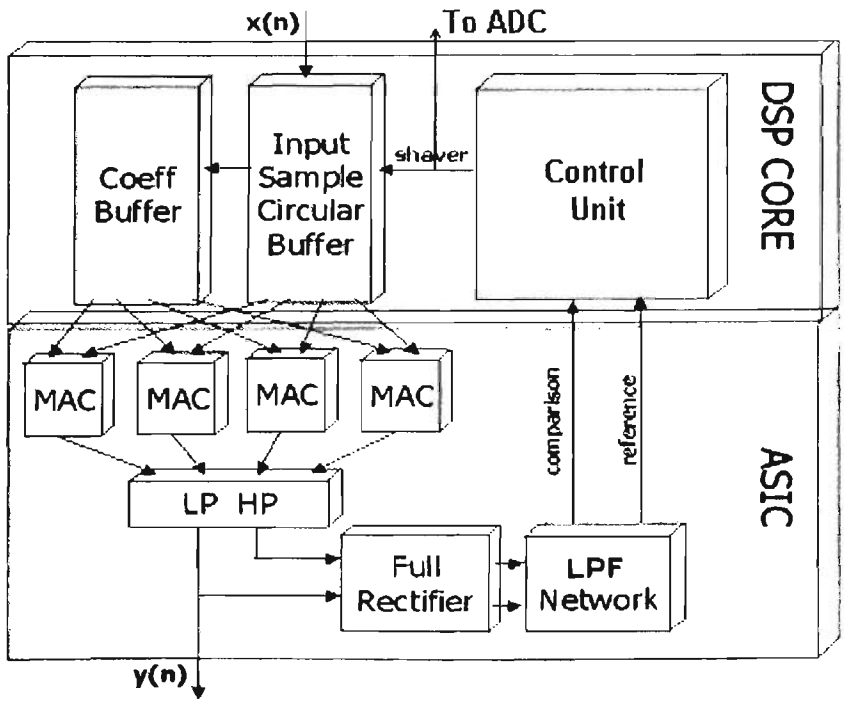



Figure 6.6: Scalable Digital Filter Architecture

The architecture presents details of the system block diagram. It consists of a DSP core and an ASIC. The DSP core is used for the control unit, coefficient buffer and input sample buffer. The ASIC using standard digital libraries consist of four multiply-accumulate (MAC) units, a LPHP block that outputs the desired low pass and unwanted high pass signals, a full wave rectifier and the LPF networks.

### 6.2.3 Modified Control Unit

The control unit of the combined reconfigurable architecture required modification in order to take care of scalable filter lengths as well as reconfigurable ADC resolution. The modified control unit calculates the appropriate filter length and word length for the filter and ADC respectively. The equation for the control unit is derived from the signal-to-noise ratio (SNR) similar to that in [102] and is as follows:

$$Eb/No = \frac{Prx^{i} pg}{Prx^{i}(M-1) + \frac{I_{total}{}^{i}}{ACP^{i}} + \eta + Q_{n}{}^{i}} \tag{6.9}$$

where $Prx^{i}$ is the received desired signal power at the $i^{th}$ MS in the cell of interest (COI). Processing gain is defined as $pg$. $Prx^{i}(M-1)$ is co-channel interference where $M$ is the number of users in the COI. The adjacent channel protection factor is defined by $ACP^{i}$. Thermal noise is given by $\eta$. $I_{total}{}^{i}$ is the ACI signal received. It is mathematically represented as:

$$I_{total}{}^{i} = \sum_{j=1}^{H} \frac{Ptx^{j} M^{j}}{\kappa^{j} B_{m}} \tag{6.10}$$

where $\kappa^{j}{}_{B_m}$ is the path loss between the $j^{th}$ adjacent channel BS causing interference and the mobile located at $m$ in the COI. $M^j$ is the number of users served by the $j^{th}$ BS. $Ptx^j$ is the $j^{th}$ adjacent BS transmission power. $Q_n{}^i$ is remaining noise in the system and is defined as the quantisation noise:

$$Q_n{}^i = G_k \bullet \frac{I_{total}{}^i}{ACP^i} \tag{6.11}$$

where $G_k$ is a gain control factor balancing $Q_n{}^i$ and $ACP^i$. If $G_k$ is set to zero, the $ACP^i$ will be at a minimum, therefore leaving no margin of error for $Q_n{}^i$. Solving for $ACP^i$ results in:

$$ACP_{scaled}{}^i = \frac{(Gk+1)I_{total}{}^i}{\left(1+\frac{pg}{Eb/No}\right)\Pr x^i - \eta - \Pr x^i M} \tag{6.12}$$

where $Prx^iM$ is the in-band signal. The actual attenuation of the filter is referred to as adjacent channel selectivity ($ACS$). The ACS depends on the Adjacent Channel Leakage Ratio ($ACLR$) as well as the $ACP$ requirement. The $ACLR$ is the ratio of the transmitted interference power to the power measured after a receiver filter in the out-of-band channels. The relationships have been investigated in [110] and it is found that:

$$ACS^i = \frac{1}{\frac{1}{ACP^i} - \frac{1}{ACLR}} \tag{6.13}$$

From Equation 6.13 it is clear that the ACP factor will be scaled higher as the $ACI$ is scaled by a factor of ($G_k$+1). Hence, if the $Eb/No$ ratio is calculated, it will be higher than the target allowing the difference to be utilised as quantisation noise. With the new

calculated value for the *ACP*, the quantisation noise can be calculated in the control unit as in Equation 6.11. This control unit accepts the three inputs, similar to the control unit of chapter 5, and by using appropriate algorithms, it determines how many taps or bits are required to be shaved off or added on to ensure the *Eb/No* is met at all times. The control unit now sends a *shaver* signal to the coefficient and input sample buffer adjusting their pointers with an offset. The shaver signal switches taps 'on' or 'off' in the FIR structure. It is defined as:

$$shaver = \frac{Max_{flength} - New_{flength}}{2} \tag{6.14}$$

where $Max_{flength}$ is the maximum filter length available and $New_{flength}$ is the new calculated filter length. For example, if $New_{flength}$ is 19 and $Max_{flength}$ is 65, the shaver is then set to 23. Therefore, 23 taps from each end of the impulse response will be switched off and the other will be switched on. It also sends a signal to the ADC that control how many blocks need to be activated. The changes take place for the next frame input to the filter. The new tap length will also apply to the quadrature filter. The feedback is performed constantly per frame to ensure the minimum number of taps and bits are used. Figure 6.7 presents numerous frequency response plots of the pulse-shaping filter as taps are shaved off the tails of its impulse response. The LUT employed in the control unit that takes care of the reconfigurable filter is illustrated in Table 6.1, where the filter length ranges from 5 to 65 taps with a margin of 4 in between them. The LUT acquires the corresponding shaver value with the calculated *ACP* factor and after each sample, the filter will reconfigure its value. Concurrently, the resolution of the ADC is also being reconfigured.

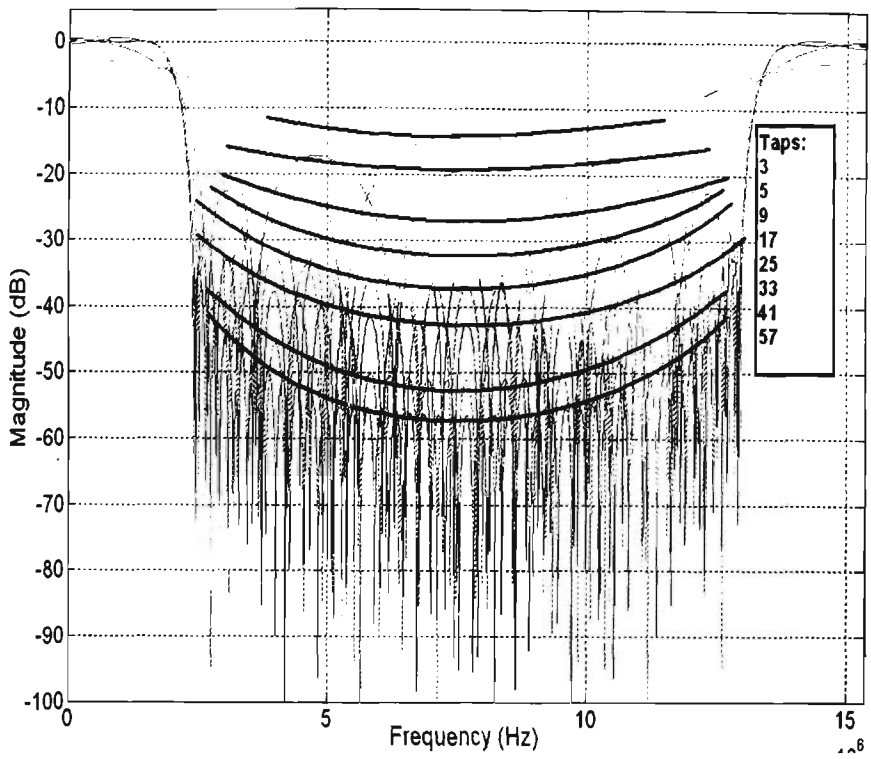



Figure 6.7: Frequency Response using various filter lengths

Table 6.1: Modified Control Unit Look-Up Table for Filter

| ACP (*dB*) | ACS (*dB*) | Filter Length | Filter Shaver |
|---|---|---|---|
| 44.8 < & ≤ 44.9 | 60 | 65 | 0 |
| 44.7 < & ≤ 44.8 | 58 | 61 | 2 |
| 44.5 < & ≤ 44.7 | 56 | 57 | 4 |
| 43.8 < & ≤ 44.5 | 54 | 53 | 6 |
| 43.6 < & ≤ 43.8 | 50 | 49 | 8 |
| 43.2 < & ≤ 43.6 | 49 | 45 | 10 |
| 42.0 < & ≤ 43.2 | 48 | 41 | 12 |
| 38.8 < & ≤ 42 | 45 | 37 | 14 |
| 36.4 < & ≤ 38.8 | 40 | 33 | 16 |
| 34.6 < & ≤ 36.4 | 37 | 29 | 18 |
| 29.8 < & ≤ 34.6 | 35 | 25 | 20 |
| 27 < & ≤ 29.8 | 30 | 21 | 22 |
| 25 < & ≤ 27 | 27 | 17 | 24 |
| 20 < & ≤ 25 | 25 | 13 | 26 |
| 14 < & ≤ 20 | 20 | 9 | 28 |
| ≤ 14 | 14 | 5 | 30 |

Further analysis on the inter symbol interference of the filter was required to determine what should be the minimum filter length to ensure the *Eb/No* requirement is met. A base band transceiver simulation model was created to measure the effect of shaving taps off with respect to inter symbol interference (ISI). The specifications for this simulation model are presented in Table 6.2.

Table 6.2: Base Band Transceiver Parameters

| **Parameter** | **Value** |
|---|---|
| Number of users | 8 |
| OSVF Code length | 16 |
| Bit rate | 16 Kbps |
| MS Rx RRC Filter roll off factor | 0.22 |
| BS Tx RRC Filter roll off factor | 0.22 |
| # of taps in Tx RRC Filter | 41 |

Analysis shows that as taps are shaved off the filter, there is an increase in error vector magnitude (EVM) when analysing the received symbols. This leads to an increase in ISI, which is defined as:

$$ISI^{j} = 10 \cdot \log_{10}\left(mean\left(EVM(n)^{2}\right)_{j}\right) \tag{6.15}$$

where $EVM$ is a vector of $n$ samples and $j$ corresponds to a certain filter length. Figure 6.8 presents the results of the ISI analysis. Overall, the ISI reduces when the filter

length increases as expected. However, the reduction is not smooth because certain filter lengths have better ISI than others. The required signal-to-noise ratio for adequate performance is 6.5dB (2 * *Eb/No*) for a QPSK modulator, obtained by using an *Eb/No* of 3.5dB, specified by the 3GPP. ISI power should be made much less than –6.5dB if it is not to affect the noise performance of the receiver. An additional safety margin of 20dB to take care of any additional interference in the system would be acceptable, resulting in –26.5dB of ISI. Therefore, acceptable filter lengths are all the troughs in Figure 6.8 under -26.5dB, such as 5, 11, 13 and ≥ 19. The minimum filter length is 5.

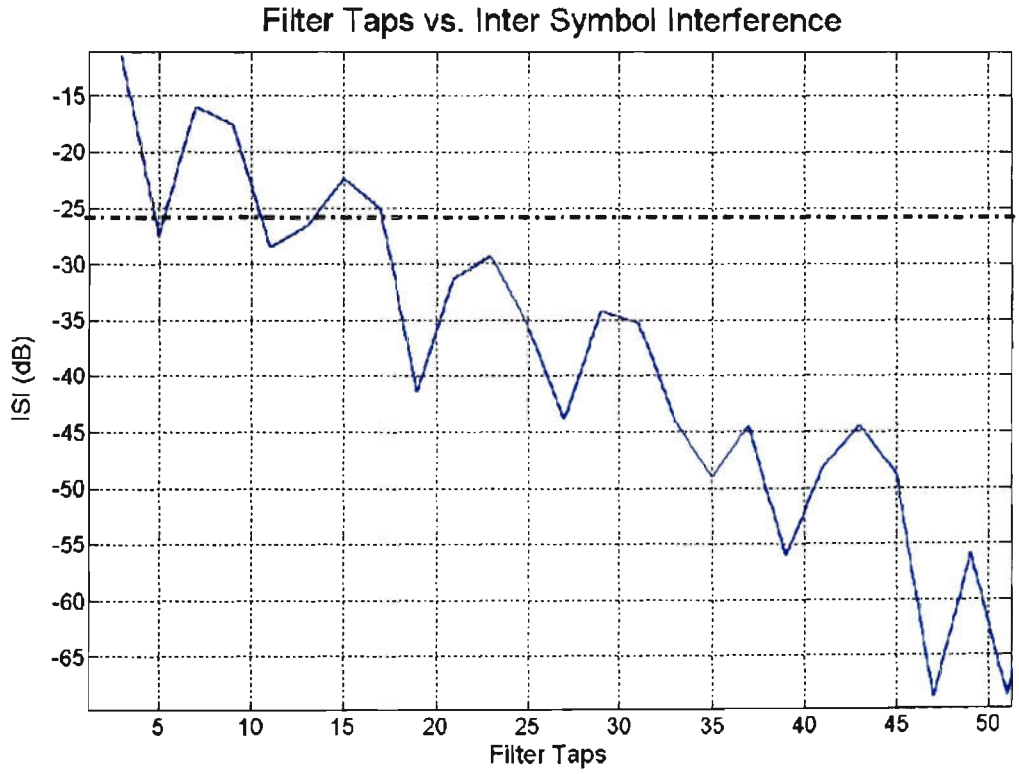



Figure 6.8: Inter-Symbol Interference Analysis

Based on the above algorithm the structure of the reconfigurable ADC with a scalable filter is illustrated in Figure 6.9.

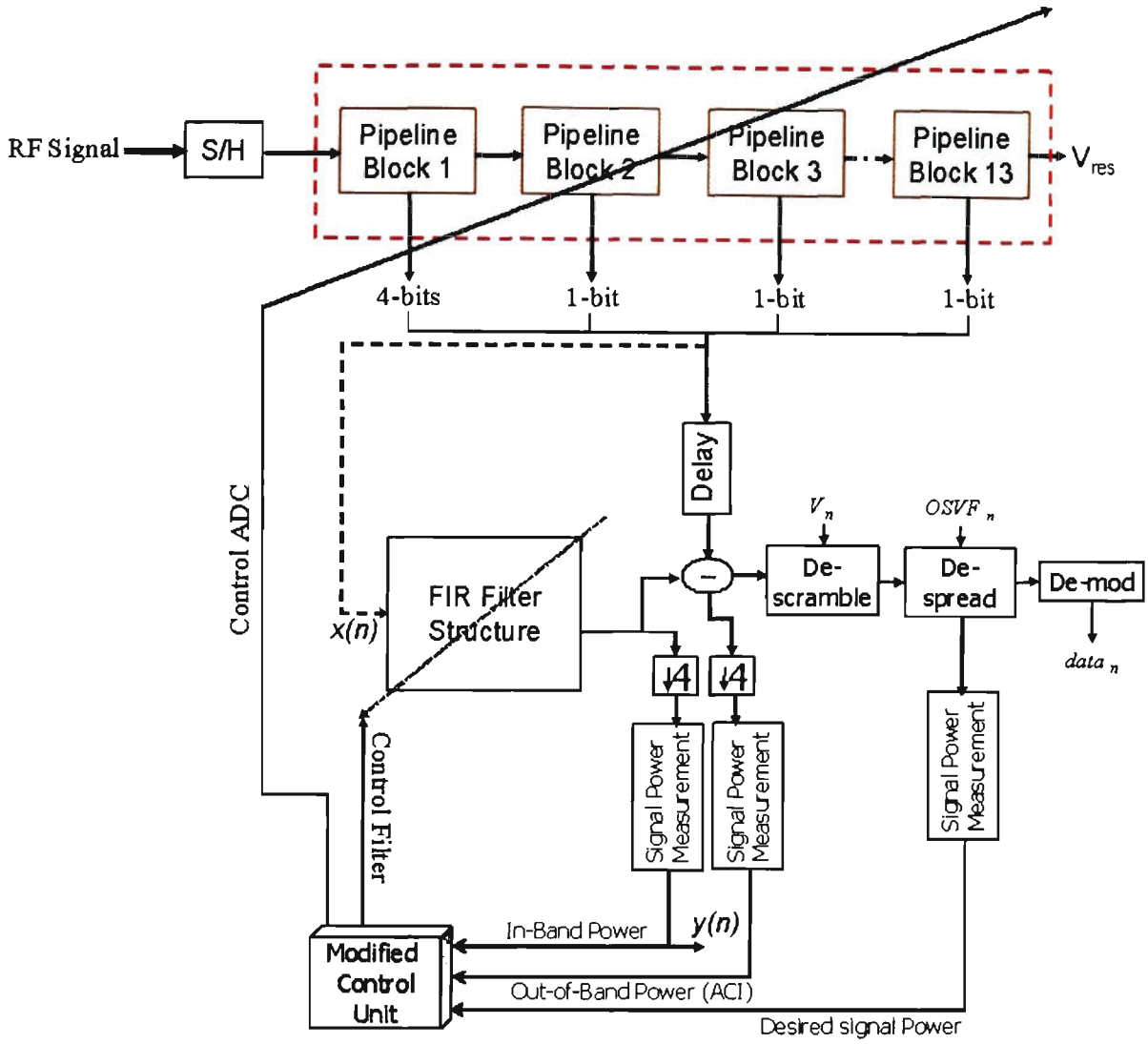



Figure 6.9: Combined Reconfigurable Architecture (CRA)

## 6.3 Statistical Analysis

A statistical analysis of the CRA, in a static environment to see the effect of the scalable filter on the reconfigurable ADC is presented in this section. The analysis divulges the efficiency of the CRA in the UTRA-TDD environment. The analysis on the CRA provides an estimated power consumption savings in percentages, as compared to a fixed ADC and filter structure. Simulation parameters for this design are listed in Table 6.3.

Table 6.3: Simulation Parameters

| Parameter | Value |
|---|---|
| Standard deviation, σ (dB) | 12 |
| Gain Factors, Gk | 0.001, 0.1, 0.5, 1, 2, 4, 6, 8, 10 |
| Bit Rate | 32 Kbits/s |
| Max TX Power (dBm) | Downlink: 10, Uplink: 4 |
| Thermal Noise (dBm) | -102.85 |
| Required Eb/No (dB) | 3.5 |
| Receiver Sensitivity, without Imargin (dBm) | -112.89 |
| Cell Radius (m) | 100 |
| # of Interfering Adjacent Cells | 7 |
| # of users in each Interfering Adjacent Cell | 8 |
| Synchronisation factor α | Uniform random 0 to 1 |
| Path loss exponent γ | 3.0 |

A range of gain factors, $G_k$, values are used to achieve a comparison between the averages of the ADC resolution and the RRC filter *ACP* factors. A lognormal shadowing variable standard deviation of 12 dB is employed as per statistical analysis of the reconfigurable ADC presented in chapter 5. Figure 6.10 illustrates the CDF of the filter *ACP* factors and the ADC resolution by Monte Carlo simulations of equation 6.12 and the bit value ($n^i$) equation shown as:

$$n^i = \frac{10 \bullet \log 10\left(\frac{(ACI^i + \Pr x^i) \bullet Decimation_F}{Q_n^{\,i}}\right)}{6.02} + Safety_M \qquad (6.16)$$

where $ACI^i$ is the adjacent channel interference, $Decimation_F$ is the decimation factor of 4, specified by the 3GPP, $Q_n^{\,i}$ is the quantisation noise of the system, and $Safety_M$ is a safety margin employed to take care of some large spikes at the input. The analysis presented is for $G_k$ values of 0.001 to 2. Figure 6.11 illustrates the results for $G_k$ values

between 4 and 8. Table 6.4 corresponds to the recorded results of the figures where the mean and standard deviation are listed.

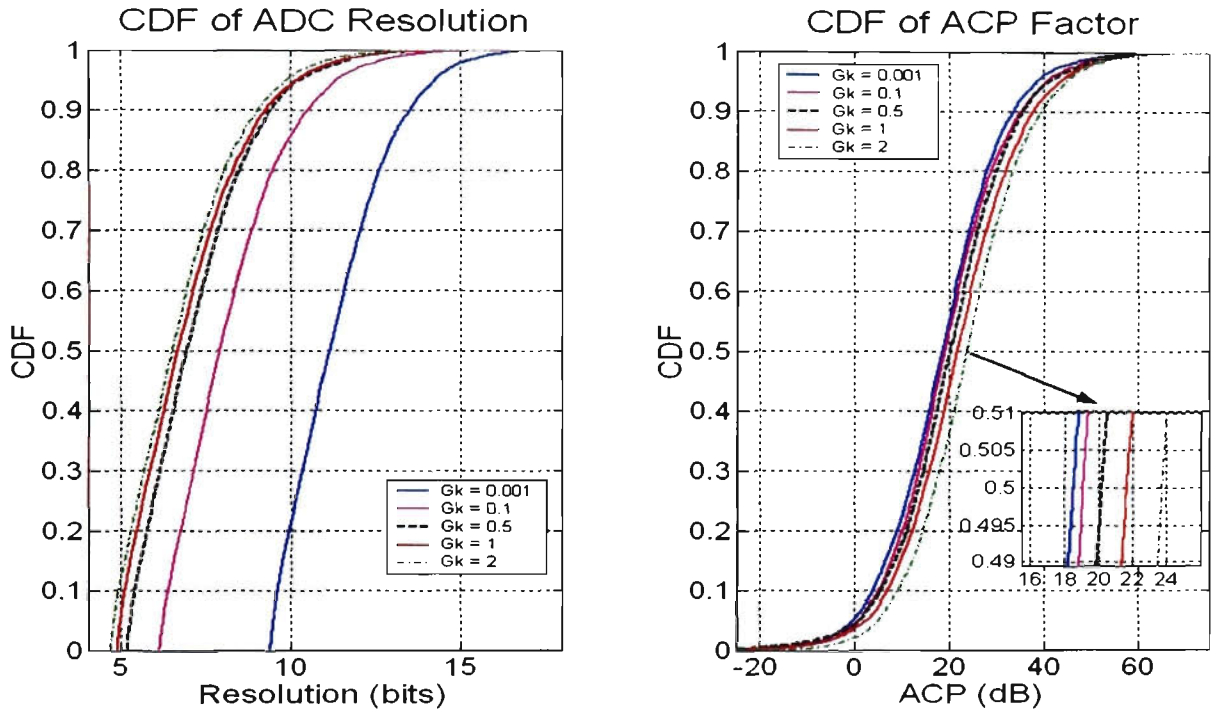



Figure 6.10: Statistical analysis of CRA ($G_k$ = 0.001 → 2)

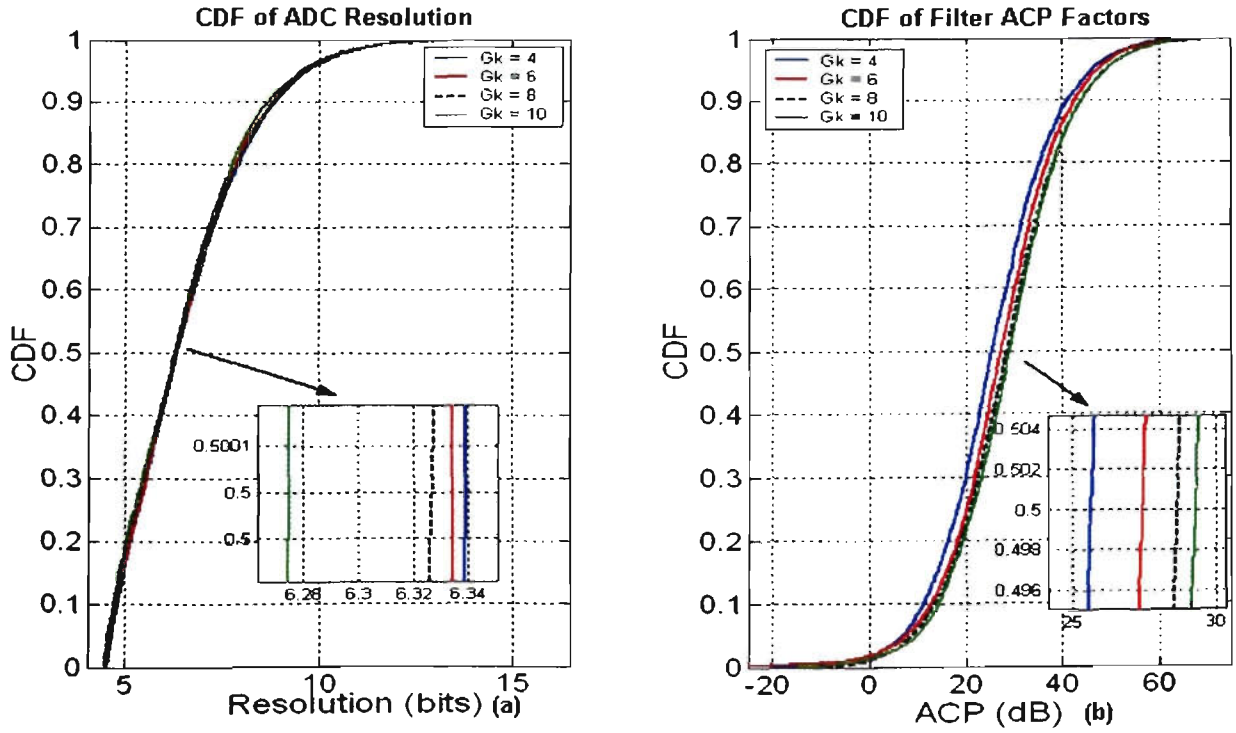



Figure 6.11: Statistical analysis of CRA ($G_k$ = 4 → 10)

Table 6.4: Statistical analysis results of CRA

| ***Gain Factor,*** $G_k$ | ***Mean (Bits)*** **(dB)** | ***STD (Bits)*** **(dB)** | ***Mean (ACP)*** **(dB)** | ***STD (ACP)*** **(dB)** |
|---|---|---|---|---|
| 0.001 | 11.3780 | 1.5094 | 18.7144 | 12.2275 |
| 0.1 | 8.2394 | 1.6481 | 19.7445 | 12.2294 |
| 0.5 | 7.2403 | 1.6214 | 20.4441 | 12.6426 |
| 1 | 7.0099 | 1.6798 | 22.0846 | 12.7245 |
| 2 | 6.8000 | 1.6300 | 24.0559 | 12.1208 |
| 4 | 6.6401 | 1.6151 | 26.0641 | 12.1137 |
| 6 | 6.6120 | 1.6043 | 27.5431 | 12.3882 |
| 8 | 6.5980 | 1.6484 | 28.8137 | 12.2289 |
| 10 | 6.5280 | 1.6060 | 29.2661 | 12.1542 |

The lowest gain factor of 0.001 presents the most efficient case for the mean, M, of *ACP* factors, but the least efficient case for mean of bits. The reason for this is because there is only a slight increase of the availability of quantisation noise of the ADC, corresponding to a necessarily higher dynamic range of the ADC. On the other hand the mean of the *ACP* is lower as it has only been adjusted by a very small gain. A gain factor of $G_k = 10$, presents the most efficient case for the mean of the ADC resolution, but the least efficient case for the mean of the filter *ACP* factors. This case is the opposite of the first case, when $G_k = 0.001$, as the ADC requires lower dynamic range whereas the filter needs a greater *ACP* factor to take the edge off the ACI. A $G_k = 0.001$ is suitable as it makes the filter efficient but the ADC not efficient as the mean resolution is significantly high and reconfigurable approach has no advantage. On the other hand, when $G_k = 10$, the ADC benefits from the reconfigurable approach, as the resolution is low, but the filter in this case has no benefit.

The standard deviation of the *ACP* factors and the ADC resolution does not vary significantly as expected. The gain factor $G_k$ should only have dramatic effects in the means due to the fact that the *ACP* factors are scaled by a gain. A 0.5289 dB variation in

the standard deviation for the *ACP* factors has been recorded and 10% variation in the ADC resolution.

A suitable gain factor which provides a good balance between the efficiency of the ADC and filter where the mean resolution is 6.8-bits and the mean *ACP* factor is 12.1208 is a $G_k$ value of 2. Gain factors between 0.001 and 2 also decrease the mean of the ADC resolution by 40%, which is considered to be a dramatic improvement, whereas the mean is only improved by 4% when gain factors between 2 and 10 are used. Therefore, there is no need to increase $G_k$ beyond a gain factor of 2. It is also essential to note gain factors greater than 2 will result in the same mean in terms of the ADC resolution, concurrently unnecessarily decreasing the efficiency of the filter. Figure 6.12 depicts the statistical analysis of the ADC resolution and filter tap length respectively.

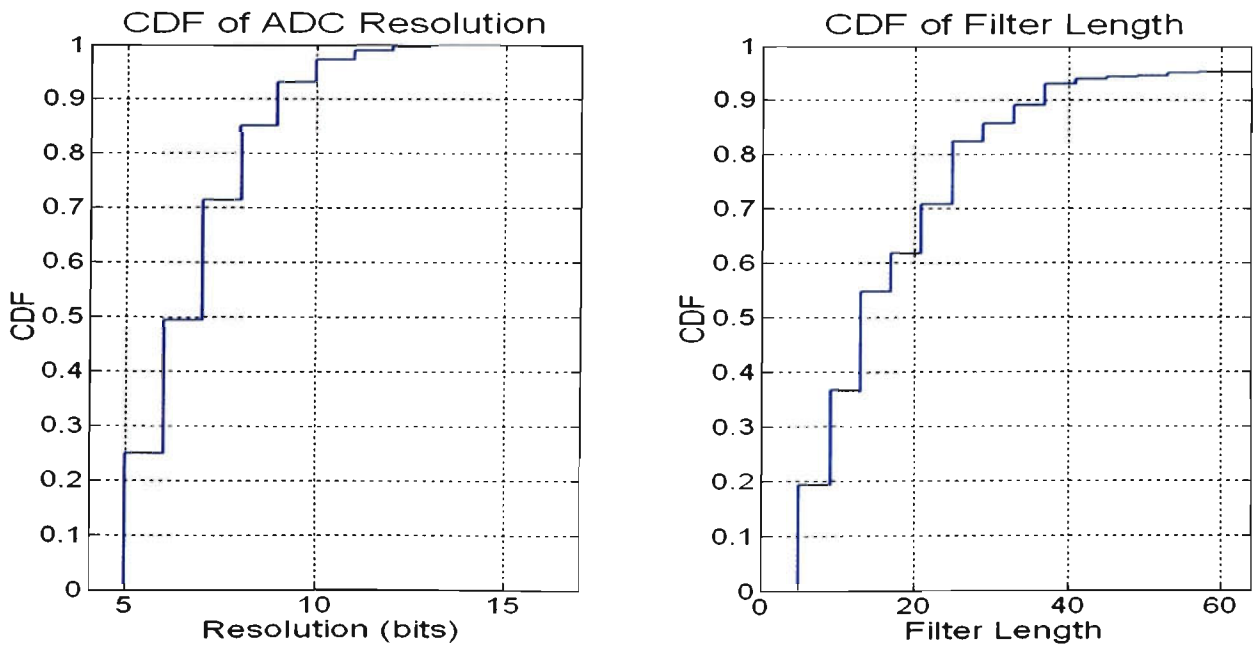



Figure 6.12: Statistical analysis of CRA ($G_k = 2$)

The filter lengths were obtained using the LUT, Table 6.1, and the ADC resolutions were obtained using the LUT, Table 5.1.

The average ADC resolution when compared to the reconfigurable ADC of chapter 5 with a fixed ACP factor is increased by 1 bit to 7-bits. This outcome corresponds to a 56% efficiency savings for the ADC, when compared to a maximum ADC resolution of 16-bits, and a 73% efficiency savings for the filter, compared to the 3GPP specifications. The efficiency will correspond to foremost and essential power consumption savings in both devices, the ADC and filter in the CRA.

## 6.4 Conclusion

In chapter 5, a reconfigurable ADC architecture with a fixed filter length was presented. The effect of scalable filter on the reconfigurable ADC is presented in chapter 6.

A reconfigurable approach to extend battery life in the mobile station by minimising power consumption has resolved cost issues in the receiver ADC. This combined reconfigurable architecture (CRA) monitors the in-band and out-of-band signal powers and intelligently calculates the required *ACP* factor, which in fact corresponds to a certain filter length (taps). The system design led to the proposal of the system structure, which consists of the reconfigurable pipeline ADC architecture in chapter 5, as well as the filter structure. The filter is a pulse-shaping filter with a finite impulse response. The impulse response of the pulse-shaping filter is a root-raised cosine. The system employs this folded FIR structure, and shaves off and adds taps to the ends of the impulse

response to lower or raise the stop band dB level. This is performed by the system control unit. As the mobile receiver deals with a complex signal, it may not be necessary to have the control loop on both in-phase (real) and quadrature (imaginary) signals. It may be sufficient for the in-phase filter to control the tap length for both itself and the quadrature filter. Therefore, the control unit applies only to the in-phase filter. The control unit in the CRA calculates the required dynamic range of the ADC and the corresponding *ACP* factor of the filter, and by employing LUTs it determines how many ADC stages and filter taps need to be turned 'on' or switch 'off', in order to provide the required resolution and ACS respectively.

The efficiency of the ADC and filter have been dramatically affected by various gain factors in search for the ultimate trade off between the two architectures. A gain factor of 2 was found to provide the right balance of efficiency between the ADC and filter. A statistical analysis provided an average ADC resolution of 7-bits and an average filter length of 13. This offers a 56% power savings for the ADC and 73% saving for the filter. These results are for an UTRA-TDD indoor environment in a static simulated domain. The control unit was modified to take into account the safety margin protection, but hysteresis was not considered. Simulations in a dynamic domain, where hysteresis is considered, will not affect the average ADC resolution because the quantisation noise is calculated before the protection takes effect, but it might very well increase the filter length.

# Chapter 7

# *Conclusions & Future Work*

## 7.1 Introduction

During the last decade, wireless communications have been the inspiration behind analog electronics development. By the emergence of new communication standards comes an ever increasing signal bandwidth, allowing more services to be provided. Concurrently, the limits between digital and analog signal processing is impending closer to the antenna, therefore aiming for a software-defined radio solution. In terms of ADCs of mobile terminal receivers, this indicates higher sample rate, lower power consumption and higher resolution.

This chapter presents the final remarks on the major research findings, along with some assumptions used through out the research. The chapter is concluded with some future work ideas for an extension on the present findings.

## 7.2 Major Findings

The objectives of this research together with the corresponding findings are listed below:

- *Design and implementation of a Modified-Flash ADC (Sub-ADC) architectures:*

The Sub-ADC is the most critical component of the pipeline ADC architecture. Making the right choice of which topology to employ is highly dependent on the design application. In this research, power consumption was of greatest concern due to the UTRA-TDD application. The standard flash design can operate at high frequencies, but it consumes large power due to the high design complexity and high device count. Therefore modification to the standard flash design has been carried out in order to compromise between power consumption and speed requirement.

Analysis on the UTRA-TDD system was performed in terms of its dynamic range in order to find out the resolution of the first pipeline block. From the dynamic analysis performed, it was concluded that for an enhancement of 6.02 dB of interference, an additional 1-bit must be added. Therefore, the reconfigurable design consisted of 13 pipeline blocks. The first being a 4-bit block followed by 12 1-bit blocks. The first block of the pipeline ADC, which uses a modified-flash architecture was presented in chapter 4. It requires only $(2^{(N-2)} + 2)$ comparators to implement the modified N-bit flash ADC. This approach greatly reduced the complexity and size of the full flash ADC and the two-step flash ADC. The new ADC architecture dissipates only 1.68 mW of power at 15.36 Ms/s as compared to a full flash ADC of 6.5 mW and a two-step flash of 2.39 mW. Results indicate that a 74% power saving is obtained and 53% of die size could be

saved when the modified flash ADC is used instead of the full flash architecture, as the sub-ADC of the first pipeline chain.

- *Design and implementation of a Pipeline ADC architectures:*

It was found that there are distinct advantages of using the pipeline ADC topology as compared to its counterparts. While the flash ADC architecture can reach very high speed, it consumes a lot of power due to the high device count. The other ADC architectures consume little power, but they operate at very low speeds, which are not appropriate for the UTRA-TDD application, where the 3rd generation system specification of 15.36 Ms/s needs to be met.

However, even though fix word-length pipeline ADC architecture could be suitable for the mobile receiver, it still has a distinct disadvantage when it comes to power consumption. In many cases a fixed word-length ADC is used, say 12-bits, when the receiver requires and uses a converter of only 8-bits. During this time the whole 12-bit device is powered up, which uses a lot more power than it is supposed to. To achieve this, a more complex receiver ADC design and implementation is required, which will have a significant impact on battery life in the mobile terminal.

ADC optimisation techniques could lower power consumption but will not reduce it to its most efficient level. A solution in theory is to use minimum resolution, and still meet the performance requirements of the UTRA-TDD receiver specified by the 3GPP. To achieve this, in-band and out-of-band signal powers were measured. The ADC intelligently choses the amount of resolution required to ensure the out-of-band signal is

below a certain tolerance level and the SNR is still met. This scheme vastly reduced power consumption, as it only utilises the required resolution as compared to traditional fixed complexity architectures.

The translation from theory into reality was obtained by taking advantage of the software radio concept and technologies. Taking advantage of the software radio theory, a solution was achieved using DSP and ASIC technologies that can meet the performance and system needs of high speed and low cost devices.

- *Design and implementation of a Reconfigurable ADC architecture:*

Chapter 5 presented the design and implementation of the reconfigurable pipeline ADC intrinsic to the UTRA-TDD mobile station receiver. The intension of the reconfigurable ADC was to provide a solution to the cost issues associated with the TDD system. The reconfigurable topology in real-time, observes the in-band and out-of-band powers, and by employing an intelligent algorithm, calculates the required resolution and switches the pipeline blocks '*on*' or '*off*' accordingly.

A sampling frequency of 15.36 MHz was used, due to the 3GPP specification, before down sampling the data by a decimation factor of 4. This was performed due to the interpolation factor of 4, which is used in the transmitter. The algorithm formulation for the reconfigurable ADC concluded that three signals are required to determine the appropriate $Q_e$ that gives the overall required resolution. The formulation led to the proposal of the system architecture. It consisted of a number of components; reconfigurable pipeline ADC structure, a RRC filter with a fixed *ACP* value of 33 dB, a

decimation factor of 4 to compromise the interpolation factor within the transmitter, and a signal power measurement components to provide clearly varying amplitudes of each three input signals to the control unit. The control unit calculated the appropriate $Q_n$ values and its corresponding bit values. A LUT was then employed to determine how many blocks of the pipeline chain were required to be switched '*on*' to provide the required resolution.

- *Statistical analysis of the UMTS system:*

A static, statistical analysis on the reconfigurable ADC was also performed and presented in chapter 5, which in fact justified the design of a reconfigurable ADC. ASIC implementation using 0.18μm CMOS technology was performed on the overall reconfigurable ADC. Performance analysis in terms of power consumption and noise was also presented, showing the significant power saving of the reconfigurable ADC in contrast to a fixed 16-bits ADC. A CDF plot of the reconfigurable ADC with a random synchronisation factor indicated that the average resolution of the converter is 6, resulting in 3.92mW of power consumption.

- *Effect of the scalable filter on the reconfigurable ADC architecture: :*

The effect of the scalable RRC filter on the reconfigurable ADC architecture inherent to the UTRA-TDD mobile station receiver was presented in chapter 6. The analysis of this architecture was an extension of the reconfigurable ADC presented and analysed in chapter 5 to see the effect of the RRC filter on the ADC and cater for power efficiency in the digital filter. A reconfigurable approach to extend battery life in the mobile station by minimising power consumption had resolved cost issues in the receiver ADC.

This CRA monitored the in-band and out-of-band signal powers and intelligently calculates the required *ACP* factor, which in fact corresponds to a certain filter length (taps). The system design led to the proposal of the system structure, which consists of the reconfigurable pipeline ADC and filter architecture.

The efficiency of the ADC with a scalable filter was dramatically affected by various gain factors in search for the ultimate trade off between the two architectures. A gain factor of 2 was found to provide the right balance of efficiency between the ADC and filter. A statistical analysis provided an average ADC resolution of 7-bits and an average filter length of 13. This offers a 56% power savings for the ADC and 73% saving for the filter. These results were for an UTRA-TDD indoor environment in a static simulated domain. The control unit was modified to take care of the safety margin protection, but hysteresis was not considered. Simulations in a dynamic domain, where hysteresis is considered, did not affect the average ADC resolution because the quantisation noise is calculated before the protection takes effect. However, the CRA provides a proficient approach to deal with cost concerns intrinsic to the UTRA-TDD mobile station receiver.

## 7.3 Assumptions

The statistical results presented in this thesis are based on computer simulations in MATLAB. Therefore, they are limited with a set of assumptions. The analysis was based on static simulations, which provided a good insight into the UTRA-TDD system with respect to the sensitivity and how certain system parameters affect the analysis. The performance of UTRA-TDD is greatly dependant on a certain set of parameters

such as *Eb/No* targets, cell structure and cluster geometry, processing gain and thermal noise. Varying these parameters will accordingly vary the results of the analysis especially if the *Eb/No* is changed.

Handover was also not assumed in the simulations where handover might improve the statistical analysis results. In addition, the same bit rate for each user was assumed. In practice, a time slot can be fully loaded by one user with high data rates. This case also improves the results as intra-cell interference will not be severe. The analysis was limited to one downlink time slot and only considered the +5 MHz adjacent channel. Considering other adjacent channels (-5 MHz and ±10 MHz) will have an impact on the results. It can be said that the results in the analysis are based on certain parameters and do not apply to all scenarios. Nevertheless, a good insight is provided with a static statistical analysis.

## 7.4 Future Work

Wireless transmission is weakened by signal fading and interference. The increasing requirements on data rate and quality of service for wireless communications systems call for new techniques to increase spectrum efficiency and to improve link reliability. The analysis in this thesis used a single-input single-output antenna, to present the reconfigurable phenomenon. The use of multiple antennas at both ends of a wireless link promises significant improvements in terms of spectral efficiency and link reliability. This technology is known as multiple-input multiple-output (MIMO) wireless system, and is illustrated in Figure 7.1.

It would be an interesting task to employ this reconfigurability to the MIMO system, where the SNR of the system would be at a more accurate level as compared to the single-input single-output scenario.

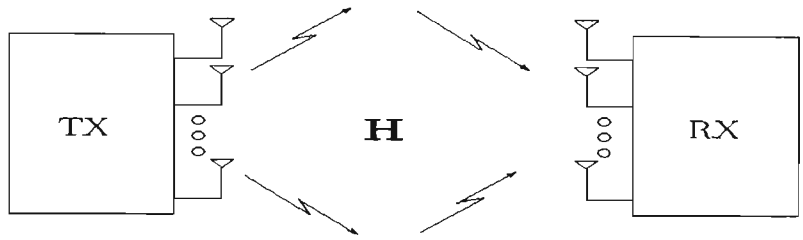



Figure 7.1: Schematic representation of a MIMO wireless system

Employing handover within the system will also improve the statistical analysis results. Handover is the mechanism that transfers an ongoing call from one cell to another as a user travels through the coverage area of a cellular system. As smaller cells are developed to meet the demands for an increased capacity, the number of cell boundary crossing increases. Each handover requires network resources to re-route the call to a new base station. Minimising an expected number of handovers decreases the switching load. The design of reliable handover algorithm is critical to the operation of a cellular communications system and especially important in micro-cellular systems where the mobile receiver may traverse several cells during a call. The improvement to the statistical results in the UTRA-TDD scenario will happen as there is less adjacent mobiles within the cell of interest, there will be less transmission power, therefore less interference. As it has been presented in this thesis, if the interference is low, then the ADC resolution is low. If handover is not present, as the case in this thesis, there is more transmission power from base station to mobile, therefore more interference to the receiver.

Another interesting scenario worth while investigating in order to reduce power besides tuning the resolution of the proposed architecture is to employ voltage scaling. Some of the components within the system do not require the full scale voltage of 2.5 volts to do their required operation, they may only need 1.5 volts or 2 volts to operate, therefore DC-DC converters could be used to scale the voltage down and/or up. Obviously power consumption is proportional to the supply voltage, therefore components operating at lower supply voltages will have less power consumption, resulting in reduction of power and longer battery life of the mobile terminal.

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# Appendix A

# *Spreading & Modulation in TDD*

This documentation is taken directly from the 3rd Generation Partnership Project (3GPP), technical specification group radio access network, 3G TS 25.223, V3.3.0. This document describes multiplexing, channel coding and interleaving for UTRA Physical Layer TDD mode.

## A.1 General Information

In the following, a separation between the data modulation and the spreading modulation has been made. The data modulation is defined in section A.2 and the spreading modulation in section A.3.

Table A.1: Basic modulation parameters

| Chip rate | Basic chiprate: 3.84 Mchip/s | Low chiprate: 1.28 Mchip/s |
|---|---|---|
| Data modulation | QPSK | QPSK |
| Spreading characteristics | Orthogonal Q chips/symbol, where $Q = 2^p$, $0 <= p <= 4$ | Orthogonal Q chips/symbol, where $Q = 2^p$, $0 <= p <= 4$ |

# A.2 Data modulation

## A.2.1 Symbol rate

The symbol duration $T_S$ depends on the spreading factor Q and the chip duration $T_C$:

$$T_s = Q \times T_c, \text{ where } T_c = \frac{1}{chiprate}.$$

## A.2.2 Mapping of bits onto signal point constellation

### A.2.2.1 Mapping for burst type 1 and 2

The data modulation is performed to the bits from the output of the physical channel mapping procedure and combines always 2 consecutive binary bits to a complex valued data symbol. Each user burst has two data carrying parts, termed data blocks:

$$\underline{\mathbf{d}}^{(k,i)} = (\underline{d}_1^{(k,i)}, \underline{d}_2^{(k,i)}, \ldots, \underline{d}_{N_k}^{(k,i)})^T \quad i = 1, 2; k = 1, \ldots, K. \tag{A.1}$$

$N_k$ is the number of symbols per data field for the user k. This number is linked to the spreading factor $Q_k$ as described in table A.1. Data block $\underline{\mathbf{d}}^{(k,1)}$ is transmitted before the midamble and data block $\underline{\mathbf{d}}^{(k,2)}$ after the midamble. Each of the $N_k$ data symbols $\underline{d}_n^{(k,i)}$; i=1, 2; k=1,...,K; n=1,...,$N_k$; of equation 1 has the symbol duration $T_s^{(k)}=Q_k.T_c$ as already given.

The data modulation is QPSK, thus the data symbols $\underline{d}_n^{(k,i)}$ are generated from two consecutive data bits from the output of the physical channel mapping procedure in [8]:

$$b_{l,n}^{(k,i)} \in \{0,1\} \qquad l = 1,2;\ k = 1,\ldots K;\ n = 1,\ldots,N_k;\ i = 1,2 \tag{A.2}$$

Using the following mapping to complex symbols:

Table A.2: Mapping to Complex Symbols

| consecutive binary bit pattern $b_{l,n}^{(k,i)}\ b_{2,n}^{(k,i)}$ | complex symbol $\underline{d}_n^{(k,i)}$ |
|---|---|
| 00 | +j |
| 01 | +1 |
| 10 | -1 |
| 11 | -j |

The mapping corresponds to a QPSK modulation of the interleaved and encoded data bits $b_{l,n}^{(k,i)}$ of equation 0.

### A.2.2.2 Mapping for PRACH burst type

In case of PRACH burst type, the definitions in subclause 5.2.1 apply with a modified number of symbols in the second data block. For the PRACH burst type, the number of symbols in the second data block $\underline{\mathbf{d}}^{(k,2)}$ is decreased by $\frac{96}{Q_K}$ symbols.

# A.3 Spreading modulation

## A.3.1 Basic spreading parameters

Spreading of data consists of two operations: Channelisation and Scrambling. Firstly, each complex valued data symbol $\underline{d}_n^{(k,i)}$ of equation 1 is spread with a real valued channelisation code $\mathbf{c}^{(k)}$ of length $Q_k \in \{1,2,4,8,16\}$. The resulting sequence is then scrambled by a complex sequence $\underline{\mathbf{v}}$ of length 16.

## A.3.2 Channelisation codes

The elements $c_q^{(k)}$; k=1,...,K; q=1,...,$Q_k$; of the real valued channelisation codes

$$\mathbf{c}^{(k)}=(c_1^{(k)},c_2^{(k)},...,c_{Q_k}^{(k)}) \quad ; \quad k=1,...,K;$$

shall be taken from the set

$$V_c = \{1,-1\} \tag{A.3}$$

The $\mathbf{c}_{Q_k}^{(k)}$ are Orthogonal Variable Spreading Factor (OVSF) codes, allowing to mix in the same timeslot channels with different spreading factors while preserving the orthogonality. The OVSF codes can be defined using the code tree of Figure A.1.

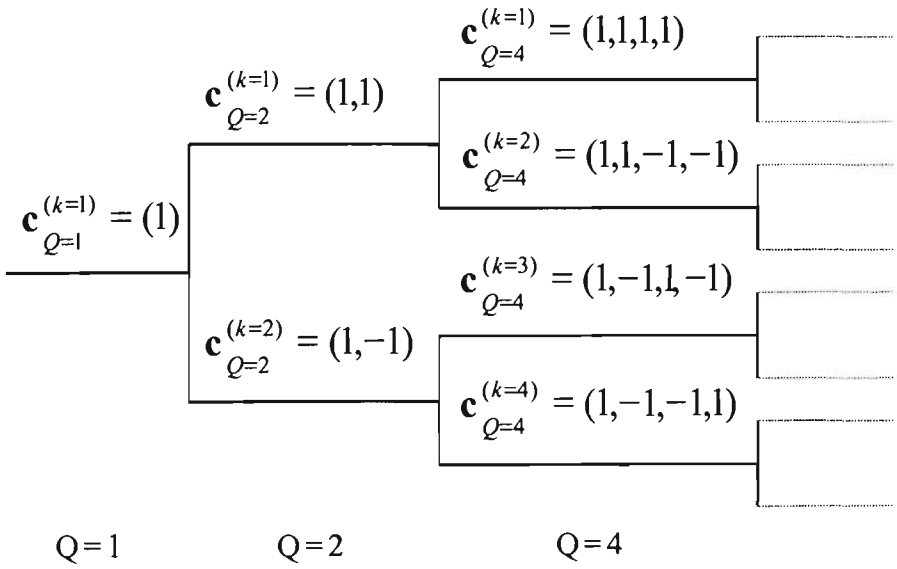


Figure A.1: Code-tree for generation of Orthogonal Variable Spreading Factor (OVSF) codes for Channelisation Operation

Each level in the code tree defines a spreading factor indicated by the value of Q in the figure. All codes within the code tree cannot be used simultaneously in a given timeslot. A code can be used in a timeslot if and only if no other code on the path from the specific code to the root of the tree or in the sub-tree below the specific code is used in

this timeslot. This means that the number of available codes in a slot is not fixed but depends on the rate and spreading factor of each physical channel. The spreading factor goes up to $Q_{MAX}$=16.

### A.3.3 Scrambling codes

The spreading of data by a real valued channelisation code $\mathbf{c}^{(k)}$ of length $Q_k$ is followed by a cell specific complex scrambling sequence $\underline{\mathbf{v}} = (\underline{v}_1, \underline{v}_2, \ldots, \underline{v}_{16})$. The elements $\underline{v}_i; i = 1,\ldots,16$ of the complex valued scrambling codes shall be taken from the complex set:

$$\underline{V}_{\underline{v}} = \{1, j, -1, -j\} \tag{A.4}$$

The scheme is illustrated in Figure A.2 below and is described in more detail in section A.3.4.

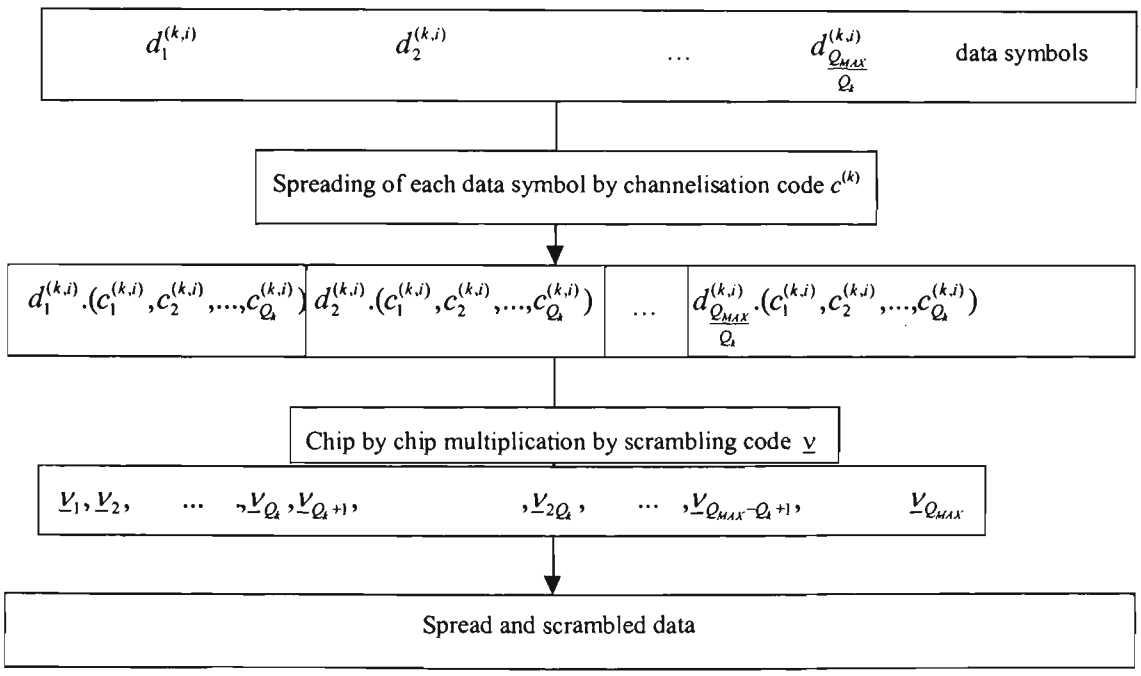


Figure A.2: Spreading of data symbols

In Equation A.4 the letter j denotes the imaginary unit. A complex scrambling code $\underline{\mathbf{v}}$ is generated from the binary scrambling codes $\mathbf{v} = (v_1, v_2, \ldots, v_{16})$ of length 16 shown in Annex A. The relation between the elements $\underline{\mathbf{v}}$ and $\mathbf{v}$ is given by:

$$\underline{v}_i = (j)^i \cdot v_i \qquad v_i \in \{1, -1\}, \; i = 1, \ldots, 16 \tag{A.5}$$

Hence, the elements $\underline{v}_i$ of the complex scrambling code $\underline{\mathbf{v}}$ are alternating real and imaginary. The length matching is obtained by concatenating $Q_{MAX}/Q_k$ spread words before the scrambling.

## A.3.4 Spread signal of data symbols and data blocks

The combination of the user specific channelisation and cell specific scrambling codes can be seen as a user and cell specific spreading code $\mathbf{s}^{(k)} = (s_p^{(k)})$ with

$$s_p^{(k)} = c^{(k)}_{1+[(p-1) \bmod Q_k]} \cdot \underline{v}_{1+[(p-1) \bmod Q_{MAX}]}, \; k=1,\ldots,K, \; p=1,\ldots,N_k Q_k.$$

With the root raised cosine chip impulse filter $Cr_0(t)$ the transmitted signal belonging to the data block $\underline{\mathbf{d}}^{(k,1)}$ of equation 1 transmitted before the midamble is

$$\underline{d}^{(k,1)}(t) = \sum_{n=1}^{N_k} \underline{d}_n^{(k,1)} \sum_{q=1}^{Q_k} s^{(k)}_{(n-1)Q_k+q} \cdot Cr_0(t - (q-1)T_c - (n-1)Q_k T_c) \tag{A.6}$$

and for the data block $\underline{\mathbf{d}}^{(k,2)}$ of equation 1 transmitted after the midamble

$$\underline{d}^{(k,2)}(t) = \sum_{n=1}^{N_k} \underline{d}_n^{(k,2)} \sum_{q=1}^{Q_k} s^{(k)}_{(n-1)Q_k+q} \cdot Cr_0(t - (q-1)T_C - (n-1)Q_k T_c - N_k Q_k T_c - L_m T_c). \tag{A.7}$$

where $L_m$ is the number of midamble chips.

### A.3.5 Modulation

The complex-valued chip sequence is QPSK modulated as shown in Figure A.3 below.

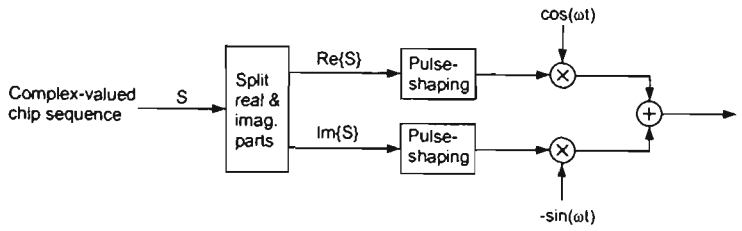


Figure A.3: Modulation of complex valued chip sequences

## A.4 Synchronisation codes

### A.4.1 Code Generation

The Primary code sequence, $C_p$ is constructed as a so-called generalised hierarchical Golay sequence. The Primary SCH is furthermore chosen to have good aperiodic auto correlation properties.

Define $a = < x_1, x_2, x_3, \ldots, x_{16} > = < 1, 1, 1, 1, 1, 1, -1, -1, 1, -1, 1, -1, 1, -1, -1, 1 >$

The PSC code word is generated by repeating the sequence 'a' modulated by a Golay complementary sequence and creating a complex-valued sequence with identical real and imaginary components.

The PSC code word $C_p$ is defined as $C_p = < y(0), y(1), y(2), \ldots, y(255) >$

where $y = (1 + j) \times < a, a, a, -a, -a, a, -a, -a, a, a, a, -a, a, -a, a, a >$

and the left most index corresponds to the chip transmitted first in each time slot.

The 16 secondary synchronization code words, $\{C_0, \ldots, C_{15}\}$ are complex valued with identical real and imaginary components, and are constructed from the position wise multiplication of a Hadamard sequence and a sequence z, defined as:

$$z = < b,b,b,-b,b,b,-b,-b,b,-b,b,-b,-b,-b,-b,-b >$$ , where

$$b = < x_1,...,x_8,-x_9,...,-x_{16} > = <1, 1, 1, 1, 1, 1, -1, -1, -1, 1, -1, 1, -1, 1, 1, -1>.$$

The Hadamard sequences are obtained as the rows in a matrix $H_8$ constructed recursively by:

$$H_0 = (1)$$

$$H_k = \begin{pmatrix} H_{k-1} & H_{k-1} \\ H_{k-1} & -H_{k-1} \end{pmatrix}, \quad k \geq 1$$

The rows are numbered from the top starting with row *0* (the all zeros sequence).

Denote the *n*:th Hadamard sequence as a row of $H_8$ numbered from the top, n = 0, 1, 2, ..., 255, in the sequel.

Furthermore, let $h_m(i)$ and $z(i)$ denote the *i*:th symbol of the sequence $h_m$ and $z$, respectively where $i$ = 0, 1, 2, ..., 255 and $i$ = 0 corresponds to the leftmost symbol.

The i:th SCH code word, $C_{SCH,i}$, i = 0, ..., 15 is then defined as:

$$C_{SCH,i} = (1 + j) \times <h_m(0) \times z(0), h_m(1) \times z(1), h_m(2) \times z(2), ..., h_m(255) \times z(255)>,$$

where $m$ = (16×i) and the leftmost chip in the sequence corresponds to the chip transmitted first in time. This code word is chosen from every 16th row of the matrix $H_8$., which yields 16 possible codewords.

The Secondary SCH code words are defined in terms of $C_{SCH,i}$ and the definition of $\{C_0,...,C_{15}\}$ now follows as:

$$C_i = C_{SCH,i}, \quad i=0,...,15$$

## A.4.2 Code Allocation

Three SCH codes are QPSK modulated and transmitted in parallel with the primary synchronization code. The QPSK modulation carries the following information:

- the code group that the base station belongs to (5 bits; Cases 1, 2);
- the position of the frame within an interleaving period of 20msec (1 bit, Cases 1, 2);
- the position of the slot within the frame (1 bit, Case 2).

The modulated codes are also constructed such that their cyclic-shifts are unique, i.e. a non-zero cyclic shift less than 2 (Case 1) and 4 (Case 2) of any of the sequences is not equivalent to some cyclic shift of any other of the sequences. Also, a non-zero cyclic shift less than 2 (Case 1) and 4 (Case 2) of any of the sequences is not equivalent to itself with any other cyclic shift less than 8. The secondary synchronization codes are partitioned into two code sets for Case 1 and four code sets for Case 2. The set is used to provide the following information:

Case 1:

Table A.2: Code Set Allocation for Case 1

| Code Set | Code Group |
|---|---|
| 1 | 0-15 |
| 2 | 16-31 |

The code group and frame position information is provided by modulating the secondary codes in the code set.

Case 2:

Table A.4: Code Set Allocation for Case 2

| Code Set | Code Group |
|---|---|
| 1 | 0-7 |
| 2 | 8-15 |
| 3 | 16-23 |
| 4 | 24-31 |

The slot timing and frame position information is provided by the comma free property of the code word and the Code group is provided by modulating some of the secondary codes in the code set.

The following SCH codes are allocated for each code set:

Case 1

Code set 1: $C_0$, $C_1$, $C_2$.

Code set 2: $C_3$, $C_4$, $C_5$.

Case 2

Code set 1: $C_0$, $C_1$, $C_2$.

Code set 2: $C_3$, $C_4$, $C_5$.

Code set 3: $C_6$, $C_7$, $C_8$.

Code set 4: $C_9$, $C_{10}$, $C_{11}$.

The following subclauses 7.2.1 to 7.2.2 refer to the two cases of SCH/P-CCPCH usage as described in [7]. Note that in the Tables A.5 – A.7 corresponding to Cases 1, 2, and 3, respectively, Frame 1 implies the frame with an odd SFN and Frame 2 implies the frame with an even SFN.

### A.4.2.1 Code allocation for Case 1

NOTE: Modulation by "j" indicates that the code is transmitted on the Q channel.

Table A.5: Code Allocation for Case 1

| Code Group | Code Set | Frame 1 | | | Frame 2 | | | Associated $t_{offset}$ |
|---|---|---|---|---|---|---|---|---|
| 0 | 1 | $C_0$ | $C_1$ | $C_2$ | $C_0$ | $C_1$ | $-C_2$ | $t_0$ |
| 1 | 1 | $C_0$ | $-C_1$ | $C_2$ | $C_0$ | $-C_1$ | $-C_2$ | $t_1$ |
| 2 | 1 | $-C_0$ | $C_1$ | $C_2$ | $-C_0$ | $C_1$ | $-C_2$ | $t_2$ |
| 3 | 1 | $-C_0$ | $-C_1$ | $C_2$ | $-C_0$ | $-C_1$ | $-C_2$ | $t_3$ |
| 4 | 1 | $jC_0$ | $JC_1$ | $C_2$ | $jC_0$ | $jC_1$ | $-C_2$ | $t_4$ |
| 5 | 1 | $jC_0$ | $-jC_1$ | $C_2$ | $jC_0$ | $-jC_1$ | $-C_2$ | $t_5$ |
| 6 | 1 | $-jC_0$ | $JC_1$ | $C_2$ | $-jC_0$ | $jC_1$ | $-C_2$ | $t_6$ |
| 7 | 1 | $-jC_0$ | $-jC_1$ | $C_2$ | $-jC_0$ | $-jC_1$ | $-C_2$ | $t_7$ |
| 8 | 1 | $jC_0$ | $JC_2$ | $C_1$ | $jC_0$ | $jC_2$ | $-C_1$ | $t_8$ |
| 9 | 1 | $jC_0$ | $-jC_2$ | $C_1$ | $jC_0$ | $-jC_2$ | $-C_1$ | $t_9$ |
| 10 | 1 | $-jC_0$ | $JC_2$ | $C_1$ | $-jC_0$ | $jC_2$ | $-C_1$ | $t_{10}$ |
| 11 | 1 | $-jC_0$ | $-jC_2$ | $C_1$ | $-jC_0$ | $-jC_2$ | $-C_1$ | $t_{11}$ |
| 12 | 1 | $jC_1$ | $JC_2$ | $C_0$ | $JC_1$ | $jC_2$ | $-C_0$ | $t_{12}$ |
| 13 | 1 | $jC_1$ | $-jC_2$ | $C_0$ | $JC_1$ | $-jC_2$ | $-C_0$ | $t_{13}$ |
| 14 | 1 | $-jC_1$ | $JC_2$ | $C_0$ | $-jC_1$ | $jC_2$ | $-C_0$ | $t_{14}$ |
| 15 | 1 | $-jC_1$ | $-jC_2$ | $C_0$ | $-jC_1$ | $-jC_2$ | $-C_0$ | $t_{15}$ |
| 16 | 2 | $C_3$ | $C_4$ | $C_5$ | $C_3$ | $C_4$ | $-C_5$ | $t_{16}$ |
| 17 | 2 | $C_3$ | $-C_4$ | $C_5$ | $C_3$ | $-C_4$ | $-C_5$ | $t_{17}$ |
| ... | ... | ... | ... | ... | ... | ... | ... | ... |
| 20 | 2 | $jC_3$ | $JC_4$ | $C_5$ | $jC_3$ | $jC_4$ | $-C_5$ | $t_{20}$ |
| ... | ... | ... | ... | ... | ... | ... | ... | ... |
| 24 | 2 | $jC_3$ | $jC_5$ | $C_4$ | $jC_3$ | $JC_5$ | $-C_4$ | $t_{24}$ |
| ... | ... | ... | ... | ... | ... | ... | ... | ... |
| 31 | 2 | $-jC_4$ | $-jC_5$ | $C_3$ | $-jC_4$ | $-jC_5$ | $-C_3$ | $t_{31}$ |

NOTE: The code construction for code groups 0 to 15 using only the SCH codes from code set 1 is shown. The construction for code groups 16 to 31 using the SCH codes from code set 2 is done in the same way.

### A.4.2.2 Code allocation for Case 2

Table A.6: Code Allocation for Case 2

| Code Group | Set | Frame 1 | | | | | | Frame 2 | | | | | | Associated $t_{offset}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Slot k | | | Slot k+8 | | | Slot k | | | Slot k+8 | | | |
| 0 | 1 | $C_0$ | $C_1$ | $C_2$ | $C_0$ | $C_1$ | $-C_2$ | $-C_0$ | $-C_1$ | $C_2$ | $-C_0$ | $-C_1$ | $-C_2$ | $t_0$ |
| 1 | 1 | $C_0$ | $-C_1$ | $C_2$ | $C_0$ | $-C_1$ | $-C_2$ | $-C_0$ | $C_1$ | $C_2$ | $-C_0$ | $C_1$ | $-C_2$ | $t_1$ |
| 2 | 1 | $jC_0$ | $jC_1$ | $C_2$ | $jC_0$ | $jC_1$ | $-C_2$ | $-jC_0$ | $-jC_1$ | $C_2$ | $-jC_0$ | $-jC_1$ | $-C_2$ | $t_2$ |
| 3 | 1 | $jC_0$ | $-jC_1$ | $C_2$ | $jC_0$ | $-jC_1$ | $-C_2$ | $-jC_0$ | $jC_1$ | $C_2$ | $-jC_0$ | $jC_1$ | $-C_2$ | $t_3$ |
| 4 | 1 | $jC_0$ | $jC_2$ | $C_1$ | $jC_0$ | $jC_2$ | $-C_1$ | $-jC_0$ | $-jC_2$ | $C_1$ | $-jC_0$ | $-jC_2$ | $-C_1$ | $t_4$ |
| 5 | 1 | $jC_0$ | $-jC_2$ | $C_1$ | $jC_0$ | $-jC_2$ | $-C_1$ | $-jC_0$ | $jC_2$ | $C_1$ | $-jC_0$ | $jC_2$ | $-C_1$ | $t_5$ |
| 6 | 1 | $jC_1$ | $jC_2$ | $C_0$ | $jC_1$ | $jC_2$ | $-C_0$ | $-jC_1$ | $-jC_2$ | $C_0$ | $-jC_1$ | $-jC_2$ | $-C_0$ | $t_6$ |
| 7 | 1 | $jC_1$ | $-jC_2$ | $C_0$ | $jC_1$ | $-jC_2$ | $-C_0$ | $-jC_1$ | $jC_2$ | $C_0$ | $-jC_1$ | $jC_2$ | $-C_0$ | $t_7$ |
| 8 | 2 | $C_3$ | $C_4$ | $C_5$ | $C_3$ | $C_4$ | $-C_5$ | $-C_3$ | $-C_4$ | $C_5$ | $-C_3$ | $-C_4$ | $-C_5$ | $t_8$ |
| 9 | 2 | $C_3$ | $-C_4$ | $C_5$ | $C_3$ | $-C_4$ | $-C_5$ | $-C_3$ | $C_4$ | $C_5$ | $-C_3$ | $C_4$ | $-C_5$ | $t_9$ |
| 10 | 2 | $jC_3$ | $jC_4$ | $C_5$ | $jC_3$ | $jC_4$ | $-C_5$ | $-jC_3$ | $-jC_4$ | $C_5$ | $-jC_3$ | $-jC_4$ | $-C_5$ | $t_{10}$ |
| 11 | 2 | $jC_3$ | $-jC_4$ | $C_5$ | $jC_3$ | $-jC_4$ | $-C_5$ | $-jC_3$ | $jC_4$ | $C_5$ | $-jC_3$ | $jC_4$ | $-C_5$ | $t_{11}$ |
| 12 | 2 | $jC_3$ | $jC_5$ | $C_4$ | $jC_3$ | $jC_5$ | $-C_4$ | $-jC_3$ | $-jC_5$ | $C_4$ | $-jC_3$ | $-jC_5$ | $-C_4$ | $t_{12}$ |
| 13 | 2 | $jC_3$ | $-jC_5$ | $C_4$ | $jC_3$ | $-jC_5$ | $-C_4$ | $-jC_3$ | $jC_5$ | $C_4$ | $-jC_3$ | $jC_5$ | $-C_4$ | $t_{13}$ |
| 14 | 2 | $jC_4$ | $jC_5$ | $C_3$ | $jC_4$ | $jC_5$ | $-C_3$ | $-jC_4$ | $-jC_5$ | $C_3$ | $-jC_4$ | $-jC_5$ | $-C_3$ | $t_{14}$ |
| 15 | 2 | $jC_4$ | $-jC_5$ | $C_3$ | $jC_4$ | $-jC_5$ | $-C_3$ | $-jC_4$ | $jC_5$ | $C_3$ | $-jC_4$ | $jC_5$ | $-C_3$ | $t_{15}$ |
| 16 | 3 | $C_6$ | $C_7$ | $C_8$ | $C_6$ | $C_7$ | $-C_8$ | $-C_6$ | $-C_7$ | $C_8$ | $-C_6$ | $-C_7$ | $-C_8$ | $t_{16}$ |
| ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... |
| 23 | 3 | $jC_7$ | $-jC_8$ | $C_6$ | $jC_7$ | $-jC_8$ | $-C_6$ | $-jC_7$ | $jC_8$ | $C_6$ | $-jC_7$ | $jC_8$ | $-C_6$ | $t_{20}$ |
| 24 | 4 | $C_9$ | $C_{10}$ | $C_{11}$ | $C_9$ | $C_{10}$ | $-C_{11}$ | $-C_9$ | $-C_{10}$ | $C_{11}$ | $-C_9$ | $-C_{10}$ | $-C_{11}$ | $t_{24}$ |
| ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... |
| 31 | 4 | $jC_{10}$ | $-jC_{11}$ | $C_9$ | $jC_{10}$ | $-jC_{11}$ | $-C_9$ | $-jC_{10}$ | $jC_{11}$ | $C_9$ | $-jC_{10}$ | $jC_{11}$ | $-C_9$ | $t_{31}$ |

NOTE: The code construction for code groups 0 to 15 using the SCH codes from code sets 1 and 2 is shown. The construction for code groups 16 to 31 using the SCH codes from code sets 3 and 4 is done in the same way.

## A.4.3 Evaluation of synchronisation codes

The evaluation of information transmitted in SCH on code group and frame timing is shown in table 6, where the 32 code groups are listed. Each code group is containing 4 specific scrambling codes (cf. subclause 6.3), each scrambling code associated with a specific short and long basic midamble code.

Each code group is additionally linked to a specific $t_{Offset}$, thus to a specific frame timing. By using this scheme, the UE can derive the position of the frame border due to the position of the SCH sequence and the knowledge of $t_{Offset}$. The complete mapping of Code Group to Scrambling Code, Midamble Codes and $t_{Offset}$ is depicted in Table A.7.

Table A.7: Mapping scheme for Cell Parameters, Code Groups, Scrambling Codes, Midambles and $t_{Offset}$

| CELL PARA-METER | Code Group | Associated Codes | | | Associated $t_{Offset}$ |
|---|---|---|---|---|---|
| | | Scrambling Code | Long Basic Midamble Code | Short Basic Midamble Code | |
| 0 | Group 0 | Code 0 | $m_{PL0}$ | $m_{SL0}$ | $t_0$ |
| 1 | | Code 1 | $m_{PL1}$ | $m_{SL1}$ | |
| 2 | | Code 2 | $m_{PL2}$ | $m_{SL2}$ | |
| 3 | | Code 3 | $m_{PL3}$ | $m_{SL3}$ | |
| 4 | Group 1 | Code 4 | $m_{PL4}$ | $m_{SL4}$ | $t_1$ |
| 5 | | Code 5 | $m_{PL5}$ | $m_{SL5}$ | |
| 6 | | Code 6 | $m_{PL6}$ | $m_{SL6}$ | |
| 7 | | Code 7 | $m_{PL7}$ | $m_{SL7}$ | |
| . . . . | | | | | |
| 124 | Group 31 | Code 124 | $m_{PL124}$ | $m_{SL124}$ | $t_{31}$ |
| 125 | | Code 125 | $m_{PL125}$ | $m_{SL125}$ | |
| 126 | | Code 126 | $m_{PL126}$ | $m_{SL126}$ | |
| 127 | | Code 127 | $m_{PL127}$ | $m_{SL127}$ | |

Each cell shall cycle through two sets of cell parameters in a code group with the cell parameters changing each frame.

Table A.8 shows how the cell parameters are cycled according to the SFN.

Table A.8: Alignment of cell parameter cycling and SFN

| Initial Cell Parameter Assignment | Code Group | Cell Parameter used when SFN mod 2 = 0 | Cell Parameter used when SFN mod 2 = 1 |
|---|---|---|---|
| 0 | Group 1 | 0 | 1 |
| 1 | | 1 | 0 |
| 2 | | 2 | 3 |
| 3 | | 3 | 2 |
| 4 | Group 2 | 4 | 5 |
| 5 | | 5 | 4 |
| 6 | | 6 | 7 |
| 7 | | 7 | 6 |
| | . | | |
| | . | | |
| | . | | |
| 124 | Group 32 | 124 | 125 |
| 125 | | 125 | 124 |
| 126 | | 126 | 127 |
| 127 | | 127 | 126 |

# Appendix B

# *Comparator Noise Analysis*

Prior to the calculation of the total noise present in the dynamic comparator, lets remind our selves about the major noise source in CMOS transistors.

## B.1 Noise in MOS Transistors

The two major noise sources found in CMOS transistors are thermal noise and flicker noise. This section briefly describes these two noise sources.

### B.1.1 Thermal Noise

The occurrence of thermal noise in CMOS transistors is due to the random thermal motion of electrons since the typical electrons drift velocities in a conductor are much less than electron thermal noise. This is independent of frequency and is given by:

$$i_i^2 = 4kT \cdot \left(\frac{2gm}{3}\right) \cdot \Delta f \qquad \text{(B.1)}$$

where $gm$ is the MOS transconductance and $\Delta f$ is the bandwidth in Hz.

## B.1.2 Flicker Noise

The flicker noise in a transistor is caused by traps associated with contamination and crystal defects. This noise is inversely proportional to the frequency and is given by:

$$\overline{i_i^2} = K \cdot \left( \frac{I_D{}^a}{f} \right) \cdot \Delta f \tag{B.2}$$

where $I_D$ is the drain current, $K$ is a constant for a particular device, $\Delta f$ is the bandwidth in Hz, and $a$ is a constant in the ranges of 0.5 → 2. One of the most popular noise models of MOS transistors was shown in Figure 4.7 and is used in this thesis for noise calculations. In this model, all the noise sources from each transistor are lumped into an equivalent input noise generator. The model is given by:

$$\overline{V_i^2} = \frac{8kT}{3g_m}\Delta f + K\frac{I_D{}^a}{f}\Delta f \tag{B.3}$$

The flicker noise component is approximately independent of bias current and voltage. For typical MOS transistor, flicker noise is inversely proportional to the active gate area of the transistor, and it is also inversely proportional to the gate-oxide capacitance per unit area. The noise generator for MOS transistor, thus, can be expressed as follows:

$$\overline{V_i^2} = \frac{8kT}{3g_m}\Delta f + \frac{K_f}{WLC_{ox}f}\Delta f \tag{B.4}$$

where $W$ and $L$ are the width and length of a MOS transistor, respectively, $C_{ox}$ is the oxide capacitance, $g_m$ is the MOS transconductance, $k$ is the Boltzman's constant, $T$ is the operation temperature, and $f$ is the operating frequency.

The noise analysis of the proposed comparator in Figure 3.27 will be analysed in two sections. The first section will be the noise of the latch circuit, and the second section will contain the noise of the S-R latch circuit.

## B.2 Comparator Noise Analysis

### B.2.1 CMOS Latch Noise Analysis

By equating all the output noise current from each transistor in Figure 3.27, the equivalent input noise voltage can be given by:

$$\begin{aligned}\overline{V_{latch}^{\,2}} = &\left(\frac{gm_0}{gm_1}\right)^2 \cdot \overline{V_{i0}^{\,2}} + \overline{V_{i1}^{\,2}} + \overline{V_{i2}^{\,2}} + \left(\frac{gm_3}{gm_1}\right)^2 \cdot \overline{V_{i3}^{\,2}} + \left(\frac{gm_4}{gm_1}\right)^2 \cdot \overline{V_{i4}^{\,2}} \\ &+ \left(\frac{gm_{10}}{gm_1}\right)^2 \cdot \overline{V_{i10}^{\,2}} + \left(\frac{gm_{12}}{gm_1}\right)^2 \cdot \overline{V_{i12}^{\,2}} + \left(\frac{gm_{11}}{gm_1}\right)^2 \cdot \overline{V_{i11}^{\,2}} + \left(\frac{gm_{11}}{gm_1}\right)^2 \cdot \overline{V_{i11}^{\,2}}\end{aligned} \tag{B.5}$$

The two branches of the latch circuit are identical, therefore Equation B.5 can be simplified to:

$$\overline{V_{latch}^{\,2}} = \left(\frac{gm_0}{gm_1}\right)^2 \cdot \overline{V_{i0}^{\,2}} + \overline{2 \cdot V_{i1}^{\,2}} + 2 \cdot \left(\frac{gm_3}{gm_1}\right)^2 \cdot \overline{V_{i3}^{\,2}} + 2 \cdot \left(\frac{gm_{10}}{gm_1}\right)^2 \cdot \overline{V_{i10}^{\,2}} + 2 \cdot \left(\frac{gm_{11}}{gm_1}\right)^2 \cdot \overline{V_{i11}^{\,2}} \tag{B.6}$$

Since the thermal noise and flicker noise are independent of each, they can be considered separately. Therefore the input noise voltage of the latch circuit can be expressed by:

$$\overline{V_{latch}^{\ 2}} = \overline{V_{thermal}^{\ 2}} + \overline{V_{flicker}^{\ 2}} \tag{B.7}$$

### B.2.1.1 Thermal Noise of Latch Circuit

The thermal noise model of each transistor is:

$$\overline{V_i^2} = \left(\frac{8 \cdot k \cdot T}{3 \cdot gm}\right) \cdot \Delta f \tag{B.8}$$

Using Equation B.6 and Equation B.8, the equivalent thermal noise for the latch circuit can be expressed as:

$$\overline{V_{thermal}^{\ 2}} = \left(\frac{16 \cdot k \cdot T}{3 \cdot gm_1}\right) \cdot \left(1 + \sqrt{\frac{1}{2} \cdot \frac{\left(\frac{W}{L}\right)_0}{\left(\frac{W}{L}\right)_1}} + \sqrt{\frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_1}} + \sqrt{\frac{1}{2} \cdot \frac{\mu_n \cdot \left(\frac{W}{L}\right)_{10}}{\mu_p \cdot \left(\frac{W}{L}\right)_1}} + \sqrt{\frac{1}{2} \cdot \frac{\mu_n \cdot \left(\frac{W}{L}\right)_{11}}{\mu_p \cdot \left(\frac{W}{L}\right)_1}}\right) \cdot \Delta f \tag{B.9}$$

### B.2.1.2 Flicker Noise of Latch Circuit

One of the most widely used flicker noise model for each transistor is:

$$\overline{V_i^2} + \left(\frac{K_f}{W \cdot L \cdot f \cdot C_{ox}}\right) \cdot \Delta f \tag{B.10}$$

Solving Equation B.6 and Equation B.8, the equivalent flicker noise for the latch circuit can be expressed by:

$$\overline{V_{flicker}^{\ 2}} = \left(\frac{2 \cdot K_p}{W_1 \cdot L_1 \cdot C_{ox}}\right) \cdot \left(1 + \frac{L_1^{\ 2}}{L_0^{\ 2}} + \frac{L_1^{\ 2}}{L_3^{\ 2}} + \frac{1}{2} \cdot \frac{\mu_n \cdot K_n \cdot L_1^{\ 2}}{\mu_p \cdot K_p \cdot L_{10}^{\ 2}} + \frac{1}{2} \cdot \frac{\mu_n \cdot K_n \cdot L_1^{\ 2}}{\mu_p \cdot K_p \cdot L_{11}^{\ 2}}\right) \cdot \Delta f \quad \text{(B.11)}$$

Substituting Equation B.9 and Equation B.11 into Equation B.7, the equivalent noise generator for the latch circuit of the dynamic comparator could be expressed by:

$$\begin{aligned}\overline{V_{latch}^{\ 2}} = &\left(\frac{16 \cdot k \cdot T}{3 \cdot gm_1}\right) \cdot \left(1 + \sqrt{\frac{1}{2} \cdot \frac{\left(\frac{W}{L}\right)_0}{\left(\frac{W}{L}\right)_1}} + \sqrt{\frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_1}} + \sqrt{\frac{1}{2} \cdot \frac{\mu_n \cdot \left(\frac{W}{L}\right)_{10}}{\mu_p \cdot \left(\frac{W}{L}\right)_1}} + \sqrt{\frac{1}{2} \cdot \frac{\mu_n \cdot \left(\frac{W}{L}\right)_{11}}{\mu_p \cdot \left(\frac{W}{L}\right)_1}}\right) \cdot \Delta f \\ &+ \left(\frac{2 \cdot K_p}{W_1 \cdot L_1 \cdot C_{ox}}\right) \cdot \left(1 + \frac{L_1^{\ 2}}{L_0^{\ 2}} + \frac{L_1^{\ 2}}{L_3^{\ 2}} + \frac{1}{2} \cdot \frac{\mu_n \cdot K_n \cdot L_1^{\ 2}}{\mu_p \cdot K_p \cdot L_{10}^{\ 2}} + \frac{1}{2} \cdot \frac{\mu_n \cdot K_n \cdot L_1^{\ 2}}{\mu_p \cdot K_p \cdot L_{11}^{\ 2}}\right) \cdot \Delta f\end{aligned} \quad \text{(B.12)}$$

### B.2.1.3 Noise Figure of Latch Circuit

The noise figure is a measure that specifies the noise performance of a certain circuit. This measure can be defined as:

$$NF = \frac{Total\ Output\ Noise}{That\ Part\ of\ Noise\ due\ to\ source\ resis\tan ce} = 1 + \frac{V_{latch}^{\ 2}}{4 \cdot k \cdot T \cdot R_s \cdot \Delta f} \quad \text{(B.13)}$$

By substituting Equation B.12 into Equation B.13, the noise figure of the latch circuit within the comparator could be obtained. This is given by:

$$NF_{latch} = 1 + \frac{K_p}{2kTR_s fW_1 L_1 C_{ox}} \cdot \left( 1 + \frac{L_1^2}{L_0^2} + \frac{L_1^2}{L_3^2} + \frac{1}{2} \cdot \frac{\mu_n \cdot K_n \cdot L_1^2}{\mu_p \cdot K_p \cdot L_{10}^2} + \frac{1}{2} \cdot \frac{\mu_n \cdot K_n \cdot L_1^2}{\mu_p \cdot K_p \cdot L_{11}^2} \right)$$
$$+ \frac{4}{3R_s gm_1} \cdot \left( 1 + \sqrt{\frac{1}{2} \cdot \frac{\left(\frac{W}{L}\right)_0}{\left(\frac{W}{L}\right)_1}} + \sqrt{\frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_1}} + \sqrt{\frac{1}{2} \cdot \frac{\mu_n \cdot \left(\frac{W}{L}\right)_{10}}{\mu_p \cdot \left(\frac{W}{L}\right)_1}} + \sqrt{\frac{1}{2} \cdot \frac{\mu_n \cdot \left(\frac{W}{L}\right)_{11}}{\mu_p \cdot \left(\frac{W}{L}\right)_1}} \right) \quad \text{(B.14)}$$

## B.2.2 S-R Latch Noise Analysis

In a similar manner as the noise analysis of the CMOS latch within the proposed comparator in Figure 3.27, the S-R latch noise analysis is performed. Both branches of the S-R are identical, therefore by equating the output noise currents, the equivalent input noise voltage of the S-R latch can be calculated, and is given by:

$$\overline{V_{S-R}^2} = 2 \cdot \left( \frac{gm_5}{gm_5 + gm_{13}} \right)^2 \cdot V_{i5}^2 + 2 \cdot \left( \frac{gm_7}{gm_5 + gm_{13}} \right)^2 \cdot V_{i7}^2 + 2 \cdot \left( \frac{gm_{13}}{gm_5 + gm_{13}} \right)^2 \cdot V_{i13}^2 + 2 \cdot \left( \frac{gm_{14}}{gm_5 + gm_{13}} \right)^2 \cdot V_{i14}^2 \quad \text{(B.15)}$$

Due to the fact that the NMOS and PMOS transistors of the S-R latch have equal width and length dimensions, Equation B.15 can be reduced to:

$$\overline{V_{S-R}^2} = 2 \cdot \left( \frac{gm_5}{gm_5 + gm_{13}} \right)^2 \cdot V_{i5}^2 + 4 \cdot \left( \frac{gm_7}{gm_5 + gm_{13}} \right)^2 \cdot V_{i7}^2 \quad \text{(B.16)}$$

Once again the thermal and flicker noise are independent, therefore they can be considered separately.

$$\overline{V_{i5}^{\,2}} = \overline{V_{i5(thermal)}^{\,2}} + \overline{V_{i5(flicker)}^{\,2}} = \left(\frac{K_p}{W_5 \cdot L_5 \cdot C_{ox} \cdot f}\right) \cdot \Delta f + \left(\frac{8 \cdot k \cdot T}{3 \cdot gm_5}\right) \cdot \Delta f \qquad \text{(B.17)}$$

$$\overline{V_{i13}^{\,2}} = \overline{V_{i13(thermal)}^{\,2}} + \overline{V_{i13(flicker)}^{\,2}} = \left(\frac{K_N}{W_{13} \cdot L_{13} \cdot C_{ox} \cdot f}\right) \cdot \Delta f + \left(\frac{8 \cdot k \cdot T}{3 \cdot gm_{13}}\right) \cdot \Delta f \qquad \text{(B.18)}$$

Substituting Equation B.17 and Equation B.18 into Equation B.16, the equivalent noise generator for the S-R can be expressed as:

$$\begin{aligned}\overline{V_{S-R}^{\,2}} = {} & 4 \cdot \left(\frac{gm_5}{gm_5 + gm_{13}}\right)^2 \cdot \left(\frac{K_p}{W_5 \cdot L_5 \cdot C_{ox} \cdot f} + \frac{8 \cdot k \cdot T}{3 \cdot gm_5}\right) \cdot \Delta f \\ & + \; 4 \cdot \left(\frac{gm_{13}}{gm_5 + gm_{13}}\right)^2 \cdot \left(\frac{K_N}{W_5 \cdot L_{13} \cdot C_{ox} \cdot f} + \frac{8 \cdot k \cdot T}{3 \cdot gm_{13}}\right) \cdot \Delta f\end{aligned} \qquad \text{(B.19)}$$

The noise figure of the S-R latch is given by:

$$NF_{S-R} = 1 + \frac{\overline{V_{S-R}^{\,2}}}{4 \cdot k \cdot T \cdot R_s \cdot \Delta f} \qquad \text{(B.20)}$$

Also equivalent to:

$$NF_{S-R} = 1 + \frac{1}{4 \cdot k \cdot T \cdot R_s \cdot \Delta f} \cdot \left[\begin{array}{l} \left(\frac{gm_5}{gm_5 + gm_{13}}\right)^2 \cdot \left(\frac{K_p}{W_5 \cdot L_5 \cdot C_{ox} \cdot f} + \frac{8 \cdot k \cdot T}{3 \cdot gm_5}\right) \\ + \left(\frac{gm_{13}}{gm_5 + gm_{13}}\right)^2 \cdot \left(\frac{K_N}{W_5 \cdot L_{13} \cdot C_{ox} \cdot f} + \frac{8 \cdot k \cdot T}{3 \cdot gm_{13}}\right) \end{array}\right] \qquad \text{(B.21)}$$

The total noise figure of the comparator is given by:

$$NF_{Comp} = NF_{latch} \cdot NF_{S-R} \quad = \quad 4.48\,dB \tag{B.22}$$

# Appendix C

# *Cadence Power Consumption Measurement Flow*

Figure C.1 illustrates the cadence power consumption measurement flow.

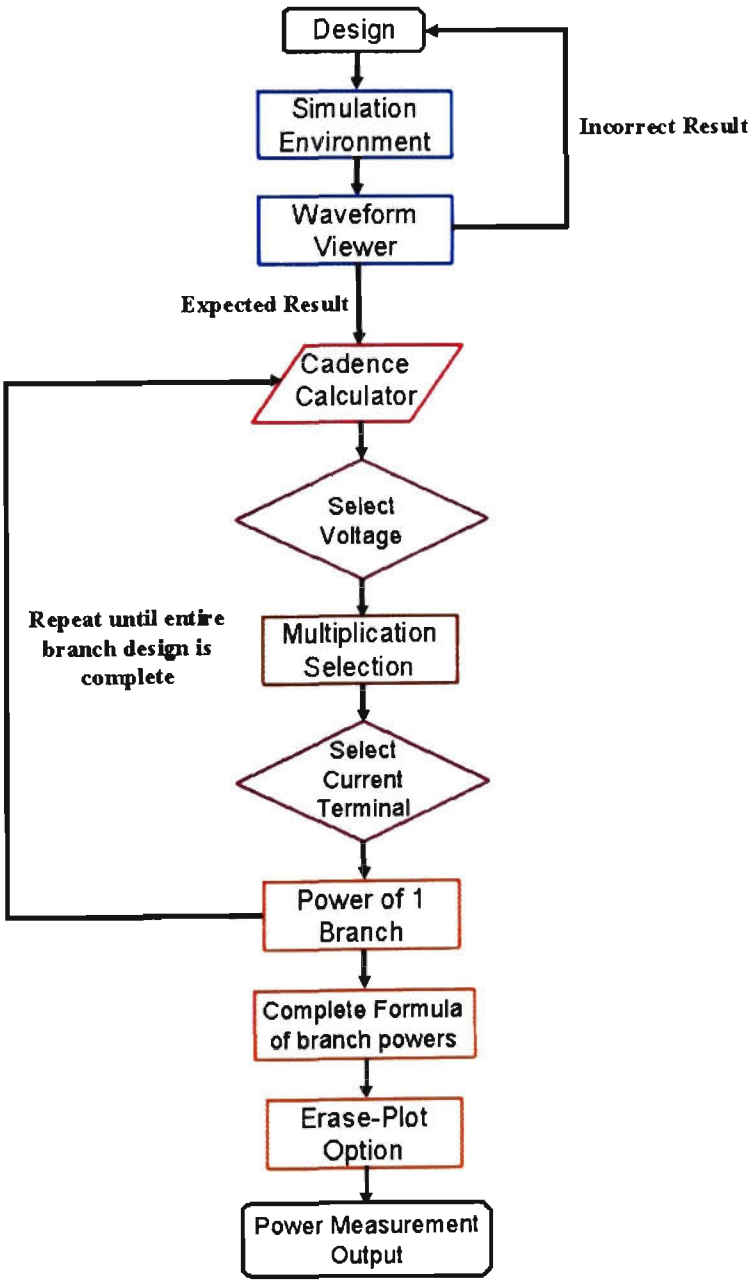


Figure C.1: Cadence Power Consumption Measurement Flow